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MAR 31 1987
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PATENT PROFILES

MICROELECTRONICS - I

PATENT PROFILES

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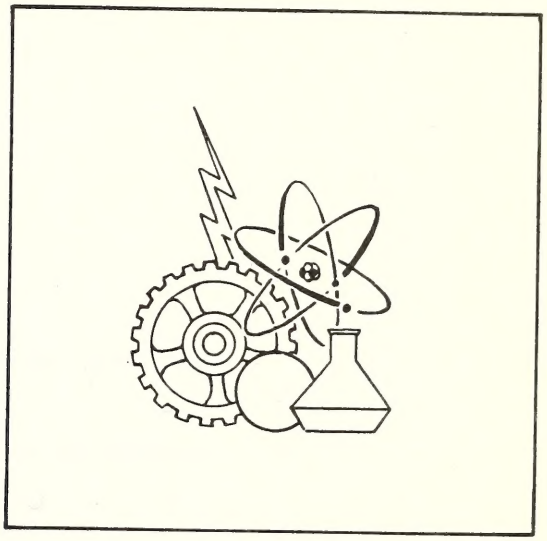
& FORECAST



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INTRODUCTION

Background

Patents, as incentives for innovation, are well established in the U.S. free-enterprise system. Often overlooked, however, is a second great benefit of the patent system: the enormous, continually expanding patent file. This file includes more than 4 million distinct U.S. patents. These patents are classified and cross-referenced among the approximately 100,000 categories of technology that make up the U.S. Patent Classification System. Along with similarly categorized foreign patents and other technical publications, they make up a collection totaling about 24 million documents -- a collection which grows by over half a million documents annually.

Patent law requirements for a full disclosure of invention (which is then published as part of a patent grant) have resulted in a unique assemblage of technological information. Not only does the patent file embody the most comprehensive collection of technical information of its kind in the world, the information is inherently presented in a manner such that nearly every significant development in almost all technical fields flows in a natural time-series sequence -- virtually welcoming monitoring and analysis.

In its own unique way, this file represents a national resource. The Patent and Trademark Office (PTO) recognizes the heavy responsibilities not only to preserve, maintain, and improve the file, but, as well, to maximize its use for the greatest public benefit. As part of the effort to discharge this latter responsibility, the Patent and Trademark Office established, in 1971, its technology assessment and forecast program.

In its most general terms, the mission of the program is to stimulate and enhance the use and usability of the patent file, and to assemble, analyze and make available meaningful data about the file. In carrying out this mission, the Office of Technology Assessment and Forecast (OTAF), which administers the program, has assembled and built a master data base covering all U.S. patents. This data base has been used to support: (1) the preparation of a series of eleven OTAF publications (see Appendix B); and (2) OTAF's special report services (see Appendix C).

Patent Profiles

In an effort to continually provide data in a form which is useful and convenient to the interested reader, OTAF, in December 1979, initiated a new publication series -- PATENT PROFILES. Each publication deals with a specific technological area and surveys the patent activity of that area for a given period of time.

PATENT PROFILES provides many different kinds of information about a particular area of the patent file and assembles this information in a format which enables the user to extract easily the information needed.

Thus, interested users, both technically and non-technically oriented, from the public and private sectors, will be able to gain insight into the "who, what and where" of the patent activity in a technology and, perhaps, discern the direction the technology is headed.

The objective of these publications is to increase the awareness and use of the U.S. patent file as a prime technological information resource, so that the file may contribute more fully to the knowledge from which future inventors and innovators draw, and upon which corporate and public policy planners rely.

About This Publication

In 1957, Patent Number 2,816,228 was issued to Harwick Johnson for an invention in phase shift oscillators. The major difference between that invention and the oscillators that had been known before was the fact that the entire circuit was included on a single chip of germanium.

Improvements in single crystal growing, lithography, computer controlled design aids, automatic test equipment and other techniques and devices have led us from that beginning to the present, rapidly expanding, state of the art of microelectronics. Today, microelectronics has spread into many areas of our lives, from wrist watches, pocket calculators and TV games to control systems for our home appliances and automobiles.

This publication is directed to two major areas of microelectronics. The first relates to specific integrated circuit structure. The second relates to systems in which the inventive thrust involves the use of a microelectronic information processing device, for example a central processing unit or "CPU."

Obviously, these two areas encompass but a portion of the highly active field of microelectronics technology. Yet, that high activity (i.e., the large number of patents being granted) limits the coverage that can be provided in a single publication. Consequently, depending on interest and available resources, a series of follow-on reports is planned covering such areas, for example, as microelectronic memory devices and microelectronic device manufacturing techniques.

The reader should understand, however, that no feasible series of publications could cover, comprehensively, all U.S. patenting which is pertinent to microelectronics. The field has simply become too diverse. We will attempt, therefore, to "snapshot" the patent activity in selected portions of the patent file which relate to important segments of microelectronics technology development. The purpose is two-fold: first, to present a range of information about the present "actors" and activity in the technology; and second, as noted above, to stimulate an awareness of the richness of the patent file as a technological information resource.

EXPLANATION OF DATA AND FORMAT

This report presents profiles of patenting* in two areas of microelectronics. Each of the profiles is divided into four parts:

PART 1

Part 1, the first page of each profile, identifies the area which is examined, lists the pertinent U.S. Patent Classification(s) involved, and graphically illustrates patent activity (across a designated 10-year span) in two ways: (1) by the patent grant date; (2) by the granted patents' application filing date. The latter method presents what is often considered a more useful measurement tool since application filing dates are closer in time to the actual development of the technology disclosed in the patent and are independent of PTO production variance.** The relative growth in the particular technological area, as well as levels of involvement by foreign residents, corporations, and government agencies, expressed as a percentage of recent U.S. patent activity, are presented in the "Activity Indices" (defined below).

EXAMPLE

CPU'S AND OTHER SYSTEMS

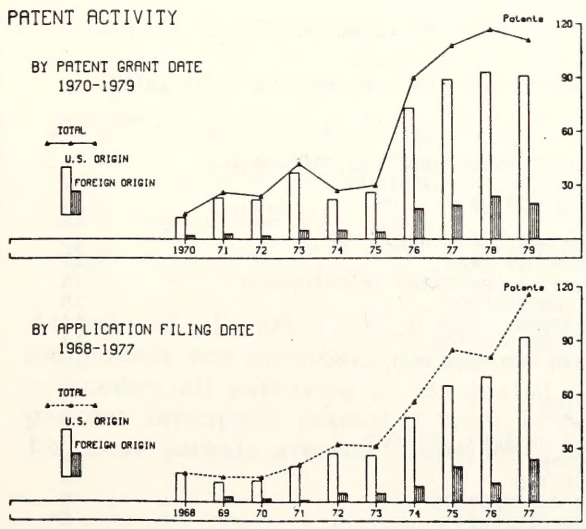
This profile is drawn to systems in which the inventive thrust involves the use of microelectronic processing devices, e.g., CPU's.

INCLUDED IN THIS PROFILE ARE SELECTED PATENTS FROM:

Class 364, Subclasses 200 and 900

ACTIVITY INDICES (1977-1979)

GROWTH	57.0%
FOREIGN SHARE	18.8%
CORPORATE OWNED	91.7%
GOVERNMENT OWNED	1.8%
U.S. OWNED OF FOREIGN	12.7%



TECHNOLOGY SCOPE

U.S. PATENT CLASSIFICATION

ACTIVITY INDICES - DEFINED

% GROWTH: The number of patents granted in the period 1977-79 divided by the total number of patents granted in the period 1970-79, multiplied by 100. (Average for all technologies = 26.1%)

% FOREIGN SHARE: The number of patents granted to residents of foreign countries in the years 1977-79, divided by total number of patents granted in these years, multiplied by 100. (Average for all technologies = 37.4%)

% CORPORATE OWNED: The number of 1977-79 patents assigned at time of grant to U.S. or foreign non-government organizations -- mainly corporations -- divided by the total number of patents granted in this three year period, multiplied by 100. (Average for all technologies = 76.1%)

% GOVERNMENT OWNED: The number of 1977-79 patents assigned at time of grant to the U.S. Government or a foreign government, divided by total number of patents granted in this three year period, multiplied by 100. (Average for all technologies = 2.4%)

% U.S. OWNED OF FOREIGN: The number of 1977-79 patents with a foreign resident inventor assigned at the time of grant to a U.S. organization, divided by the number of patents with a foreign resident inventor in these years, multiplied by 100. (Average for all technologies = 8.2%)

The information on this page can be interpreted as indicative of trends in the direction and rate of growth of the subject technology.

---

* U.S. Patents only

**See further explanation in Appendix A.

PART 2A

Part 2A of each profile shows in tabular form the data relied upon in constructing the graphical illustrations in Part 1. The first table shows the yearly distribution of patents by the date of the patent grant, while the second table redistributes these data based on the application filing date of the patents. The usefulness of this latter data distribution is mentioned in the explanation of Part 1, and further detailed in Appendix A.

EXAMPLE

MICROELECTRONICS - INTEGRATED CIRCUIT STRUCTURE

PATENT ACTIVITY (1963-1979) BY DATE OF PATENT GRANT

	NUMBER OF PATENTS									
	63-65	1966	1967	1968	1969	1970	1971	1972	1973	1974
TOTAL	116	94	117	168	233	179	276	215	241	187
U.S. ORIGIN	102	82	108	139	182	144	200	145	160	127
FOREIGN ORIGIN	14	12	9	29	51	35	76	70	81	60
JAPAN	5	4	2	6	15	9	30	30	37	27
GERMANY	2	1	2	7	14	7	13	15	11	15
NETHERLANDS	1	2	1	1	2	6	15	14	11	6
UNITED KINGDOM	3	3		4	7	5	6	5	6	5
FRANCE	1	2	1	5	6	4	8	4	9	4
CANADA			1	3	3	1	1	1	4	
SWITZERLAND	2			2	2	1		1	2	2
ITALY				1		1	2			1
SWEDEN					1					
U.S.S.R.										
CZECHOSLOVAKIA			1							
AUSTRIA							1			
BELGIUM						1				
GREECE					1					
DENMARK			1							
BURMA										
BULGARIA									1	
ISRAEL										
SOUTH AFRICA										
U.S. ORIGIN	102	82	108	139	182	144	200	145	160	127
U.S. CORP. OWNED	94	80	100	132	175	139	185	134	150	120
U.S. GOVT. OWNED	2	1	3	2	2		4	4	3	2

PART 2B

Part 2B of each profile provides a list of assignees* ranked by the number of patents, in the technology, to which they held title at the time of the patent grant. The listing is limited by designation of a "cut-off" (e.g., "3 or more patents"). The time period covered is 1969-1979. This list identifies those assignees (mostly corporations), which received the most patents in the technology encompassed by the profile during the subject time period, and shows the comparative relationship of their activity to that of the other participants in the field.

EXAMPLE

CPU'S AND OTHER SYSTEMS

ASSIGNEES WITH 3 OR MORE PATENTS (1/69-12/79)

INTERNATIONAL BUSINESS MACHINES CORPORATION	73
TEXAS INSTRUMENTS, INCORPORATED	72
BURROUGHS CORPORATION	34
MOTOROLA INC.	28
HONEYWELL INFORMATION SYSTEMS INC.	26
HEWLETT-PACKARD COMPANY	17
BELL TELEPHONE LABORATORIES INCORPORATED	15
SPERRY RAND CORPORATION	15
XEROX CORPORATION	14
DATA GENERAL CORPORATION	13
TOKYO SHIBAURA ELECTRIC CO., LTD.	10
HITACHI, LTD.	9
NCR CORPORATION	9
HONEYWELL INC.	9
UNITED STATES OF AMERICA, NAVY	9
RCA CORPORATION	8
INTEL CORPORATION	6
U.S. PHILIPS CORPORATION	6
ALLEN-BRADLEY COMPANY	6*
OLYMPIA WERKE AG	5

---

*See definition in Appendix A.

PART 2C

Part 2C of each profile also covers assigned patenting during the period 1969-1979. Assignees are listed alphabetically followed by a numerical listing of their patents with titles.

This section provides valuable information to potential entrepreneurs, competitors and those in need of technological know-how by identifying corporate actors in the field. Inclusion of patent titles further defines the subject technology.

EXAMPLE

```
MICROELECTRONICS - INTEGRATED CIRCUIT STRUCTURE

                    ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

ADVANCED MICRO DEVICES, INC.
  4042950  -  PLATINUM SILICIDE FUSE LINKS FOR INTEGRATED CIRCUIT DEVI
  4135295  -  PROCESS OF MAKING PLATINUM SILICIDE FUSE LINKS FOR INTEG

AEROJET-GENERAL CORPORATION
  3436668  -  BROAD BAND AMPLIFIERS USING DISTRIBUTED RC NETWORK
  3436669  -  NARROW BAND AMPLIFIERS USING DISTRIBUTED RC NETWORK

AERONUTRONIC FORD CORPORATION (FORMERLY PHILCO-FORD CORP.)
  3447092  -  TRANSISTOR AMPLIFYING CIRCUIT HAVING HIGH INPUT IMPEDANC
  3454785  -  SHIFT REGISTER EMPLOYING INSULATED GATE FIELD EFFECT TRA
  3502515  -  METHOD OF FABRICATING SEMICONDUCTOR DEVICE WHICH INCLUDE
  3576478  -  IGFET COMPRISING N-TYPE SILICON SUBSTRATE, SILICON OXIDE

AGENCE NATIONALE DE VALORISATION DE LA RECHERCHE (ANVAR)
  3813585  -  COMPOUND SEMICONDUCTOR DEVICE HAVING UNDERCUT ORIENTED (
  4035831  -  RADIAL EMITTER PRESSURE CONTACT TYPE SEMICONDUCTOR DEVI(
  4077044  -  NONVOLATILE MEMORY SEMICONDUCTOR DEVICE

ALPHA INDUSTRIES INC.
  3800412  -  PROCESS FOR PRODUCING SURFACE-ORIENTED SEMICONDUCTING DI
```

PART 2D

Part 2D of each profile presents an alphabetical listing of inventors of unassigned patents (1975 to 1979) together with their addresses, the patent numbers and titles. This information facilitates identification of the apparently unaffiliated or "independent inventor" participants in the technology. Standard, two character codes are used to designate U.S. states and foreign countries. While the meaning of state codes should be obvious, the foreign country codes may not. Consequently, those appearing in the Part 2D listing are defined in Appendix A.

EXAMPLE

```
MICROELECTRONICS - CPUS AND OTHER SYSTEMS                                                                    PAGE D

                                UNASSIGNED PATENTS(1/75-12/79) INVENTORS(ALPHA LISTING)

  INVENTOR NAME                                    STREET                          CITY                  ST    ZIP/CNTRY

  VANDIERENDONCK      JERRY          L.            645 GLENWOOD CUTOFF             SANTA CRUZ            CA      95060
 3987416  -  ELECTRONIC CALCULATOR WITH DISPLAY AND KEYBOARD SCANNING SIGNAL GENERATOR IN DATA MEMORY

  VASENKOV            ALEXANDR       A.            ZELENOGRAD 103460, KORPUS 3, K  MOSCOW                        SU
 4124890  -  MICROPROCESSOR COMPUTING SYSTEM

  WALKER              RICHARD        L.            P.O. BOX 7344                   SAN DIEGO             CA      92107
 3918030  -  GENERAL PURPOSE DIGITAL COMPUTER

  WINKLER             DEAN           A.            R.R. +190 4, BOX 268            LOOGOOTEE             IN      47553
 4168527  -  ANALOG AND DIGITAL CIRCUIT TESTER
```

At the end of Part 2D is a list of those patents (1963-1979) with neither assignment nor inventor information in the data base. Essentially, this encompasses all patenting in the period 1963-1968, and non-assigned ("independent inventor") patenting from 1969 through 1974. Titles are included for most patents granted subsequent to January, 1969.

```
                    PATENTS (1/63-12/79) WITH NEITHER ASSIGNMENT NOR INVENTOR INFORMATION IN DATABASE

 3597744  -  DIGITAL COMPUTING AND INFORMATION PROCESSING MACHINE AND SYSTEM
 3711837  -  HEADLINE COUNTING AND PRINTING DESIGN DEVICE
 3735361  -  INFORMATION STORE SYSTEM HAVING DATA BLOCK SHIFT REGISTERS
 4159536  -  PORTABLE ELECTRONIC LANGUAGE TRANSLATION DEVICE
 4179733  -  COMPUTER FOR CONTROL OF COMMUNICATION SIGNALS
        3167685   3268871   3292151   3332069   3340513   3350690   3372379   3374465   3389380   3401376   3403383   3416139
```

PART 3

Part 3 of each profile updates the preceding material and is directed to those patents which issued from January to October, 1980. The first page is a ranked listing of assignees having two or more patents for the time period. The pages which follow the list, show the title page of each patent in the update. These pages are grouped by assignee in the order in which they appear on the ranked list. Title pages of patents to assignees having only one patent and to independent inventors follow, arranged in alphabetical order, respectively.

PART 4

Part 4 of each profile provides information about the references which were cited during the examination period of patents which issued in the technology between 1975 and 1979. This information may be indicative of the countries, corporations and patents which dominate the technological area. The total number of U.S. Patents which issued is given, followed by the total number of references considered by the examiner during the examination of these patents. The number of references is given in three categories -- U.S., foreign and non-patent references. For those reference citations which are U.S. Patents, there are included: 1) the distribution according to the country of origin; 2) a list of the four most frequently cited patents and the number of times each was cited; 3) a list of the four most frequently cited assignees and the number of times each was cited; and 4) the title pages of the four most frequently cited patents. A more detailed explanation of this information appears in Appendix A.

PATENTS INCLUDED IN THE PROFILES

Patent activity profiles are normally generated by first identifying key Patent and Trademark Office classifications, i.e., those entirely or substantially pertinent to the technology of interest. All the patents in these classifications are then included in the profile. This procedure results, in most cases, with the inclusion of the majority of patents relevant to the technology and few non-relevant patents. While one can never be sure of the absolute completeness or "purity" of any subset in a collection as large and varied as the patent file, it is felt that the patent file portions selected for review in this publication include patents representative of the overall trends in the defined areas and essentially exclude patents which are not relevant to the subject technology.

IMPORTANT NOTE:
It should also be noted that in 1979, the Patent and Trademark Office issued substantially fewer patents than normal (about 49,000 as compared to about 66,000 in 1978) due to a lack of funds to print patents. Therefore, while the 1979 patent grant data may be low, the decrease should not be attributed to a fall-off in technological activity.

INTEGRATED CIRCUIT STRUCTURE

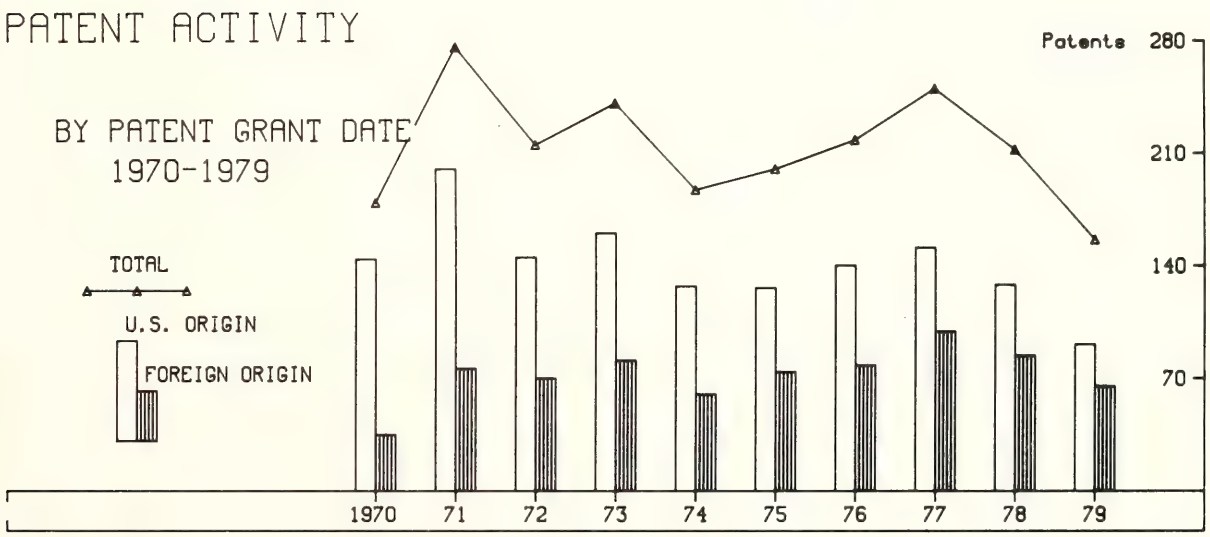
This profile includes circuits made up of plural electronic devices united in one structure or substrate. The structure of a potential barrier between two materials, at least one of which is semiconductive, is significantly described.

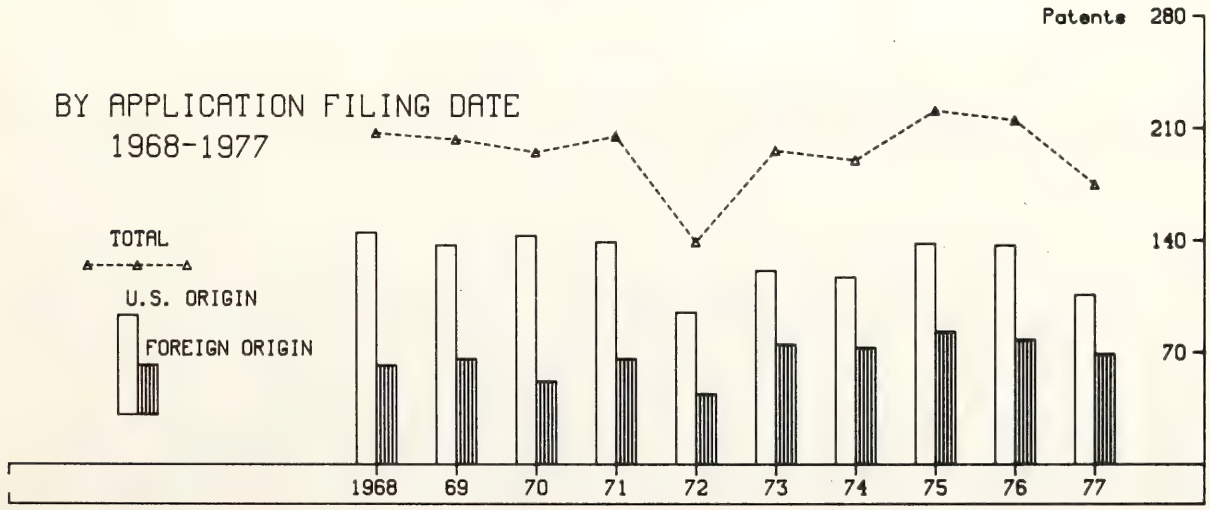
INCLUDED IN THIS PROFILE ARE ALL OF THE PATENTS FROM:

Class 357, Subclasses 40-51

ACTIVITY INDICES (1977-1979)

GROWTH	29.0%
FOREIGN SHARE	40.1%
CORPORATE OWNED	96.3%
GOVERNMENT OWNED	1.9%
U.S. OWNED OF FOREIGN	20.6%





MICROELECTRONICS - INTEGRATED CIRCUIT STRUCTURE

PATENT ACTIVITY (1963-1979) BY DATE OF PATENT GRANT

	NUMBER OF PATENTS															
	63-65	1966	1967	1968	1969	1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	TOTAL
TOTAL	116	94	117	168	233	179	276	215	241	187	200	218	250	212	156	2862
U.S. ORIGIN	102	82	108	139	182	144	200	145	160	127	126	140	151	128	91	2025
FOREIGN ORIGIN	14	12	9	29	51	35	76	70	81	60	74	78	99	84	65	837
JAPAN	5	4	2	6	15	9	30	30	37	27	39	39	54	46	37	380
GERMANY	2	1	2	7	14	7	13	15	11	15	9	11	21	12	10	150
NETHERLANDS	1	2	1	1	2	6	15	14	11	6	14	10	8	8	6	105
UNITED KINGDOM	3	3		4	7	5	6	5	6	5	4	9	5	4	5	71
FRANCE	1	2	1	5	6	4	8	4	9	4		6	6	9	4	69
CANADA			1	3	3	1	1	1	4		1		1	1		17
SWITZERLAND	2			2	2	1		1	2	2	2		2		1	17
ITALY				1		1	2			1	1			2	1	9
SWEDEN					1						2		1	1		5
U.S.S.R.											2	2	1			5
CZECHOSLOVAKIA			1													1
AUSTRIA							1									1
BELGIUM						1										1
GREECE					1											1
DENMARK			1													1
BURMA															1	1
BULGARIA									1							1
ISRAEL												1				1
SOUTH AFRICA														1		1
U.S. ORIGIN	102	82	108	139	182	144	200	145	160	127	126	140	151	128	91	2025
U.S. CORP. OWNED	94	80	100	132	175	139	185	134	150	120	119	135	144	116	88	1911
U.S. GOVT. OWNED	2	1	3	2	2		4	4	3	2	1	2	3	6	3	38
U.S. INDIV. OWNED	5	1	5	5	4	4	7	7	6	5	5	3	4	6		67
FOREIGN OWNED	1				1	1	4		1		1					9
FOREIGN ORIGIN	14	12	9	29	51	35	76	70	81	60	74	78	99	84	65	837
U.S. OWNED	3	4	1	5	15	16	34	25	23	13	21	25	21	14	16	236
FOREIGN OWNED	11	8	8	24	36	19	42	45	58	47	53	53	78	70	49	601
FOREIGN CORP.	9	8	8	21	34	19	38	42	56	44	47	50	77	70	49	572
FOREIGN GOVT.									1							1
FOREIGN INDIV.	2			3	2		4	3	1	3	6	3	1			28

MICROELECTRONICS - INTEGRATED CIRCUIT STRUCTURE

PATENT ACTIVITY (PATENTS GRANTED 1/67-12/79) BY DATE OF PATENT APPLICATION

	NUMBER OF PATENTED APPLICATIONS															
	PRE 66	1966	1967	1968	1969	1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	TOTAL
TOTAL	313	152	185	207	203	195	205	139	196	190	221	215	175	56		2652
U.S. ORIGIN	267	121	141	145	137	143	139	95	121	117	138	137	106	34		1841
FOREIGN ORIGIN	46	31	44	62	66	52	66	44	75	73	83	78	69	22		811
JAPAN	9	4	21	22	30	26	28	19	42	36	42	44	35	13		371
GERMANY	14	12	5	9	15	9	11	7	11	9	18	13	11	3		147
NETHERLANDS	4	1	4	14	9	8	9	7	9	11	8	8	7	3		102
UNITED KINGDOM	7	4	5	3	7	2	7	3	5	5	7	6	2	2		65
FRANCE	6	4	3	11	2	5	5	3	2	7	5	4	8	1		66
CANADA	3	1	3	1	1		3	3				1	1			17
SWITZERLAND	1	3			1	2	1	1	2	2	1		1			15
ITALY		1	1	2			1	1				1	2			9
SWEDEN		1							2		1		1			5
U.S.S.R.									2	2	1					5
CZECHOSLOVAKIA	1															1
AUSTRIA					1											1
BELGIUM			1													1
GREECE			1													1
DENMARK	1															1
BURMA													1			1
BULGARIA							1									1
ISRAEL										1						1
SOUTH AFRICA												1				1
U.S. ORIGIN	267	121	141	145	137	143	139	95	121	117	138	137	106	34		1841
U.S. CORP. OWNED	254	115	133	136	133	134	128	87	112	114	131	130	97	33		1737
U.S. GOVT. OWNED	4		3	2	1	4	3	1	3	1	3	4	5	1		35
U.S. INDIV. OWNED	9	5	4	4	2	5	7	6	6	2	4	3	4			61
FOREIGN OWNED		1	1	3	1		1	1								8
FOREIGN ORIGIN	46	31	44	62	66	52	66	44	75	73	83	78	69	22		811
U.S. OWNED	12	8	10	31	24	12	20	13	17	24	23	12	17	6		229
FOREIGN OWNED	34	23	34	31	42	40	46	31	58	49	60	66	52	16		582
FOREIGN CORP.	31	23	33	29	40	36	43	30	52	45	59	66	52	16		555
FOREIGN GOVT.							1									1
FOREIGN INDIV	3		1	2	2	4	2	1	6	4	1					26

INTEGRATED CIRCUIT STRUCTURE

ASSIGNEES WITH 7 OR MORE PATENTS (1/69-12/79)

INTERNATIONAL BUSINESS MACHINES CORPORATION	289
TEXAS INSTRUMENTS, INC.	194
U.S. PHILIPS CORPORATION	163
RCA CORPORATION	153
HITACHI, LTD.	131
MOTOROLA INC.	121
WESTINGHOUSE ELECTRIC CORP.	80
BELL TELEPHONE LABORATORIES INCORPORATED	79
GENERAL ELECTRIC COMPANY	78
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*COMPOSITE TOTAL, SEE APPENDIX A

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

ADVANCED MICRO DEVICES, INC.
4042950 - PLATINUM SILICIDE FUSE LINKS FOR INTEGRATED CIRCUIT DEVICES
4135295 - PROCESS OF MAKING PLATINUM SILICIDE FUSE LINKS FOR INTEGRATED CIRCUIT DEVICES

AEROJET-GENERAL CORPORATION
3436668 - BROAD BAND AMPLIFIERS USING DISTRIBUTED RC NETWORK
3436669 - NARROW BAND AMPLIFIERS USING DISTRIBUTED RC NETWORK

AERONUTRONIC FORD CORPORATION (FORMERLY PHILCO-FORD CORP.)
3447092 - TRANSISTOR AMPLIFYING CIRCUIT HAVING HIGH INPUT IMPEDANCE AND TEMPERTURE-STABILIZED OUTPUT POTENTIAL
3454785 - SHIFT REGISTER EMPLOYING INSULATED GATE FIELD EFFECT TRANSISTORS
3502515 - METHOD OF FABRICATING SEMICONDUCTOR DEVICE WHICH INCLUDES REGION IN WHICH MINORITY CARRIERS HAVE SHORT LIFETIME
3576478 - IGFET COMPRISING N-TYPE SILICON SUBSTRATE, SILICON OXIDE GATE INSULATOR AND P-TYPE POLYCRYSTALLINE SILICON GATE ELECTROD
E

AGENCE NATIONALE DE VALORISATION DE LA RECHERCHE (ANVAR)
3813585 - COMPOUND SEMICONDUCTOR DEVICE HAVING UNDERCUT ORIENTED GROOVE
4035831 - RADIAL EMITTER PRESSURE CONTACT TYPE SEMICONDUCTOR DEVICES
4077044 - NONVOLATILE MEMORY SEMICONDUCTOR DEVICE

ALPHA INDUSTRIES INC.
3800412 - PROCESS FOR PRODUCING SURFACE-ORIENTED SEMICONDUCTING DEVICE

AMDAHL CORPORATION
3808475 - LSI CHIP CONSTRUCTION AND METHOD

AMERICAN MICRO-SYSTEMS, INC.
3478229 - MULTIFUNCTION CIRCUIT DEVICE
3924265 - LOW CAPACITANCE V GROOVE MOS NOR GATE AND METHOD OF MANUFACTURE
3975221 - LOW CAPACITANCE V GROOVE MOS NOR GATE AND METHOD OF MANUFACTURE
4003036 - SINGLE IGFET MEMORY CELL WITH BURIED STORAGE ELEMENT
4057844 - MOS INPUT PROTECTION STRUCTURE
4105475 - EPITAXIAL METHOD OF FABRICATING SINGLE IGFET MEMORY CELL WITH BURIED STORAGE ELEMENT

AMF INTERNATIONAL LIMITED, MESNE
3597641 - INTEGRATED CIRCUIT CHIPS

ANALOG DEVICES, INC.
3747088 - SOLID STATE DIGITAL-TO-ANALOG CONVERTER
4123698 - INTEGRATED CIRCUIT TWO TERMINAL TEMPERATURE TRANSDUCER

ARBEITSSTELLE FUR MOLEKULARELEKTRONIK KONIGSBRUCKER -
3562548 - CIRCUIT ARRANGEMENT WITH SEMICONDUCTOR ELEMENTS
3579058 - SEMICONDUCTOR MODULE AND METHOD OF THE PRODUCTION
3610949 - CIRCUIT FOR PERFORMING LOGIC FUNCTIONS
3725146 - FABRICATION OF INTEGRATED MICROCIRCUITS UTILIZING DIELECTRIC-P-N JUNCTION ISOLATION

ASEA AKTIEBOLAG
3486103 - THYRISTOR RECTIFIER COMPRISING SERIES CONNECTED THYRISTORS OF ALTERNATELY PNPN AND NPNP TYPE

ASTRONICS CORPORATION
3883887 - METAL OXIDE SWITCHING ELEMENTS

ATES COMPONENTI ELECTRONICI S.P.A.
3885999 - PLANAR EPITAXIAL PROCESS FOR MAKING LINEAR INTEGRATED CIRCUITS

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

BATTELLE MEMORIAL INSTITUTE
3845331 - ARRANGEMENTS FOR BIASING THE SUBSTRATE OF AN INTEGRATED CIRCUIT

BECKMAN INSTRUMENTS INC.
3497774 - ELECTRICAL CIRCUIT MODULE AND METHOD OF MANUFACTURE

BELL CANADA-NORTHERN ELECTRIC RESEARCH LIMITED
3775191 - MODIFICATION OF CHANNEL REGIONS IN INSULATED GATE FIELD EFFECT TRANSISTORS

BELL TELEPHONE LABORATORIES INCORPORATED
3420706 - TECHNIQUE FOR FABRICATION OF PRINTED CIRCUIT RESISTORS
3421029 - BISTABLE CIRCUIT EMPLOYING NEGATIVE RESISTANCE SEMICONDUCTOR DIODES
3440477 - MULTIPLE READOUT ELECTRON BEAM DEVICE
3440715 - METHOD OF FABRICATING INTEGRATED CIRCUITS BY CONTROLLED PROCESS
3458782 - ELECTRON BEAM CHARGE STORAGE DEVICE EMPLOYING DIODE ARRAY AND ESTABLISHING AN IMPURITY GRADIENT IN ORDER TO REDUCE THE S URFACE RECOMBINATION VELOCITY
3476621 - IMPURITY DIFFUSION SOURCE AND METHOD
3483464 - VOLTAGE REGULATOR SYSTEMS EMPLOYING A MULTIFUNCTIONAL CIRCUIT COMPRISING A FIELD EFFECT TRANSISTOR CONSTANT CURRENT SOUR CE
3500066 - RADIO FREQUENCY POWER TRANSISTOR WITH INDIVIDUAL CURRENT LIMITING CONTROL FOR THERMALLY ISOLATED REGIONS
3500142 - FIELD EFFECT SEMICONDUCTOR APPARATUS WITH MEMORY INVOLVING ENTRAPMENT OF CHARGE CARRIERS
3500148 - MULTIPURPOSE INTEGRATED CIRCUIT ARRANGEMENT
3502950 - GATE STRUCTURE FOR INSULATED GATE FIELD EFFECT TRANSISTOR
3505527 - ELECTRONIC DRIVE CIRCUIT EMPLOYING SUCCESSIVELY ENABLED MULTISTATE IMPEDANCE ELEMENTS
3540010 - DIODE-COUPLED
3541531 - SEMICONDUCTIVE MEMORY ARRAY WHEREIN OPERATING POWER IS SUPPLIED VIA INFORMATION PATHS
3543052 - DEVICE EMPLOYING IGFET IN COMBINATION WITH SCHOTTKY DIODE
3553541 - BILATERAL SWITCH USING COMBINATION OF FIELD EFFECT TRANSISTORS AND BIPOLAR TRANSISTORS
3558366 - METAL SHIELDING FOR ION IMPLANTED SEMICONDUCTOR DEVICE
3559087 - DIFFERENCE AMPLIFIER WITH PARALLEL ISOLATED EMITTER CONFIGURATION
3575741 - METHOD FOR PRODUCING SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE
3585412 - SCHOTTKY BARRIER DIODES AS IMPEDANCE ELEMENTS
3586542 - SEMICONDUCTOR JUNCTION DEVICES
3591840 - CONTROLLABLE SPACE-CHARGE-LIMITED IMPEDANCE DEVICE FOR INTEGRATED CIRCUITS
3597706 - STRIP LINE SWITCH
3609593 - VIBRATORY REED DEVICE
3611317 - NESTED CHIP ARRANGEMNT FOR INTEGRATED CIRCUIT MEMORIES
3614480 - TEMPERATURE STABILIZED ELECTRONIC DEVICE
3614555 - MONOLITHIC INTEGRATED CIRCUIT STRUCTURE
3626313 - CLASS AB AMPLIFIER FOR MONOLITHIC INTEGRATED CIRCUIT
3638202 - ACCESS CIRCUIT ARRANGEMENT FOR EQUALIZED LOADING IN INTEGRATED CIRCUIT ARRAYS
3647585 - METHOD OF ELIMINATING PINHOLE SHORTS IN AN AIR-ISOLATED CROSSOVER
3649386 - METHOD OF FABRICATING SEMICONDUCTOR DEVICES
3653988 - METHOD OF FORMING MONOLITHIC SEMICONDUCTOR INTEGRATED CIRCUIT DEVICES
3661741 - FABRICATION OF INTEGRATED SEMICONDUCTOR DEVICES BY ELECTROCHEMICAL ETCHING
3665218 - CONTROL CIRCUIT FOR INSULATED GATE FIELD EFFECT TRANSISTORS
3667004 - ELECTROLUMINESCENT SEMICONDUCTOR DISPLAY APPARATUS
3674580 - ZIRCONIUM MASK FOR SEMICONDUCTOR FABRICATED USING ALKALINE ETCHANTS
3676715 - SEMICONDUCTOR APPARATUS FOR IMAGE SENSING AND DYNAMIC STORAGE
3693251 - METHOD OF FORMING CLOSELY SPACED CONDUCTIVE LAYERS
3701198 - MONOLITHIC INTEGRATED CIRCUIT STRUCTURES AND METHODS OF MAKING SAME
3715732 - TWO-TERMINAL NPN-PNP TRANSISTOR MEMORY CELL
3719797 - SOLID STATE TEMPERATURE SENSOR EMPLOYING A PAIR OF DISSIMILAR SCHOTTKY-BARRIER DIODES
3730787 - METHOD OF FABRICATING SEMICONDUCTOR INTEGRATED CIRCUITS USING DEPOSITED DOPED OXIDES AS A SOURCE OF DOPANT IMPURITIES
3731164 - COMBINED BIPOLAR AND FIELD EFFECT TRANSISTORS
3753248 - TWO-TERMINAL NONDESTRUCTIVE READ JFET-NPN TRANSISTOR SEMICONDUCTOR MEMORY

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

BELL TELEPHONE LABORATORIES INCORPORATED (CONTINUED)

3761744 - SEMICONDUCTOR CHARGE TRANSFER DEVICES
3767983 - CHARGE TRANSFER DEVICE WITH IMPROVED TRANSFER EFFICIENCY
3771147 - IGFET MEMORY SYSTEM
3786425 - INTEGRATED CIRCUIT SWITCHING NETWORK PROVIDING CROSSPOINT GAIN
3786493 - ANALOG TO DIGITAL CONVERTER USING A DRIFT TRANSISTOR
3793088 - COMPATIBLE PNP AND NPN DEVICES IN AN INTEGRATED CIRCUIT
3798139 - ELECTROLYTIC OXIDATION OF GALLIUM CONTAINING COMPOUND SEMICONDUCTORS
3801884 - CHARGE TRANSFER IMAGING DEVICES
3806774 - BISTABLE LIGHT EMITTING DEVICES
3825771 - IGFET INVERTER CIRCUIT
3831041 - COMPENSATING CIRCUIT FOR SEMICONDUCTIVE APPARATUS
3841918 - METHOD OF INTEGRATED CIRCUIT FABRICATION
3852799 - BURIED CHANNEL CHARGE COUPLED APPARATUS
3859642 - RANDOM ACCESS MEMORY ARRAY OF HYSTERESIS LOOP CAPACITORS
3866066 - POWER SUPPLY DISTRIBUTION FOR INTEGRATED CIRCUITS
3904450 - METHOD OF FABRICATING INJECTION LOGIC INTEGRATED CIRCUITS USING OXIDE ISOLATION
3909807 - INTEGRATED CIRCUIT MEMORY CELL
3914855 - METHODS FOR MAKING MOS READ-ONLY MEMORIES
3922571 - SEMICONDUCTOR VOLTAGE TRANSFORMER
3928092 - SIMULTANEOUS MOLECULAR BEAM DEPOSITION OF MONOCRYSTALLINE AND POLYCRYSTALLINE III(A)-V(A) COMPOUNDS TO PRODUCE SEMICONDUCTOR DEVICES
3962590 - TTL COMPATIBLE LOGIC GATE CIRCUIT
3967136 - INPUT CIRCUIT FOR SEMICONDUCTOR CHARGE TRANSFER DEVICE CIRCULATING MEMORY APPARATUS
3978515 - INTEGRATED INJECTION LOGIC USING OXIDE ISOLATION
4001858 - SIMULTANEOUS MOLECULAR BEAM DEPOSITION OF MONOCRYSTALLINE AND POLYCRYSTALLINE III(A)-V(A) COMPOUNDS TO PRODUCE SEMICONDUCTOR DEVICES
4030083 - SELF-REFRESHED CAPACITOR MEMORY CELL
4076556 - METHOD FOR FABRICATION OF IMPROVED BIPOLAR INJECTION LOGIC CIRCUIT
4087900 - FABRICATION OF SEMICONDUCTOR INTEGRATED CIRCUIT STRUCTURE INCLUDING INJECTION LOGIC CONFIGURATION COMPATIBLE WITH COMPLEMENTARY BIPOLAR TRANSISTORS UTILIZING SIMULTANEOUS FORMATION OF DEVICE REGIONS
4125853 - INTEGRATED CIRCUIT TRANSISTOR
4125855 - INTEGRATED SEMICONDUCTOR CROSSPOINT ARRANGEMENT
4127862 - INTEGRATED OPTICAL DETECTORS
4130827 - INTEGRATED CIRCUIT SWITCHING NETWORK USING LOW SUBSTRATE LEAKAGE CURRENT THYRISTOR CONSTRUCTION
4131910 - HIGH VOLTAGE SEMICONDUCTOR DEVICES
4140558 - ISOLATION OF INTEGRATED CIRCUITS UTILIZING SELECTIVE ETCHING AND DIFFUSION
4156246 - COMBINED OHMIC AND SCHOTTKY OUTPUT TRANSISTORS FOR LOGIC CIRCUIT
4167748 - HIGH VOLTAGE MONOLITHIC TRANSISTOR CIRCUIT

BENDIX CORPORATION

3462658 - MULTI-EMITTER SEMICONDUCTOR DEVICE
3963993 - POWER AMPLIFIER USING A PLURALITY OF PARALLEL CONNECTED AMPLIFIER ELEMENTS AND HAVING BURN-OUT PROTECTION

BOEING COMPANY

3466544 - INTEGRATED CIRCUITS HAVING INTEGRATED TEST TRANS- FORMATION NETWORKS INCORPORATED THEREWITH ON COMMON SUBSTRATE CHIPS

BROWN, BOVERI + CIE A. G.

3437889 - CONTROLLABLE SEMICONDUCTOR ELEMENT
3708732 - COMPOUND ELECTRICAL CIRCUIT UNIT COMPRISING A MAIN POWER TYPE THYRISTOR AND AUXILIARY CONTROL SEMICONDUCTOR ELEMENTS STRUCTURALLY AND ELECTRICALLY UNITED TO FORM A COMPACT ASSEMBLY
3746948 - SEMICONDUCTOR STRUCTURE INCORPORATING TUNNEL DIODES LOCATED IN THE PATH OF THE MAIN CURRENT FLOW

BULOVA WATCH COMPANY, INC.

3564245 - INTEGRATED CIRCUIT MULTI-CELL P-N JUNCTION RADIATION DETECTORS WITH DIODES TO REDUCE CAPACITANCE OF NETWORKS

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

BURROUGHS CORPORATION
3466461 - SEMICONDUCTOR DEVICE AND CIRCUIT FREE OF AVALANCHE OSCILLATIONS
3534237 - POWER ISOLATION OF INTEGRATED CIRCUITS
3997813 - MOS INTEGRATED CIRCUIT CHIP FOR DISPLAY PANELS
4021788 - CAPACITOR MEMORY CELL
4025907 - INTERLACED MEMORY MATRIX ARRAY HAVING SINGLE TRANSISTOR CELLS
4116720 - METHOD OF MAKING A V-MOS FIELD EFFECT TRANSISTOR FOR A DYNAMIC MEMORY CELL HAVING IMPROVED CAPACITANCE
4125933 - IGFET INTEGRATED CIRCUIT MEMORY CELL
4141027 - IGFET INTEGRATED CIRCUIT MEMORY CELL
4145702 - ELECTRICALLY PROGRAMMABLE READ-ONLY-MEMORY DEVICE
4153949 - ELECTRICALLY PROGRAMMABLE READ-ONLY-MEMORY DEVICE

CENTRE ELECTRONIQUE HORLOGER, S.A.
3453498 - SEMI-CONDUCTING RESISTANCE AND A METHOD FOR ITS MANUFACTURE
3491274 - DIFFUSED RESISTANCE IN AN INTEGRATED CIRCUIT
3810006 - CURRENT COMPARING DEVICE
4041522 - INTEGRATED CIRCUIT AND MANUFACTURE THEREOF

CITIZEN WATCH CO., LTD.
3905188 - ELECTRONIC TIMEPIECE

COGAR CORPORATION
3576549 - SEMICONDUCTOR DEVICE, METHOD AND MEMORY ARRAY
3629782 - RESISTOR WITH MEANS FOR DECREASING CURRENT DENSITY
3716469 - FABRICATION METHOD FOR MAKING AN ALUMINUM ALLOY HAVING A HIGH RESISTANCE TO ELECTROMIGRATION
3717564 - FABRICATION METHOD FOR MAKING AN ALUMINUM ALLOY HAVING A HIGH RESISTANCE TO ELECTROMIGRATION
3756876 - FABRICATION PROCESS FOR FIELD EFFECT AND BIPOLAR TRANSISTOR DEVICES
3760384 - FET MEMORY CHIP INCLUDING FET DEVICES THEREFOR AND FABRICATION METHOD

COMMISSARIAT A L+3 ENERGIE ATOMIQUE
3716290 - LIQUID-CRYSTAL DISPLAY DEVICE

COMMUNICATIONS TRANSISTOR CORPORATION
3742319 - R.F. POWER TRANSISTOR

COMPAGNIE GENERALE D+3 ELECTRICITE
3452206 - PHOTO-DIODE AND TRANSISTOR SEMICONDUCTOR RADIATION DETECTOR WITH THE PHOTO-DIODE BIASED SLIGHTLY BELOW ITS BREAKDOWN VOL TAGE
3707767 - MATRIX WITH INTERGRATED SEMICONDUCTORS FOR DEAD MEMORY

COMPAGNIE HONEYWELL BULL
3849757 - TANTALUM RESISTORS WITH GOLD CONTACTS

CONTINENTAL DEVICE CORPORATION
3632432 - GLASS COATED SEMICONDUCTOR

CORNELL AERONAUTICAL LABORATORY, INC.
3433677 - FLEXIBLE SHEET THIN-FILM PHOTOVOLTAIC GENERATOR

CORNING GLASS WORKS
3474304 - MONOLITHIC THIN-FILM DEVICES WITH ACTIVE AND RESISTIVE REGIONS

CSF-COMPAGNIE GENERALE DE TELEGRAPHIE SANS FIL
3436612 - SEMI-CONDUCTOR DEVICE HAVING DIELECTRIC AND METAL PROTECTORS
3492861 - STRAIN GAUGE ARRANGEMENT
3510806 - INDUCTIVE REACTANCE CIRCUIT

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

CSF-COMPAGNIE GENERALE DE TELEGRAPHIE SANS FIL (CONTINUED)
3521081 - LOGICAL CIRCUIT ELEMENT COMPRISING AN MOS FIELD EFFECT TRANSISTOR

CUTLER-HAMMER INC.
4134080 - LOW INDUCTANCE RESISTOR

DIONICS, INC.
3559283 - METHOD CIRCUITS
3680205 - METHOD OF PRODUCING AIR-ISOLATED INTEGRATED CIRCUITS
3918083 - BILATERAL SWITCHING INTEGRATED CIRCUIT
3920493 - METHOD OF PRODUCING A HIGH VOLTAGE PN JUNCTION
4001866 - MONOLITHIC, JUNCTION ISOLATED PHOTRAC
4001867 - SEMICONDUCTIVE DEVICES WITH INTEGRATED CIRCUIT SWITCHES
4068255 - MESA-TYPE HIGH VOLTAGE SWITCHING INTEGRATED CIRCUIT
4074293 - HIGH VOLTAGE PN JUNCTION AND SEMICONDUCTIVE DEVICES EMPLOYING SAME

DISPLAYTEK CORPORATION
3905094 - THERMAL DISPLAY MODULE

E. I. DU PONT DE NEMOURS AND COMPANY
3864715 - DIODE ARRAY-FORMING ELECTRICAL ELEMENT
3990098 - STRUCTURE CAPABLE OF FORMING A DIODE AND ASSOCIATED CONDUCTIVE PATH

ELECTRONICS ARRAYS, INC.
3609406 - INTEGRATED CIRCUIT INVERTER
3673427 - INPUT CIRCUIT STRUCTURE FOR MOS INTEGRATED CIRCUITS
3878404 - INTEGRATED CIRCUIT OF THE MOS VARIETY

ENERGY CONVERSION DEVICES, INC.
3634927 - METHOD OF SELECTIVE WIRING OF INTEGRATED ELECTRONIC CIRCUITS AND THE ARTICLE FORMED THEREBY
3675090 - FILM DEPOSITED SEMICONDUCTOR DEVICES
3699543 - COMBINATION FILM DEPOSITED SWITCH UNIT AND INTEGRATED CIRCUITS
3886577 - FILAMENT-TYPE MEMORY SEMICONDUCTOR DEVICE AND METHOD OF MAKING THE SAME

ENGLISH ELECTRIC COMPANY LIMITED
3637425 - INSULATING COATING ON SILICON

ENGLISH ELECTRIC VALVE COMPANY LIMITED
4060823 - ELECTRON-EMISSIVE SEMICONDUCTOR DEVICES

FAIRCHILD CAMERA AND INSTRUMENT CORPORATION
3439214 - BEAM-JUNCTION SCAN CONVERTER
3465293 - DETECTOR ARRAY CONTROLLING MOS TRANSISTOR MATRIX
3488564 - PLANAR EPITAXIAL RESISTORS
3488636 - OPTICALLY PROGRAMMABLE READ ONLY MEMORY
3489961 - MESA ETCHING FOR ISOLATION OF FUNCTIONAL ELEMENTS IN INTEGRATED CIRCUITS
3498833 - DOUBLE MASKING TECHNIQUE FOR INTEGRATED CIRCUIT
3509433 - CONTACTS FOR BURIED LAYER IN A DIELECTRICALLY ISOLATED SEMICONDUCTOR POCKET
3530443 - MOS GATED RESISTOR MEMORY CELL
3550256 - CONTROL OF SURFACE INVERSION OF P AND N-TYPE SILICON USING DENSE DIELECTRICS
3562721 - SOLID STATE SWITCHING AND MEMORY APPARATUS
3571674 - FAST SWITCHING PNP TRANSISTOR
3586922 - MULTIPLE LAYER METAL STRUCTURE AND PROCESSING
3606679 - METHOD FOR INTERCONNECTING SOLID STATE DEVICES SUCH AS INTEGRATED CIRCUIT CHIPS
3609413 - CIRCUIT FOR THE PROTECTION OF MONOLITHIC SILICON CONTROLLED RECTIFIERS FROM FALSE TRIGGERING
3611067 - COMPLEMENTARY NPN/PNP STRUCTURE FOR MONOLITHIC INTEGRATED CIRCUITS

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

FAIRCHILD CAMERA AND INSTRUMENT CORPORATION (CONTINUED)

3623925 - SCHOTTKY-BARRIER DIODE PROCESS AND DEVICES
3648051 - PHOTOSENSOR CIRCUIT WITH INTEGRATED CURRENT DRIVE
3648125 - METHOD OF FABRICATING INTEGRATED CIRCUITS WITH OXIDIZED ISOLATION AND THE RESULTING STRUCTURE
3648127 - REACHTHROUGH OR PUNCHTHROUGH BREAKDOWN FOR GATE PROTECTION IN MOS DEVICES
3673471 - DOPED SEMICONDUCTOR ELECTRODES FOR MOS TYPE DEVICES
3677280 - OPTIMUM HIGH GAIN-BANDWIDTH PHOTOTRANSISTOR
3702427 - ELECTROMIGRATION RESISTANT METALLIZATION FOR INTEGRATED CIRCUITS, STRUCTURE AND PROCESS
3723258 - USE OF ANODIZED ALUMINUM AS ELECTRICAL INSULATION AND SCRATCH PROTECTION FOR SEMICONDUCTOR DEVICES
3736193 - SINGLE CRYSTAL-POLYCRYSTALLINE PROCESS FOR ELECTRICAL ISOLATION IN INTEGRATED CIRCUITS
3737347 - GRADED IMPURITY PROFILE IN EPITAXIAL FILMS TO IMPROVE INTEGRATED CIRCUIT PERFORMANCE
3761326 - PROCESS FOR MAKING AN OPTIMUM HIGH GAIN-BANDWIDTH PHOTOTRANSISTOR STRUCTURE
3806772 - CHARGE COUPLED AMPLIFIER
3838440 - MONOLITHIC MOS/BIPOLAR INTEGRATED CIRCUIT STRUCTURE
3873989 - DOUBLE-DIFFUSED, LATERAL TRANSISTOR STRUCTURE
3891977 - CHARGE COUPLED MEMORY DEVICE
3898482 - NOISE SUPPRESSION CIRCUIT
3898483 - BIPOLAR MEMORY CIRCUIT
3919005 - METHOD FOR FABRICATING DOUBLE-DIFFUSED, LATERAL TRANSISTOR
3920481 - PROCESS FOR FABRICATING INSULATED GATE FIELD EFFECT TRANSISTOR STRUCTURE
3945857 - METHOD FOR FABRICATING DOUBLE-DIFFUSED, LATERAL TRANSISTORS
3962717 - OXIDE ISOLATED INTEGRATED INJECTION LOGIC WITH SELECTIVE GUARD RING
3993513 - COMBINED METHOD FOR FABRICATING OXIDE-ISOLATED VERTICAL BIPOLAR TRANSISTORS AND COMPLEMENTARY OXIDE-ISOLATED LATERAL BIPOLAR TRANSISTORS AND THE RESULTING STRUCTURES
3999082 - CHARGE COUPLED AMPLIFIER
4003034 - SENSE AMPLIFIER CIRCUIT FOR A RANDOM ACCESS MEMORY
4021786 - MEMORY CELL CIRCUIT AND SEMICONDUCTOR STRUCTURE THEREFORE
4027380 - COMPLEMENTARY INSULATED GATE FIELD EFFECT TRANSISTOR STRUCTURE AND PROCESS FOR FABRICATING THE STRUCTURE
4032902 - AN IMPROVED SEMICONDUCTOR MEMORY CELL CIRCUIT AND STRUCTURE
4035784 - ASYMMETRICAL MEMORY CELL ARRANGEMENT
4047217 - HIGH-GAIN, HIGH-VOLTAGE TRANSISTOR FOR LINEAR INTEGRATED CIRCUITS
4056414 - PROCESS FOR PRODUCING AN IMPROVED DIELECTRICALLY-ISOLATED SILICON CRYSTAL UTILIZING ADJACENT AREAS OF DIFFERENT INSULATORS
4084174 - GRADUATED MULTIPLE COLLECTOR STRUCTURE FOR INVERTED VERTICAL BIPOLAR TRANSISTORS
4115797 - INTEGRATED INJECTION LOGIC WITH HEAVILY DOPED INJECTOR BASE SELF-ALIGNED WITH INJECTOR EMITTER AND COLLECTOR
4118728 - INTEGRATED CIRCUIT STRUCTURES UTILIZING CONDUCTIVE BURIED REGIONS
4141209 - CRYSTAL CONTROLLED OSCILLATOR AND METHOD OF TUNING SAME
4149177 - METHOD OF FABRICATING CONDUCTIVE BURIED REGIONS IN INTEGRATED CIRCUITS AND THE RESULTING STRUCTURES
4168999 - METHOD FOR FORMING OXIDE ISOLATED INTEGRATED INJECTION LOGIC SEMICONDUCTOR STRUCTURES HAVING MINIMAL ENCROACHMENT UTILIZING SPECIAL MASKING TECHNIQUES
4173766 - INSULATED GATE FIELD-EFFECT TRANSISTOR READ-ONLY MEMORY CELL

FERRANTI LIMITED

3781977 - SEMICONDUCTOR DEVICES
3818463 - SEMICONDUCTOR INFORMATION STORAGE DEVICES
3827034 - SEMICONDUCTOR INFORMATION STORAGE DEVICES
3886004 - METHOD OF MAKING SILICON SEMICONDUCTOR DEVICES UTILIZING ENHANCED THERMAL OXIDATION
3929526 - METHOD OF MAKING SEMI-CONDUCTOR DEVICES UTILIZING A COMPENSATING PREDIFFUSION
3945032 - SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE HAVING A CONDUCTIVE PLANE AND A DIFFUSED NETWORK OF CONDUCTIVE TRACKS
4053336 - METHOD OF MANUFACTURING A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE HAVING A CONDUCTIVE PLANE AND A DIFFUSED NETWORK OF CONDUCTIVE TRACKS
4069494 - INVERTER CIRCUIT ARRANGEMENTS
4134124 - SEMICONDUCTOR DEVICES AND CIRCUIT ARRANGEMENTS INCLUDING SUCH DEVICES
4145621 - TRANSISTOR LOGIC CIRCUITS
4160990 - SEMICONDUCTOR DEVICES AND CIRCUIT ARRANGEMENTS INCLUDING SUCH DEVICES
4161742 - SEMICONDUCTOR DEVICES WITH MATCHED RESISTOR PORTIONS

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

FERROSIL CORPORATION
4149301 - MONOLITHIC SEMICONDUCTOR INTEGRATED CIRCUIT-FERROELECTRIC MEMORY DRIVE
4149302 - MONOLITHIC SEMICONDUCTOR INTEGRATED CIRCUIT FERROELECTRIC MEMORY DEVICE

FUJITSU LIMITED
3484302 - METHOD OF GROWING SEMICONDUCTOR CRYSTALS
3578420 - METAL FILM RESISTOR
3726733 - METHOD OF MANUFACTURING THIN-FILM INTEGRATED CIRCUITS
3886003 - METHOD OF MAKING AN INTEGRATED CIRCUIT
4003071 - METHOD OF MANUFACTURING AN INSULATED GATE FIELD EFFECT TRANSISTOR
4015278 - FIELD EFFECT SEMICONDUCTOR DEVICE
4031608 - PROCESS FOR PRODUCING SEMICONDUCTOR MEMORY DEVICE UTILIZING SELECTIVE DIFFUSION OF THE POLYCRYSTALLINE SILICON ELECTRODE S
4062037 - SEMICONDUCTOR MEMORY DEVICE
4137108 - PROCESS FOR PRODUCING A SEMICONDUCTOR DEVICE BY VAPOR GROWTH OF SINGLE CRYSTAL AL+HD 2+B O+HD 3
4151542 - TRANSISTOR
4157561 - HIGH POWER TRANSISTOR

GENERAL ELECTRIC COMPANY
3421026 - MEMORY FLIP-FLOP
3434023 - SEMICONDUCTOR SWITCHING DEVICES WITH A TUNNEL JUNCTION DIODE IN SERIES WITH THE GATE ELECTRODE
3462657 - PROTECTION MEANS FOR SURFACE SEMICONDUCTOR DEVICES HAVING THIN OXIDE FILMS THEREIN
3463970 - INTEGRATED SEMICONDUCTOR RECTIFIER ASSEMBLY
3486029 - RADIATIVE INTERCONNECTION ARRANGEMENT
3500428 - MICROWAVE HYBRID MICROELECTRONIC CIRCUIT MODULE
3509446 - FULL-WAVE RECTIFYING MONOLITHIC INTEGRATED CIRCUIT
3529350 - THIN FILM RESISTOR-CONDUCTOR SYSTEM EMPLOYING ALPHA- TUNGSTEN RESISTOR FILMS
3533022 - MAGNETICALLY DRIVEN ELECTROMECHANICAL FILTER WITH CANTILEVERED RESONATOR AND VARIABLE Q
3541357 - INTEGRATED CIRCUIT FOR ALTERNATING CURRENT OPERATION
3566457 - BURIED METALLIC FILM DEVICES AND METHOD OF MAKING THE SAME
3566518 - METHOD FOR FABRICATING FIELD-EFFECT TRANSISTOR DEVICES AND INTEGRATED CIRCUIT MODULES CONTAINING THE SAME BY SELECTIVE D IFFUSION OF ACTIVATOR IMPURTIES THROUGH PRESELECTED PORTIONS OF PASSIVATING-INSULATING FILMS
3573568 - LIGHT EMITTING SEMICONDUCTOR CHIPS MOUNTED IN A SLOTTED SUBSTRATE FORMING A DISPLAY APPARATUS
3608189 - METHOD OF MAKING COMPLEMENTARY FIELD-EFFECT TRANSISTORS BY SINGLE STEP DIFFUSION
3611066 - THYRISTOR WITH INTEGRATED BALLASTED GATE AUXILIARY THYRISTOR PORTION
3611070 - VOLTAGE-VARIABLE CAPACITOR WITH CONTROLLABLY EXTENDIBLE P-N JUNCTION REGION
3614829 - METHOD OF FORMING HIGH STABILITY, SELF- REGISTERED FIELD EFFECT TRANSISTORS
3634150 - METHOD FOR FORMING EPITAXIAL CRYSTALS OR WAFERS IN SELECTED REGIONS OF SUBSTRATES
3641405 - FIELD-EFFECT TRANSISTORS WITH SUPERIOR PASSIVATING FILMS AND METHOD OF MAKING SAME
3646665 - COMPLEMENTARY MIS-FET DEVICES AND METHOD OF FABRICATION
3653120 - METHOD OF MAKING LOW RESISTANCE POLYCRYSTALLINE SILICON CONTACTS TO BURIED COLLECTOR REGIONS USING REFRACTORY METAL SILI CIDES
3654527 - UNITARY FULL WAVE INVERTER
3662356 - INTEGRATED CIRCUIT BISTABLE MEMORY CELL USING CHARGE-PUMPED DEVICES
3679941 - COMPOSITE INTEGRATED CIRCUITS INCLUDING SEMICONDUCTOR CHIPS MOUNTED ON A COMMON SUBSTRATE WITH CONNECTIONS MADE THROUGH A DIELECTRIC ENCAPSULATOR
3689900 - PHOTO-CODED DIODE ARRAY FOR READ ONLY MEMORY
3693003 - STORAGE TARGET FOR AN ELECTRON-BEAM ADDRESSED READ, WRITE AND ERASE MEMORY
3699402 - HYBRID CIRCUIT POWER MODULE
3701980 - HIGH DENSITY FOUR-TRANSISTOR MOS CONTENT ADDRESSED MEMORY
3703456 - METHOD OF MAKING RESISTOR THIN FILMS BY REACTIVE SPUTTERING FROM A COMPOSITE SOURCE
3715245 - SELECTIVE LIQUID PHASE EPITAXIAL GROWTH PROCESS
3716759 - ELECTRONIC DEVICE WITH THERMALLY CONDUCTIVE DIELECTRIC BARRIER
3743897 - HYBRID CIRCUIT ARRANGEMENT WITH METAL OXIDE VARISTOR SHUNT
3750115 - READ MOSTLY ASSOCIATIVE MEMORY CELL FOR UNIVERSAL LOGIC
3754169 - RECTIFIER BRIDGE

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

GENERAL ELECTRIC COMPANY (CONTINUED)

3781827 - DEVICE FOR STORING INFORMATION AND PROVIDING AN ELECTRIC READOUT
3784847 - DIELECTRIC STRIP ISOLATION FOR JFET OR MESFET DEPLETION-MODE BUCKET-BRIGADE CIRCUIT
3790825 - GATE-DIFFUSION ISOLATION FOR JFET DEPLETION-MODE BUCKET BRIGADE CIRCUIT
3801883 - SURFACE CHARGE SIGNAL CORRELATOR
3806771 - SMOOTHLY BEVELED SEMICONDUCTOR DEVICE WITH THICK GLASS PASSIVANT
3812518 - PHOTODIODE WITH PATTERNED STRUCTURE
3821616 - MONOLITHIC SEMICONDUCTOR DISPLAY DEVICES
3882531 - APPARATUS FOR SENSING RADIATION AND PROVIDING ELECTRICAL READ OUT
3896480 - SEMICONDUCTOR DEVICE WITH HOUSING OF VARISTOR MATERIAL
3904442 - METHOD OF MAKING ISOLATION GRIDS IN BODIES OF SEMICONDUCTOR MATERIAL
3905036 - FIELD EFFECT TRANSISTOR DEVICES AND METHODS OF MAKING SAME
3906541 - FIELD EFFECT TRANSISTOR DEVICES AND METHODS OF MAKING SAME
3916268 - DEVICE FOR STORING INFORMATION AND PROVIDING AN ELECTRIC READOUT FROM A CONDUCTOR-INSULATOR-SEMICONDUCTOR STRUCTURE
3955187 - PROPORTIONING THE ADDRESS AND DATA SIGNALS IN A R.M.S. RESPONSIVE DISPLAY DEVICE MATRIX TO OBTAIN ZERO CROSS-TALK AND MA XIMUM CONTRAST
3979230 - METHOD OF MAKING ISOLATION GRIDS IN BODIES OF SEMICONDUCTOR MATERIAL
3979820 - DEEP DIODE LEAD THROUGHS
3982268 - DEEP DIODE LEAD THROUGHS
3982269 - SEMICONDUCTOR DEVICES AND METHOD, INCLUDING TGZM, OF MAKING SAME
3988762 - MINORITY CARRIER ISOLATION BARRIERS FOR SEMICONDUCTOR DEVICES
3988763 - ISOLATION JUNCTIONS FOR SEMICONDUCTORS DEVICES
3988764 - DEEP DIODE SOLID STATE INDUCTOR COIL
3988766 - MULTIPLE P-N JUNCTION FORMATION WITH AN ALLOY DROPLET
3988772 - CURRENT ISOLATION MEANS FOR INTEGRATED POWER DEVICES
3995309 - ISOLATION JUNCTIONS FOR SEMICONDUCTOR DEVICES
4006040 - SEMICONDUCTOR DEVICE MANUFACTURE
4024562 - RADIATION SENSING AND CHARGE STORAGE DEVICES
4024565 - DEEP DIODE SOLID STATE TRANSFORMER
4024566 - DEEP DIODE DEVICE
4031416 - SEMICONDUCTOR AMPLIFICATION MEANS COMBINING TWO CASCADED TRANSISTOR AMPLIFIERS OF HIGH INVERSE IMPEDANCES
4032960 - ANISOTROPIC RESISTOR FOR ELECTRICAL FEED THROUGHS
4032961 - GATE MODULATED BIPOLAR TRANSISTOR
4042448 - POST TGZM SURFACE ETCH
4047220 - BIPOLAR TRANSISTOR STRUCTURE HAVING LOW SATURATION RESISTANCE
4053922 - LIGHT TRIGGERED THYRISTOR HAVING CONTROLLED TURN ON DELAY
4060821 - FIELD CONTROLLED THYRISTOR WITH BURIED GRID
4063272 - SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE THEREOF
4063966 - METHOD FOR FORMING SPACED ELECTRICALLY ISOLATED REGIONS IN A BODY OF SEMICONDUCTOR MATERIAL
4071378 - PROCESS OF MAKING A DEEP DIODE SOLID STATE TRANSFORMER
4082572 - PROCESS FOR MAKING ANISOTROPIC RESISTOR FOR ELECTRICAL FEED THROUGHS
4096430 - METAL-OXIDE-SEMICONDUCTOR VOLTAGE REFERENCE
4129879 - VERTICAL FIELD EFFECT TRANSISTOR
4157564 - DEEP DIODE DEVICES
4163244 - SYMMETRICAL INTEGRATED INJECTION LOGIC CIRCUIT
4178519 - INPUT CIRCUIT FOR CHARGE TRANSFER APPARATUS

GENERAL ELECTRIC INFORMATION SYSTEMS S.P.A.

3555365 - INTEGRATED CIRCUIT MATRIX HAVING PARALLEL CIRCUIT STRIPS
3590378 - FAULT-DETECTING MONITOR FOR INTEGRATED CIRCIUT UNITS

GENERAL INSTRUMENT CORPORATION

3656119 - MEMORY UTILIZING THE NON-LINEAR INPUT CAPACITANCE OF AN MOS DEVICE
3736521 - MOS AMPLIFIER UTILIZING PARASITIC CONDUCTION STATE OPERATION
3766448 - INTEGRATED IGFET CIRCUITS WITH INCREASED INVERSION VOLTAGE UNDER METALLIZATION RUNS
3812520 - PARASITIC TRANSISTOR SHIFT REGISTER

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

GENERAL INSTRUMENT CORPORATION (CONTINUED)
3855008 - MOS INTEGRATED CIRCUIT PROCESS
3868274 - METHOD FOR FABRICATING MOS DEVICES WITH A MULTIPLICITY OF THRESHOLDS ON A SEMICONDUCTOR SUBSTRATE
3893087 - RANDOM ACCESS MEMORY WITH SHARED COLUMN CONDUCTORS

GENERAL MOTORS CORPORATION
3469148 - PROTECTIVELY COVERED HYBRID MICROCIRCUITS
3624454 - MESA-TYPE SEMICONDUCTOR DEVICE
3689357 - GLASS-POLYSILICON DIELECTRIC ISOLATION
3755722 - RESISTOR ISOLATION FOR DOUBLE MESA TRANSISTORS
3764507 - METHOD OF MAKING SEMICONDUCTOR LAYERS ON HIGH PURITY ALUMINA LAYERS
3792525 - METHOD OF MAKING A SEMICONDUCTIVE SIGNAL TRANSLATING DEVICE
3814994 - FOUR TERMINAL POWER TRANSISTOR
3821780 - DOUBLE MESA TRANSISTOR WITH INTEGRAL BLEEDER RESISTORS
3860448 - METHOD OF APPLYING SILICONE PASSIVANTS TO ETCH MOATS IN MESA DEVICE WAFERS
4003127 - POLYCRYSTALLINE SILICON PRESSURE TRANSDUCER
4133000 - INTEGRATED CIRCUIT PROCESS COMPATIBLE SURGE PROTECTION RESISTOR
4133701 - SELECTIVE ENHANCEMENT OF PHOSPHORUS DIFFUSION BY IMPLANTING HALOGEN IONS
4144100 - METHOD OF LOW DOSE PHOSHORUS IMPLANTATION FOR OXIDE PASSIVATED DIODES IN +21 100+22 +0 P-TYPE SILICON

GTE LABORATORIES INCORPORATED
3493824 - INSULATED-GATE FIELD EFFECT TRANSISTORS UTILIZING A HIGH RESISTIVITY SUBSTRATE
3500138 - BIPOLAR MOS FIELD EFFECT TRANSISTOR
3585463 - COMPLEMENTARY ENHANCEMENT TYPE MOS TRANSISTORS
3699409 - SOLID STATE DEVICE HAVING DIELECTRIC AND SEMICONDUCTOR FILMS SANDWICHED BETWEEN ELECTRODES
3819867 - MATRIX EMPLOYING SEMICONDUCTOR SWITCHING CIRCUIT
3872495 - NEGATIVE IMPEDANCE CONVERTER
3913125 - NEGATIVE IMPEDANCE CONVERTER

GTE SYLVANIA INCORPORATED
3421206 - METHOD OF FORMING LEADS ON SEMICONDUCTOR DEVICES
3421985 - METHOD OF PRODUCING SEMICONDUCTOR DEVICES HAVING CONNECTING LEADS ATTACHED THERETO
3450959 - FOUR-LAYER SEMICONDUCTOR SWITCHING DEVICES IN INTEGRATED CIRCUITRY
3456334 - METHOD OF PRODUCING AN ARRAY OF SEMICONDUCTOR ELEMENTS
3518135 - METHOD FOR PRODUCING PATTERNS OF CONDUCTIVE LEADS
3621562 - METHOD OF MANUFACTURING INTEGRATED CIRCUIT ARRAYS
3638079 - COMPLEMENTARY SEMICONDUCTOR DEVICES IN MONOLITHIC INTEGRATED CIRCUITS
3639786 - VIDEO SIGNALLING PROCESSING APPARATUS

HANS LIST
3564442 - INTEGRATED FIELD-EFFECT DISTRIBUTED AMPLIFIER

HARRIS CORPORATION
3766447 - HETEROEPITAXIAL STRUCTURE
3779841 - FABRICATION OF THIN FILM RESISTOR CROSSOVERS FOR INTEGRATED CIRCUITS
3783349 - FIELD EFFECT TRANSISTOR
3865649 - FABRICATION OF MOS DEVICES AND COMPLEMENTARY BIPOLAR TRANSISTOR DEVICES IN A MONOLITHIC SUBSTRATE
3886587 - ISOLATED PHOTODIODE ARRAY
3935040 - PROCESS FOR FORMING MONOLITHIC SEMICONDUCTOR DISPLAY
3953255 - FABRICATION OF MATCHED COMPLEMENTARY TRANSISTORS IN INTEGRATED CIRCUITS
3956034 - ISOLATED PHOTODIODE ARRAY
3974517 - METALLIC GROUND GRID FOR INTEGRATED CIRCUITS
3975752 - JUNCTION FIELD EFFECT TRANSISTOR
3979237 - DEVICE ISOLATION IN INTEGRATED CIRCUITS
3984857 - HETEROEPITAXIAL DISPLAYS
4045259 - PROCESS FOR FABRICATING DIFFUSED COMPLEMENTARY FIELD EFFECT TRANSISTORS

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

HARRIS CORPORATION (CONTINUED)

4067038 - SUBSTRATE FED LOGIC AND METHOD OF FABRICATION
4120707 - PROCESS OF FABRICATING JUNCTION ISOLATED IGFET AND BIPOLAR TRANSISTOR INTEGRATED CIRCUIT BY DIFFUSION
4124863 - POSITIVELY BIASED SUBSTRATE IC WITH THERMAL OXIDE GUARD RING
4135955 - PROCESS FOR FABRICATING HIGH VOLTAGE CMOS WITH SELF-ALIGNED GUARD RINGS UTILIZING SELECTIVE DIFFUSION AND LOCAL OXIDATION
4140559 - METHOD OF FABRICATING AN IMPROVED SUBSTRATE FED LOGIC UTILIZING GRADED EPITAXIAL DEPOSITION
4174521 - PROM ELECTRICALLY WRITTEN BY SOLID PHASE EPITAXY

HAYAKAWA DENKI KOGYO KABUSHIKI KAISHA
3569729 - INTEGRATED FET STRUCTURE WITH SUBSTRATE BIASING MEANS TO EFFECT BIDIRECTIONAL TRANSISTOR OPERATION

HEWLETT-PACKARD COMPANY
3423823 - METHOD FOR MAKING THIN DIAPHRAGMS
3590342 - MOS INTEGRATED CIRCUIT WITH REGIONS OF GROUND POTENTIAL INTERCONNECTED THROUGH THE SUBSTRATE
3836793 - PHOTON ISOLATOR WITH IMPROVED PHOTODETECTOR TRANSISTOR STAGE
3925801 - PHOTON ISOLATOR WITH IMPROVED PHOTODETECTOR TRANSISTOR STAGE
3975648 - FLAT-BAND VOLTAGE REFERENCE
4068134 - BARRIER HEIGHT VOLTAGE REFERENCE
4097890 - LOW PARASITIC CAPACITANCE AND RESISTANCE BEAMLEAD SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURE
4163243 - ONE-TRANSISTOR MEMORY CELL WITH ENHANCED CAPACITANCE

HITACHI, LTD.
3423821 - METHOD OF PRODUCING THIN FILM INTEGRATED CIRCUITS
3430334 - METHOD OF MANUFACTURING INTEGRATED CIRCUITS
3449643 - SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE
3449682 - INTEGRATED-CASCADE AMPLIFIER WITH IMPROVED FREQUENCY CHARACTERISTIC
3458703 - REVERSE BIASED SEMICONDUCTOR LASER LIGHT MODULATOR FABRICATED FROM SAME MATERIAL AS LASER LIGHT SOURCE
3477031 - DIFFERENTIAL AMPLIFIER CIRCUIT EMPLOYING MULTIPLE DIFFERENTIAL AMPLIFIER STAGES
3500140 - MULTI-CHANNEL INTEGRATED DEVICES CONSISTING OF DARLINGTON CIRCUITS
3507716 - METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE
3531857 - METHOD OF MANUFACTURING SUBSTRATE FOR SEMICONDUCTOR INTEGRATED CIRCUIT
3546615 - FIELD EFFECT
3555374 - FIELD PROTECTIVE DIODE
3560750 - OPTOELECTRONIC AMPLIFIER
3562560 - TRANSISTOR-TRANSISTOR LOGIC
3564443 - SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE CONTAINING LATERAL AND PLANAR TRANSISTORS IN A SEMICONDUCTOR LAYER
3566214 - INTEGRATED CIRCUIT HAVING A PLURALITY OF CIRCUIT ELEMENT REGIONS AND CONDUCTING LAYERS EXTENDING ON BOTH OF THE OPPOSED COMMON MAJOR SURFACES OF SAID CIRCUIT ELEMENT REGIONS
3581166 - GOLD-ALUMINUM LEAD-OUT STRUCTURE OF A SEMICONDUCTOR DEVICE
3584218 - INFRARED SPECTROMETER USING INTEGRATED MOS STRUCTURE
3590340 - BREAKDOWN PREVENTING CIRCUIT AND AN INTEGRATED DEVICE THEREOF FOR A SEMICONDUCTOR DEVICE HAVING AN INSULATE GATE ELECTRODE
3596149 - SEMICONDUCTOR INTEGRATED CIRCUIT WITH REDUCED MINORITY CARRIER STORAGE EFFECT
3615932 - METHOD OF FABRICATING A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE
3636372 - SEMICONDUCTOR SWITCHING CIRCUITS AND INTEGRATED DEVICES THEREOF
3645808 - METHOD FOR FABRICATING A SEMICONDUCTOR INTEGRATED CIRCUIT
3652347 - METHOD FOR MANUFACTURING A SEMICONDUCTOR DEVICE
3699011 - METHOD OF PRODUCING THIN FILM INTEGRATED CIRCUITS
3700981 - SEMICONDUCTOR INTEGRATED CIRCUIT COMPOSED OF CASCADE CONNECTION OF INVERTER CIRCUITS
3707036 - METHOD FOR FABRICATING SEMICONDUCTOR LSI CIRCUIT DEVICES
3718780 - ACTIVE PULSE TRANSMISSION CIRCUIT FOR AN INTEGRATED CIRCUIT
3719864 - SEMICONDUCTOR DEVICE WITH TWO MOS TRANSISTORS OF NON-SYMMETRICAL TYPE
3725145 - METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICES
3735481 - METHOD OF MANUFACTURING AN INTEGRATED CIRCUIT HAVING A TRANSISTOR ISOLATED BY THE COLLECTOR REGION
3736192 - INTEGRATED CIRCUIT AND METHOD OF MAKING THE SAME

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

HITACHI, LTD. (CONTINUED)

3742598 - METHOD FOR FABRICATING A DISPLAY DEVICE AND THE DEVICE FABRICATED THEREBY
3745424 - SEMICONDUCTOR PHOTOELECTRIC TRANSDUCER
3753803 - METHOD OF DIVIDING SEMICONDUCTOR LAYER INTO A PLURALITY OF ISOLATED REGIONS
3754171 - INSULATED GATE TYPE FIELD EFFECT SEMICONDUCTOR DEVICE HAVING A BREAKDOWN PREVENTING ELEMENT
3761786 - SEMICONDUCTOR DEVICE HAVING RESISTORS CONSTITUTED BY AN EPITAXIAL LAYER
3763379 - SEMICONDUCTOR DEVICE FOR SCANNING DIGITAL SIGNALS
3764409 - METHOD FOR FABRICATING A SEMICONDUCTOR COMPONENT FOR A SEMICONDUCTOR CIRCUIT
3767483 - METHOD OF MAKING SEMICONDUCTOR DEVICES
3767486 - DOUBLE EPITAXIAL METHOD FOR FABRICATING COMPLEMENTARY INTEGRATED CIRCUIT
3771026 - CONDUCTIVE REGION FOR SEMICONDUCTOR DEVICE AND METHOD FOR MAKING THE SAME
3773566 - METHOD FOR FABRICATING SEMICONDUCTOR DEVICE HAVING SEMICONDUCTOR CIRCUIT ELEMENT IN ISOLATED SEMICONDUCTOR REGION
3775623 - SEMICONDUCTOR DEVICE FOR SCANNING DIGITAL SIGNALS
3780426 - METHOD OF FORMING A SEMICONDUCTOR CIRCUIT ELEMENT IN AN ISOLATED EPITAXIAL LAYER
3785043 - METHOD OF PRODUCING SEMICONDUCTOR DEVICES
3786318 - SEMICONDUCTOR DEVICE HAVING CHANNEL PREVENTING STRUCTURE
3788905 - SEMICONDUCTOR DEVICE AND METHOD OF PRODUCING THE SAME
3789503 - INSULATED GATE TYPE FIELD EFFECT DEVICE AND METHOD OF MAKING THE SAME
3791882 - METHOD OF MANUFACTURING SEMICONDUCTOR DEVICES UTILIZING SIMULTANEOUS DEPOSITION OF MONOCRYSTALLINE AND POLYCRYSTALLINE R EGIONS
3795846 - INTEGRATED SEMICONDUCTOR DEVICE HAVING FUNCTIONAL REGIONS ISOLATED BY P-N JUNCTION THEREBETWEEN
3798513 - SEMICONDUCTOR DEVICE HAVING A SURFACE PARALLEL TO THE [100] PLANE AND A CHANNEL STOPPER PARALLEL TO THE [111] PLANE
3801880 - MULTILAYER INTERCONNECTED STRUCTURE FOR SEMICONDUCTOR INTEGRATED CIRCUIT AND PROCESS FOR MANUFACTURING THE SAME
3801886 - VARIABLE RESISTANCE ELEMENT
3829888 - SEMICONDUCTOR DEVICE AND THE METHOD OF MAKING THE SAME
3846167 - METHOD OF MANUFACTURING SEMICONDUCTOR DEVICES
3847677 - METHOD OF MANUFACTURING SEMICONDUCTOR DEVICES
3858233 - LIGHT-RECEIVING SEMICONDUCTOR DEVICE
3891469 - METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE
3893155 - COMPLEMENTARY MIS INTEGRATED CIRCUIT DEVICE ON INSULATING SUBSTRATE
3909636 - SEMICONDUCTOR LARGE SCALE INTEGRATED CIRCUIT CHIP HAVING CURRENT SWITCHING TYPE LOGICAL CIRCUITS
3913123 - BIPOLAR TYPE SEMICONDUCTOR INTEGRATED CIRCUIT
3914783 - MULTI-LAYER SEMICONDUCTOR DEVICE
3919008 - METHOD OF MANUFACTURING MOS TYPE SEMICONDUCTOR DEVICES
3920484 - METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE
3925120 - A METHOD FOR MANUFACTURING A SEMICONDUCTOR DEVICE HAVING A BURIED EPITAXIAL LAYER
3928091 - METHOD FOR MANUFACTURING A SEMICONDUCTOR DEVICE UTILIZING SELECTIVE OXIDATION
3933540 - METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE
3934159 - SEMICONDUCTOR CIRCUIT DEVICES USING INSULATED GATE-TYPE FIELD EFFECT ELEMENTS HAVING PROTECTIVE DIODES
3936676 - MULTI-LEVEL VOLTAGE SUPPLY CIRCUIT FOR LIQUID CRYSTAL DISPLAY DEVICE
3946425 - MULTI-EMITTER TRANSISTOR HAVING HEAVILY DOPED N+ REGIONS SURROUNDING BASE REGION OF TRANSISTORS
3947864 - DIODE-INTEGRATED THYRISTOR
3959812 - HIGH-VOLTAGE SEMICONDUCTOR INTEGRATED CIRCUIT
3961357 - SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE
3962718 - CAPACITANCE CIRCUIT
3967309 - SEMICONDUCTOR DEVICE WITH A SEMICONDUCTOR SUBSTRATE HAVING DIELECTRICALLY ISOLATED FUNCTIONAL REGIONS
3967310 - SEMICONDUCTOR DEVICE HAVING CONTROLLED SURFACE CHARGES BY PASSIVATION FILMS FORMED THEREON
3967364 - METHOD OF MANUFACTURING SEMICONDUCTOR DEVICES
3969748 - INTEGRATED MULTIPLE TRANSISTORS WITH DIFFERENT CURRENT GAINS
3978514 - DIODE-INTEGRATED HIGH SPEED THYRISTOR
3983619 - LARGE SCALE INTEGRATED CIRCUIT ARRAY OF UNIT CELLS AND METHOD OF MANUFACTURING SAME
3990092 - RESISTANCE ELEMENT FOR SEMICONDUCTOR INTEGRATED CIRCUIT
3990102 - SEMICONDUCTOR INTEGRATED CIRCUITS AND METHOD OF MANUFACTURING THE SAME
3992232 - METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE HAVING OXIDE ISOLATION STRUCTURE AND GUARD RING
3994011 - HIGH WITHSTAND VOLTAGE-SEMICONDUCTOR DEVICE WITH SHALLOW GROOVES BETWEEN SEMICONDUCTOR REGION AND FIELD LIMITING RINGS
3997378 - METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE UTILIZING MONOCRYSTALLINE-POLYCRYSTALLINE GROWTH

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

HITACHI, LTD. (CONTINUED)

3999212 - FIELD EFFECT SEMICONDUCTOR DEVICE HAVING A PROTECTIVE DIODE
4008107 - METHOD OF MANUFACTURING SEMICONDUCTOR DEVICES WITH LOCAL OXIDATION OF SILICON SURFACE
4009484 - INTEGRATED CIRCUIT ISOLATION USING GOLD-DOPED POLYSILICON
4011581 - MOSFET ANTIPARASITIC LAYER
4012764 - SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE
4014718 - METHOD OF MAKING INTEGRATED CIRCUITS FREE FROM THE FORMATION OF A PARASITIC PNPN THYRISTOR
4015216 - FREQUENCY-VOLTAGE CONVERTER AND A STABILIZED PULSE GENERATOR USING IT
4015281 - MIS-FETS ISOLATED ON COMMON SUBSTRATE
4016007 - METHOD FOR FABRICATING A SILICON DEVICE UTILIZING ION-IMPLANTATION AND SELECTIVE OXIDATION
4017341 - METHOD OF MANUFACTURING SEMICONDUCTOR INTEGRATED CIRCUIT WITH PREVENTION OF SUBSTRATE WARPAGE
4021687 - TRANSISTOR CIRCUIT FOR DEEP SATURATION PREVENTION
4024568 - TRANSISTOR WITH BASE/EMITTER ENCIRCLEMENT CONFIGURATION
4025941 - HALL ELEMENT
4032952 - BULK CHARGE TRANSFER SEMICONDUCTOR DEVICE
4039359 - METHOD OF MANUFACTURING A FLATTENED SEMICONDUCTOR DEVICE
4041518 - MIS SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME
4042726 - SELECTIVE OXIDATION METHOD
4044340 - SEMICONDUCTOR MEMORY
4044373 - IGFET WITH GATE PROTECTION DIODE AND ANTIPARASITIC ISOLATION MEANS
4045249 - OXIDE FILM ISOLATION PROCESS
4049476 - METHOD OF MANUFACTURING A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE WHICH INCLUDES AT LEAST ONE V-GROOVE JFET AND ONE BIPO LAR TRANSISTOR
4051389 - FLIP-FLOP CIRCUIT
4051506 - COMPLEMENTARY SEMICONDUCTOR DEVICE
4056413 - ETCHING METHOD FOR FLATTENING A SILICON SUBSTRATE UTILIZING AN ANISOTROPIC ALKALI ETCHANT
4060827 - SEMICONDUCTOR DEVICE AND A METHOD OF MAKING THE SAME
4070654 - BIPOLAR READ-ONLY MEMORY
4073054 - METHOD OF FABRICATING SEMICONDUCTOR DEVICE
4079506 - METHOD OF PREPARING A DIELECTRIC-ISOLATED SUBSTRATE FOR SEMICONDUCTOR INTEGRATED CIRCUITRIES
4080616 - ELECTROSTATIC PUNCTURE PREVENTING ELEMENT
4086662 - MEMORY SYSTEM WITH READ/WRITE CONTROL LINES
4089021 - SEMICONDUCTOR DEVICE CAPABLE OF WITHSTANDING HIGH VOLTAGE AND METHOD OF MANUFACTURING SAME
4089022 - ELECTRON DEVICE
4089024 - SEMICONDUCTOR SWITCHING DEVICE
4100564 - POWER TRANSISTOR DEVICE
4111724 - METHOD OF MANUFACTURING OXIDE ISOLATED SEMICONDUCTOR DEVICE UTILIZING SELECTIVE ETCHING TECHNIQUE
4114178 - SEMICONDUCTOR CONTROLLED RECTIFIER HAVING AN AUXILIARY REGION WITH LOCALIZED LOW RESISTANCE PATHS TO THE CONTROL GATE
4118794 - MEMORY ARRAY WITH LARGER MEMORY CAPACITORS AT ROW ENDS
4122479 - OPTOELECTRONIC DEVICE HAVING CONTROL CIRCUIT FOR LIGHT EMITTING ELEMENT AND CIRCUIT FOR LIGHT RECEIVING ELEMENT INTEGRAT ED IN A SEMICONDUCTOR BODY
4122481 - SEMICONDUCTOR IC STRUCTURE INCLUDING ISOLATED DEVICES IN A SINGLE SUBSTRATE AND METHOD FOR FABRICATING SAME
4136356 - WIRING SUBSTRATE FOR A MATRIX CIRCUIT
4145701 - SEMICONDUCTOR DEVICE
4146906 - LOW FORWARD VOLTAGE DROP SEMICONDUCTOR DEVICE HAVING POLYCRYSTALLINE LAYERS OF DIFFERENT RESISTIVITY
4148048 -
4152716 - VOLTAGE DIVIDING CIRCUIT IN IC STRUCTURE
4167018 - MIS CAPACITANCE ELEMENT
4172260 - INSULATED GATE FIELD EFFECT TRANSISTOR WITH SOURCE FIELD SHIELD EXTENDING OVER MULTIPLE REGION CHANNEL

HOFFMANN-LA ROCHE INC.

3818426 - ULTRASONIC IMAGE RECORDING SYSTEM

HONEYWELL INC.

3453507 - PHOTO-DETECTOR
3475735 - SEMICONDUCTOR MEMORY

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

HONEYWELL INC. (CONTINUED)

3494809 - SEMICONDUCTOR PROCESSING
3509375 - SWITCHING CIRCUITRY FOR ISOLATING AN INPUT AND OUTPUT CIRCUIT UTILIZING A PLURALITY OF INSULATED GATE MAGNETIC OXIDE FIELD EFFECT TRANSISTORS
3596114 - HALL EFFECT CONTACTLESS SWITCH WITH PRE-BIASED SCHMITT TRIGGER
3702025 - DISCRETIONARY INTERCONNECTION PROCESS
3849678 - DETECTOR ARRAY
3850707 - SEMICONDUCTORS
3860836 - STABILIZATION OF EMITTER FOLLOWERS
3891480 - BIPOLAR SEMICONDUCTOR DEVICE CONSTRUCTION
3970866 - LOGIC GATE CIRCUITS
4033787 - FABRICATION OF SEMICONDUCTOR DEVICES UTILIZING ION IMPLANTATION
4034395 - MONOLITHIC INTEGRATED CIRCUIT HAVING A PLURALITY OF RESISTOR REGIONS ELECTRICALLY CONNECTED IN SERIES
4044371 - PLURALITY OF PRECISE TEMPERATURE RESISTORS FORMED IN MONOLITHIC INTEGRATED CIRCUITS
4092662 - SENSISTOR APPARATUS
4119997 - DOT-AND LOGIC GATE DEVICE INCLUDING MULTIEMITTER TRANSISTOR
4139781 - LOGIC GATE CIRCUITS
4148046 -
4148047 -
4152714 - SEMICONDUCTOR APPARATUS
4165470 - LOGIC GATES WITH FORWARD BIASED DIODE LOAD IMPEDENCES

HONEYWELL INFORMATION SYSTEMS ITALIA
3787252 - CONNECTION MEANS FOR SEMICONDUCTOR COMPONENTS AND INTEGRATED CIRCUITS

HUGHES AIRCRAFT COMPANY
3421092 - MULTIRANK MULTISTAGE SHIFT REGISTER
3533158 - METHOD OF UTILIZING AN ION BEAM TO FORM CUSTOM CIRCUITS
3748187 - SELF-REGISTERED DOPED LAYER FOR PREVENTING FIELD INVERSION IN MISCIRCUITS
3824003 - LIQUID CRYSTAL DISPLAY PANEL
3862360 - LIQUID CRYSTAL DISPLAY SYSTEM WITH INTEGRATED SIGNAL STORAGE CIRCUITRY
4024626 - METHOD OF MAKING INTEGRATED TRANSISTOR MATRIX FOR FLAT PANEL LIQUID CRYSTAL DISPLAY
4028147 - LIQUID PHASE EPITAXIAL PROCESS FOR GROWING SEMI-INSULATING GAAS LAYERS
4032950 - LIQUID PHASE EPITAXIAL PROCESS FOR GROWING SEMI-INSULATING GAAS LAYERS
4033797 - METHOD OF MANUFACTURING A COMPLEMENTARY METAL-INSULATION-SEMICONDUCTOR CIRCUIT
4072976 - GATE PROTECTION DEVICE FOR MOS CIRCUITS
4101349 - INTEGRATED INJECTION LOGIC STRUCTURE FABRICATED BY OUTDIFFUSION AND EPITAXIAL DEPOSITION
4103297 - LIGHT-INSENSITIVE MATRIX ADDRESSED LIQUID CRYSTAL DISPLAY SYSTEM
4144098 - P+HU +3O +O +B BURIED LAYER FOR I+HU 2+B L ISOLATION BY ION IMPLANTATION
4173767 - CMOS MONOLITHIC INTEGRATED CIRCUIT

HUGLE, FRANCES, TRUSTEE OF -
3481801 - ISOLATION TECHNIQUE FOR INTEGRATED CIRCUITS
3574007 - METHOD OF MANUFACTURING IMPROVED MIS TRANSISTOR ARRAYS

INSELEK INC.
3846194 - PROCESS FOR PRODUCING LIGHTLY DOPED P AND N-TYPE REGIONS OF SILICON ON AN INSULATING SUBSTRATE

INTEL CORPORATION
3631313 - RESISTOR FOR INTEGRATED CIRCUIT
3728695 - RANDOM-ACCESS FLOATING GATE MOS MEMORY ARRAY
3744036 - ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY ARRAY
3755721 - FLOATING GATE SOLID STATE STORAGE DEVICE AND METHOD FOR CHARGING AND DISCHARGING SAME
3825946 - ELECTRICALLY ALTERABLE FLOATING GATE DEVICE AND METHOD FOR ALTERING SAME
3891190 - INTEGRATED CIRCUIT STRUCTURE AND METHOD FOR MAKING INTEGRATED CIRCUIT STRUCTURE
3936813 - BIPOLAR MEMORY CELL EMPLOYING INVERTED TRANSISTORS AND PINCHED BASE RESISTORS

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

INTEL CORPORATION (CONTINUED)
3975671 - CAPACITIVE VOLTAGE CONVERTER EMPLOYING CMOS SWITCHES
3986903 - MOSFET TRANSISTOR AND METHOD OF FABRICATION
3997381 - METHOD OF MANUFACTURE OF AN EPITAXIAL SEMICONDUCTOR LAYER ON AN INSULATING SUBSTRATE
4002931 - INTEGRATED CIRCUIT BIPOLAR BOOTSTRAP DRIVER
4007452 - WAFER SCALE INTEGRATION SYSTEM
4012757 - CONTACTLESS RANDOM-ACCESS MEMORY CELL AND CELL PAIR
4013484 - HIGH DENSITY CMOS PROCESS
4013489 - PROCESS FOR FORMING A LOW RESISTANCE INTERCONNECT IN MOS N-CHANNEL SILICON GATE INTEGRATED CIRCUIT
4033026 - HIGH DENSITY/HIGH SPEED MOS PROCESS AND DEVICE
4052229 - PROCESS FOR PREPARING A SUBSTRATE FOR MOS DEVICES OF DIFFERENT THRESHOLDS
4092619 - MOS VOLTAGE CONTROLLED LOWPASS FILTER
4099196 - TRIPLE LAYER POLYSILICON CELL
4119995 - ELECTRICALLY PROGRAMMABLE AND ELECTRICALLY ERASABLE MOS MEMORY CELL

INTELLIGENT INSTRUMENTS INC.
3486085 - MULTILAYER INTEGRATED CIRCUIT STRUCTURE

INTERGRATED PHOTOMATRIX LTD.
3816769 - METHOD AND CIRCUIT ELEMENT FOR THE SELECTIVE CHARGING OF A SEMICONDUCTOR DIFFUSION REGION

INTERNATIONAL BUSINESS MACHINES CORPORATION
3419956 - TECHNIQUE FOR OBTAINING ISOLATED INTEGRATED CIRCUITS
3420719 - METHOD OF MAKING SEMICONDUCTORS BY LASER INDUCED DIFFUSION
3427445 - FULL ADDER USING FIELD EFFECT TRANSISTOR OF THE INSULATED GATE TYPE
3432670 - RADIATION SCANNER, EMPLOYING CONSTANT CURRENT MEANS
3433686 - PROCESS OF BONDING CHIPS IN A SUBSTRATE RECESS BY EPITAXIAL GROWTH OF THE BONDING MATERIAL
3435365 - MONOLITHICALLY FABRICATED AMPLIFIER DEVICE WITH SELF DRIVE
3437890 - DIFFUSED-EPITAXIAL SCANISTORS
3443176 - LOW RESISTIVITY SEMICONDUCTOR UNDERPASS CONNECTOR AND FABRICATION METHOD THEREFOR
3445924 - METHOD FOR FABRICATING INSULATED-GATE FIELD EFFECT TRANSISTORS HAVING CONTROLLED OPERATING CHARACTERISTICS
3451866 - SEMICONDUCTOR DEVICE
3457633 - METHOD OF MAKING CRYSTAL SHAPES HAVING OPTICALLY RELATED SURFACE'
3460010 - THIN FILM DECOUPLING CAPACITOR INCORPORATED IN AN INTEGRATED CIRCUIT CHIP, AND PROCESS FOR MAKING SAME
3461357 - MULTILEVEL DEVICES
3461360 - SEMICONDUCTOR DEVICES WITH CUP-SHAPED REGIONS
3465427 - COMBINED TRANSISTOR AND TESTING STRUCTURES AND FABRICATION THEREOF
3473976 - CARRIER LIFETIME KILLER DOPING PROCESS FOR SEMICONDUCTOR STRUCTURES AND THE PRODUCT FORMED THEREBY
3475621 - STANDARDIZED HIGH-DENSITY INTEGRATED CIRCUIT ARRANGEMENT AND METHOD
3487233 - DETECTOR WITH UPPER AND LOWER THRESHOLD POINTS
3489963 - INTEGRATED DIFFERENTIAL TRANSISTOR
3491325 - TEMPERATURE COMPENSATION FOR SEMICONDUCTOR DEVICES
3497718 - BIPOLAR INTEGRATED SHIFT REGISTER
3500220 - SENSE AMPLIFIER ADAPTED FOR MONOLITHIC FABRICATION
3500224 - DIFFERENTIAL AMPLIFIER AND BIAS CIRCUIT ADAPTED FOR MONOLITHIC FABRICATION
3500255 - INTEGRATED CIRCUIT DIRECTIONAL COUPLER
3505573 - LOW STANDBY POWER MEMORY CELL
3506880 - SEMICONDUCTOR DEVICE
3506893 - INTEGRATED CIRCUITS WITH SURFACE BARRIER DIODES
3507036 - TEST SITES FOR MONOLITHIC CIRCUITS
3508209 - MONOLITHIC INTEGRATED MEMORY ARRAY STRUCTURE INCLUDING FABRICATION AND PACKAGE THEREFOR
3509364 - VIDEO AMPLIFIER PARTICULARLY ADAPTED FOR INTEGRATED CIRCUIT FABRICATION
3517224 - REGULATED TRANSISTORIZED CURRENT SOURCE HAVING TEMPERATURE COMPENSATION
3517280 - FOUR LAYER DIODE DEVICE INSENSITIVE TO RATE EFFECT AND METHOD OF MANUFACTURE
3517438 - METHOD OF PACKAGING A CIRCUIT MODULE AND JOINING SAME TO A CIRCUIT SUBSTRATE
3518503 - SEMICONDUCTOR STRUCTURES OF SINGLE CRYSTALS ON POLYCRYSTALLINE SUBSTRATES

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

INTERNATIONAL BUSINESS MACHINES CORPORATION (CONTINUED)

3524113 - COMPLEMENTARY PNP-NPN TRANSISTORS AND FABRICATION METHOD THEREFOR
3532899 - FIELD-EFFECT, ELECTRONIC SWITCH
3539876 - MONOLITHIC INTEGRATED STRUCTURE INCLUDING FABRICATION THEREOF
3547604 - FUNCTIONAL COMPONENTS
3547716 - ISOLATION IN EPITAXIALLY GROWN MONOLITHIC DEVICES
3551761 - INTEGRATED PHOTODIODE ARRAY
3553830 - METHOD FOR MAKING INTEGRATED CIRCUIT APPARATUS
3557444 - MONOLITHIC BIPOLAR TRANSISTOR LOGIC CIRCUIT AND METHOD OF FORMING SAME
3558374 - POLYCRYSTALLINE FILM HAVING CONTROLLED GRAIN SIZE AND METHOD OF MAKING SAME
3559003 - UNIVERSAL METALLURGY FOR SEMICONDUCTOR MATERIALS
3560277 - PROCESS FOR MAKING SEMICONDUCTOR BODIES HAVING POWER CONNECTIONS INTERNAL THERETO
3561108 - ALTERNATED ORIENTATION OF CHIPS ON SEMICONDUCTOR WAFERS
3562547 - PROTECTION DIODE FOR INTEGRATED CIRCUIT
3564290 - REGENERATIVE FET SOURCE FOLLOWER
3569800 - RESISTIVELY ISOLATED INTEGRATED CURRENT SWITCH
3573573 - MEMORY CELL WITH BURIED LOAD IMPEDANCES
3575740 - METHOD OF FABRICATING PLANAR DIELECTRIC ISOLATED INTEGRATED CIRCUITS
3577036 - METHOD AND MEANS FOR INTERCONNECTING CONDUCTORS ON DIFFERENT METALIZATION PATTERN LEVELS ON MONOLITHICALLY FABRICATED IN TEGRATED CIRCUIT CHIPS BY ALLOYING AN INTERCONNECTIOND PORTION OF EACH CONDUCTOR TO CONTIGUOUS PORTIONS OF ONE LOW RESIS
3577037 - DIFFUSED ELECTRICAL CONNECTOR APPARATUS AND METHOD OF MAKING SAME
3577044 - INTEGRATED SEMICONDUCTOR DEVICES AND FABRICATION METHODS THEREFOR
3577285 - METHOD FOR EPITAXIALLY GROWING SILICON CARBIDE ONTO A CRYSTALLINE SUBSTRATE
3584269 - DIFFUSED EQUAL IMPEDANCE INTERCONNECTIONS FOR INTEGRATED CIRCUITS
3585464 - SEMICONDUCTOR DEVICE FABRICATION UTILIZING 100 ORIENTED SUBSTRATE MATERIAL
3585613 - FIELD EFFECT TRANSISTOR CAPACITOR STORAGE CELL
3590477 - METHOD FOR FABRICATING INSULATED-GATE FIELD EFFECT TRANSISTORS HAVING CONTROLLED OPERATING CHARACTERISTICS
3602635 - MICRO-CIRCUIT DEVICE
3603820 - BISTABLE DEVICE STORAGE CELL
3607468 - METHOD OF FORMING SHALLOW JUNCTION SEMICONDUCTOR DEVICES
3609414 - APPARATUS FOR STABILIZING FIELD EFFECT TRANSISTOR THRESHOLDS
3610967 - INTEGRATED MEMORY CELL CIRCUIT
3611062 - PASSIVE ELEMENTS FOR SOLID STATE INTEGRATED CIRCUITS
3611071 - INVERSION PREVENTION SYSTEM FOR SEMICONDUCTOR DEVICES
3614560 - SURFACE BARRIER TRANSISTOR
3615466 - PROCESS OF PRODUCING AN ARRAY OF INTERGRATED CIRCUITS ON SEMICONDUCTOR SUBSTRATE
3619735 - INTEGRATED CIRCUIT WITH BURIED DECOUPLING CAPACITOR
3619737 - PLANAR JUNCTION-GATE FIELD-EFFECT TRANSISTORS
3621279 - HIGH DENSITY DYNAMIC SHIFT REGISTER
3621346 - PROCESS FOR FORMING SEMICONDUCTOR DEVICES WITH POLYCRYSTALLINE DIFFUSION PATHWAYS AND DEVICES FORMED THEREBY
3622382 - SEMICONDUCTOR ISOLATION STRUCTURE AND METHOD OF PRODUCING
3622842 - SEMICONDUCTOR DEVICE HAVING HIGH SWITCHING SPEED AND METHOD OF MAKING
3623029 - BISTABLE MULTI-EMITTER SILICON CONTROLLED RECTIFIER STORAGE CELL
3625781 - METHOD OF REDUCING CARRIER LIFETIME IN SEMICONDUCTOR STRUCTURES
3626157 - FIELD EFFECT PERFORATED MEDIA READER
3626387 - FET STORAGE-THRESHOLD VOLTAGE CHANGED BY IRRADIATION
3626390 - MINI MEMORY CELL WITH EPITAXIAL LAYER RESISTORS AND DIODE ISOLATION
3628069 - MONOLITHIC INVERSELY OPERATED TRANSISTORS
3629667 - SEMICONDUCTOR RESISTOR WITH UNIFORM CURRENT DISTRIBUTION AT ITS CONTACT SURFACE
3638081 - INTEGRATED CIRCUIT HAVING LIGHTLY DOPED EXPITAXIAL COLLECTOR LAYER SURROUNDING BASE AND EMITTER ELEMENTS AND HEAVILLY DO PED BURIED COLLECTOR LAYER IN CONTACT WITH THE BASE ELEMENT
3641516 - WRITE ONCE READ ONLY STORE SEMICONDUCTOR MEMORY
3643231 - MONOLITHIC ASSOCIATIVE MEMORY CELL
3643235 - MONOLITHIC SEMICONDUCTOR MEMORY
3644850 - INTEGRATED CIRCUIT BAND PASS FILTER

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

INTERNATIONAL BUSINESS MACHINES CORPORATION (CONTINUED)

3648130 - COMMON EMITTER TRANSISTOR INTEGRATED CIRCUIT STRUCTURE
3648131 - HOUR-GLASS SHAPED CONDUCTIVE CONNECTION THROUGH SEMICONDUCTOR STRUCTURES
3654530 - INTEGRATED CLAMPING CIRCUIT
3655457 - METHOD OF MAKING OR MODIFYING A PN JUNCTION BY ION IMPLANTATION
3656028 - CONSTRUCTION OF MONOLITHIC CHIP AND METHOD OF DISTRIBUTING POWER THEREIN FOR INDIVIDUAL ELECTRONIC DEVICES CONSTRUCTED T HEREON
3656034 - INTEGRATED LATERAL TRANSISTOR HAVING INCREASED BETA AND BANDWIDTH
3657612 - INVERSE TRANSISTOR WITH HIGH CURRENT GAIN
3660180 - CONSTRAINMENT OF AUTODOPING IN EPITAXIAL DEPOSITION
3660822 - VARIABLE BREAKDOWN STORAGE CELL WITH NEGATIVE RESISTANCE OPERATING CHARACTERISTIC
3662351 - ALTERABLE-LATENT IMAGE MONOLITHIC MEMORY
3666548 - MONOCRYSTALLINE SEMICONDUCTOR BODY HAVING DIELECTRICALLY ISOLATED REGIONS AND METHOD OF FORMING
3667115 - FABRICATION OF SEMICONDUCTOR DEVICES WITH CUP-SHAPED REGIONS
3676713 - SATURATION CONTROL SCHEME FOR TTL CIRCUIT
3689803 - INTEGRATED CIRCUIT STRUCTURE HAVING A UNIQUE SURFACE METALLIZATION LAYOUT
3693032 - ANTISATURATION TECHNIQUE FOR TTL CIRCUITS
3693057 - MONOLITHIC CIRCUITS WITH PINCH RESISTORS
3697318 - MONOLITHIC INTEGRATED STRUCTURE INCLUDING FABRICATION THEREOF
3697962 - TWO DEVICE MONOLITHIC BIPOLAR MEMORY ARRAY
3703420 - LATERAL TRANSISTOR STRUCTURE AND PROCESS FOR FORMING THE SAME
3704384 - MONOLITHIC CAPACITOR STRUCTURE
3705419 - SILICON GATE FET-NIOBIUM OXIDE DIODE-MEMORY CELL
3707656 - TRANSISTOR COMPRISING LAYERS OF SILICON DIOXIDE AND SILICON NITRIDE
3709746 - DOUBLE EPITAXIAL METHOD OF FABRICATING A PEDESTAL TRANSISTOR
3710207 - POSITIONAL DEPENDENCY MONOLITHIC IMPEDANCE
3713908 - METHOD OF FABRICATING LATERAL TRANSISTORS AND COMPLEMENTARY TRANSISTORS
3717515 - PROCESS FOR FABRICATING A PEDESTAL TRANSISTOR
3717852 - ELECTRONICALLY REWRITABLE READ-ONLY MEMORY USING VIA CONNECTIONS
3721838 - REPAIRABLE SEMICONDUCTOR CIRCUIT ELEMENT AND METHOD OF MANUFACTURE
3723199 - OUTDIFFUSION EPITAXIAL SELF-ISOLATION TECHNIQUE FOR MAKING MONOLITHIC SEMICONDUCTOR DEVICES
3723200 - EPITAXIAL MIDDLE DIFFUSION ISOLATION TECHNIQUE FOR MAXIMIZING MICROCIRCUIT COMPONENT DENSITY
3723837 - RESISTOR BED STRUCTURE FOR MONOLITHIC MEMORY
3726719 - ION IMPLANTED SEMICONDUCTOR STRUCTURES
3728166 - SEMICONDUCTOR DEVICE FABRICATION METHOD AND PRODUCT THEREBY
3729662 - SEMICONDUCTOR RESISTOR
3729719 - STORED CHARGE STORAGE CELL USING A NON LATCHING SCR TYPE DEVICE
3730786 - PERFORMANCE MATCHED COMPLEMENTARY PAIR TRANSISTORS
3734787 - FABRICATION OF DIFFUSED JUNCTION CAPACITOR BY SIMULTANEOUS OUTDIFFUSION
3735358 - SPECIALIZED ARRAY LOGIC
3736477 - MONOLITHIC SEMICONDUCTOR CIRCUIT FOR A LOGIC CIRCUIT CONCEPT OF HIGH PACKING DENSITY
3737739 - SINGLE CRYSTAL REGIONS IN DIELECTRIC SUBSTRATE
3740620 - STORAGE SYSTEM HAVING HETEROJUNCTION-HOMOJUNCTION DEVICES
3747064 - FET DYNAMIC LOGIC CIRCUIT AND LAYOUT
3749987 - SEMICONDUCTOR DEVICE EMBODYING FIELD EFFECT TRANSISTORS AND SCHOTTKY BARRIER DIODES
3751720 - RADIALLY ORIENTED MONOLITHIC CIRCUIT MASTERSLICE
3752715 - PRODUCTION OF HIGH SPEED COMPLEMENTARY TRANSISTORS
3756862 - PROTON ENHANCED DIFFUSION METHODS
3760242 - COATED SEMICONDUCTOR STRUCTURES AND METHODS OF FORMING PROTECTIVE COVERINGS ON SUCH STRUCTURES
3761896 - MEMORY ARRAY OF CELLS CONTAINING BISTABLE SWITCHABLE RESISTORS
3762037 - METHOD OF TESTING FOR THE OPERABILITY OF INTEGRATED SEMICONDUCTOR CIRCUITS HAVING A PLURALITY OF SEPARABLE CIRCUITS
3766438 - PLANAR DIELECTRIC ISOLATED INTEGRATED CIRCUITS
3769105 - PROCESS FOR MAKING A INTEGRATED CIRCUIT WITH A DAMPING RESISTOR IN COMBINATION WITH A BURIED DECOUPLING CAPACITOR
3770516 - MONOLITHIC INTEGRATED CIRCUITS
3770519 - ISOLATION DIFFUSION METHOD FOR MAKING REDUCED BETA TRANSISTOR OR DIODES
3770968 - FIELD EFFECT TRANSISTOR DETECTOR AMPLIFIER CELL AND CIRCUIT FOR LOW LEVEL LIGHT SIGNALS

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

INTERNATIONAL BUSINESS MACHINES CORPORATION (CONTINUED)

3774079 - MONOLITHICALLY FABRICATED TRANSISTOR CIRCUIT WITH MULTILAYER CONDUCTIVE PATTERNS
3774088 - INTEGRATED CIRCUIT TEST TRANSISTOR STRUCTURE AND METHOD OF FABRICATING THE SAME
3780320 - SCHOTTKY BARRIER DIODE READ-ONLY MEMORY
3781609 - SEMICONDUCTOR INTEGRATED CIRCUIT CHIP STRUCTURE PROTECTED AGAINST IMPACT DAMAGE FROM OTHER CHIPS DURING CHIP HANDLING
3784976 - MONOLITHIC ARRAY ERROR DETECTION SYSTEM
3785886 - SEMICONDUCTOR DEVICE FABRICATION UTILIZING (100) ORIENTED SUBSTRATE MATERIAL
3787253 - EMITTER DIFFUSION ISOLATED SEMICONDUCTOR STRUCTURE
3787717 - OVER VOLTAGE PROTECTION CIRCUIT LATERAL BIPOLAR TRANSISTOR WITH GATED COLLECTOR JUNCTION
3795828 - MONOLITHIC DECODER CIRCUIT
3795845 - SEMICONDUCTOR CHIP HAVING CONNECTING PADS ARRANGED IN A NON-ORTHOGONAL ARRAY
3796613 - METHOD OF FORMING DIELECTRIC ISOLATION FOR HIGH DENSITY PEDESTAL SEMICONDUCTOR DEVICES
3796933 - SINGLE-PHASE CHARGE-COUPLED SEMICONDUCTOR DEVICE
3798512 - FET DEVICE WITH GUARD RING AND FABRICATION METHOD THEREFOR
3798621 - MONOLITHIC STORAGE ARRANGEMENT WITH LATENT BIT PATTERN
3801836 - COMMON EMITTER TRANSISTOR INTEGRATED CIRCUIT STRUCTURE
3801905 - METHOD OF TESTING FOR THE OPERABILITY OF INTEGRATED SEMICONDUCTOR CIRCUITS HAVING A PLURALITY OF SEPARABLE CIRCUITS
3801967 - MONOLITHIC BIPOLAR TRANSISTOR STORAGE ARRANGEMENT WITH LATENT BIT PATTERN
3810123 - MONOLITHIC STORAGE MULTI-EMITTER TRANSISTORS WITH DIFFERENT WIDTH BASES
3811076 - FIELD EFFECT TRANSISTOR INTEGRATED CIRCUIT AND MEMORY
3817797 - CONSTRUCTION OF MONOLITHIC CHIP AND METHOD OF DISTRIBUTING POWER THEREIN FOR INDIVIDUAL ELECTRONIC DEVICES CONSTRUCTED T HEREON
3817798 - METHOD OF FORMING INTEGRATED SEMICONDUCTOR DEVICES WITH III-V COMPOUNDS
3821781 - COMPLEMENTARY FIELD EFFECT TRANSISTORS HAVING P DOPED SILICON GATES
3823353 - MULTI LAYERED VERTICAL TRANSISTOR HAVING REACH-THROUGH ISOLATING CONTACTS
3832574 - FAST INSULATED GATE FIELD EFFECT TRANSISTOR CIRCUIT USING MULTIPLE THRESHOLD TECHNOLOGY
3834959 - PROCESS FOR THE FORMATION OF SELF-ALIGNED SILICON AND ALUMINUM GATES
3836992 - ELECTRICALLY ERASABLE FLOATING GATE FET MEMORY CELL
3838405 - NON-VOLATILE DIODE CROSS POINT MEMORY ARRAY
3840409 - INSULATING LAYER PEDESTAL TRANSISTOR DEVICE AND PROCESS
3840886 - MICROAMPERE SPACE CHARGE LIMITED TRANSISTOR
3840888 - COMPLEMENTARY MOSFET DEVICE STRUCTURE
3841926 - INTEGRATED CIRCUIT FABRICATION PROCESS
3843954 - HIGH-VOLTAGE INTEGRATED DRIVER CIRCUIT AND MEMORY EMBODYING SAME
3846193 - MINIMIZING CROSS-TALK IN L. E. D. ARRAYS
3846259 - SEMICONDUCTOR FABRICATION METHOD FOR ACCOMMODATING REDUNDANCY
3846768 - FIXED THRESHOLD VARIABLE THRESHOLD STORAGE DEVICE FOR USE IN A SEMICONDUCTOR STORAGE ARRAY
3849872 - CONTACTING INTEGRATED CIRCUIT CHIP TERMINAL THROUGH THE WAFER KERF
3852796 - GAN SWITCHING AND MEMORY DEVICES AND METHODS THEREFOR
3855609 - SPACE CHARGE LIMITED TRANSISTOR HAVING RECESSED DIELECTRIC ISOLATION
3858060 - INTEGRATED DRIVER CIRCUIT
3858061 - MULTIPLE SIZE GATES ON FET CHIPS
3858231 - DIELECTRICALLY ISOLATED SCHOTTKY BARRIER STRUCTURE AND METHOD OF FORMING THE SAME
3860454 - FIELD EFFECT TRANSISTOR STRUCTURE FOR MINIMIZING PARASITIC INVERSION AND PROCESS FOR FABRICATING
3861968 - METHOD OF FABRICATING INTEGRATED CIRCUIT DEVICE STRUCTURE WITH COMPLEMENTARY ELEMENTS UTILIZING SELECTIVE THERMAL OXIDAT ION AND SELECTIVE EPITAXIAL DEPOSITION
3865648 - METHOD OF MAKING A COMMON EMITTER TRANSISTOR INTEGRATED CIRCUIT STRUCTURE
3865652 - METHOD OF FORMING SELF-ALIGNED FIELD EFFECT TRANSISTOR AND CHARGE-COUPLED DEVICE
3865654 - COMPLEMENTARY FIELD EFFECT TRANSISTOR HAVING P DOPED SILICON GATES AND PROCESS FOR MAKING THE SAME
3877051 - MULTILAYER INSULATION INTEGRATED CIRCUIT STRUCTURE
3879236 - METHOD OF MAKING A SEMICONDUCTOR RESISTOR
3884732 - MONOLITHIC STORAGE ARRAY AND METHOD OF MAKING
3886000 - METHOD FOR CONTROLLING DIELECTRIC ISOLATION OF A SEMICONDUCTOR DEVICE
3899372 - PROCESS FOR CONTROLLING INSULATING FILM THICKNESS ACROSS A SEMICONDUCTOR WAFER
3911464 - NONVOLATILE SEMICONDUCTOR MEMORY
3916218 - INTEGRATED POWER SUPPLY FOR MERGED TRANSISTOR LOGIC CIRCUIT

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

INTERNATIONAL BUSINESS MACHINES CORPORATION (CONTINUED)

3919060 - METHOD OF FABRICATING SEMICONDUCTOR DEVICE EMBODYING DIELECTRIC ISOLATION
3922565 - MONOLITHICALLY INTEGRABLE DIGITAL BASIC CIRCUIT
3922707 - DC TESTING OF INTEGRATED CIRCUITS AND A NOVEL INTEGRATED CIRCUIT STRUCTURE TO FACILITATE SUCH TESTING
3922708 - METHOD OF PRODUCING HIGH VALUE ION IMPLANTED RESISTORS
3936856 - SPACE-CHARGE-LIMITED INTEGRATED CIRCUIT STRUCTURE
3943542 - HIGH RELIABILITY, LOW LEAKAGE, SELF-ALIGNED SILICON GATE FET AND METHOD OF FABRICATING SAME
3944447 - METHOD FOR FABRICATION OF INTEGRATED CIRCUIT STRUCTURE WITH FULL DIELECTRIC ISOLATION UTILIZING SELECTIVE OXIDATION
3954523 - PROCESS FOR FABRICATING DEVICES HAVING DIELECTRIC ISOLATION UTILIZING ANODIC TREATMENT AND SELECTIVE OXIDATION
3955210 - ELIMINATION OF SCR STRUCTURE
3955269 - FABRICATING HIGH PERFORMANCE INTEGRATED BIPOLAR AND COMPLEMENTARY FIELD EFFECT TRANSISTORS
3956641 - COMPLEMENTARY TRANSISTOR CIRCUIT FOR CARRYING OUT BOOLEAN FUNCTIONS
3958264 - SPACE-CHARGE-LIMITED PHOTOTRANSISTOR
3961355 - SEMICONDUCTOR DEVICE HAVING ELECTRICALLY INSULATING BARRIERS FOR SURFACE LEAKAGE SENSITIVE DEVICES AND METHOD OF FORMING
3961999 - METHOD FOR FORMING RECESSED DIELECTRIC ISOLATION WITH A MINIMIZED "BIRD'S BEAK" PROBLEM
3966514 - METHOD FOR FORMING DIELECTRIC ISOLATION COMBINING DIELECTRIC DEPOSITION AND THERMAL OXIDATION
3969750 - DIFFUSED JUNCTION CAPACITOR AND PROCESS FOR PRODUCING THE SAME
3972754 - METHOD FOR FORMING DIELECTRIC ISOLATION IN INTEGRATED CIRCUITS
3974003 - CHEMICAL VAPOR DEPOSITION OF DIELECTRIC FILMS CONTAINING AL, N, AND SI
3975220 - DIFFUSION CONTROL FOR CONTROLLING PARASITIC CAPACITOR EFFECTS IN SINGLE FET STRUCTURE ARRAYS
3976511 - METHOD FOR FABRICATING INTEGRATED CIRCUIT STRUCTURES WITH FULL DIELECTRIC ISOLATION BY ION BOMBARDMENT
3978577 - FIXED AND VARIABLE THRESHOLD N-CHANNEL MNOSFET INTEGRATION TECHNIQUE
3979734 - MULTIPLE ELEMENT CHARGE STORAGE MEMORY CELL
3982974 - COMPENSATION OF AUTODOPING IN THE MANUFACTURE OF INTEGRATED CIRCUITS
3983545 - RANDOM ACCESS MEMORY EMPLOYING SINGLE ENDED SENSE LATCH FOR ONE DEVICE CELL
3983572 - SEMICONDUCTOR DEVICES
3986173 - MEMORY CIRCUIT
3986180 - DEPLETION MODE FIELD EFFECT TRANSISTOR MEMORY SYSTEM
3988619 - RANDOM ACCESS SOLID-STATE IMAGE SENSOR WITH NON-DESTRUCTIVE READ-OUT
3995301 - NOVEL INTEGRATABLE SCHOTTKY BARRIER STRUCTURE AND A METHOD FOR THE FABRICATION THEREOF
3995307 - INTEGRATED MONOLITHIC SWITCH FOR HIGH VOLTAGE APPLICATIONS
3998674 - METHOD FOR FORMING RECESSED REGIONS OF THERMALLY OXIDIZED SILICON AND STRUCTURES THEREOF UTILIZING ANISOTROPIC ETCHING
3999214 - WIREABLE PLANAR INTEGRATED CIRCUIT CHIP STRUCTURE
4001612 - LINEAR RESISTANCE ELEMENT FOR LSI CIRCUITRY
4001868 - LATCHING DRIVER CIRCUIT AND STRUCTURE FOR A GAS PANEL DISPLAY
4002511 - METHOD FOR FORMING MASKS COMPRISING SILICON NITRIDE AND NOVEL MASK STRUCTURES PRODUCED THEREBY
4005469 - P-TYPE-EPITAXIAL-BASE TRANSISTOR WITH BASE-COLLECTOR SCHOTTKY DIODE CLAMP
4005471 - SEMICONDUCTOR RESISTOR HAVING A HIGH VALUE RESISTANCE FOR USE IN AN INTEGRATED CIRCUIT SEMICONDUCTOR DEVICE
4006492 - HIGH DENSITY SEMICONDUCTOR CHIP ORGANIZATION
4007103 - PLANARIZING INSULATIVE LAYERS BY RESPUTTERING
4015147 - LOW POWER TRANSMISSION LINE TERMINATOR
4016596 - HIGH PERFORMANCE INTEGRATED BIPOLAR AND COMPLEMENTARY FIELD EFFECT TRANSISTORS
4021789 - SELF-ALIGNED INTEGRATED CIRCUITS
4021838 - SEMICONDUCTOR INTEGRATED CIRCUIT DEVICES
4023148 - WRITE SPEED-UP CIRCUIT FOR INTEGRATED DATA MEMORIES
4024417 - INTEGRATED SEMICONDUCTOR STRUCTURE WITH MEANS TO PREVENT UNLIMITED CURRENT FLOW
4024561 - FIELD EFFECT TRANSISTOR MONITORS
4028149 - PROCESS FOR FORMING MONOCRYSTALLINE SILICON CARBIDE ON SILICON SUBSTRATES
4032372 - EPITAXIAL OUTDIFFUSION TECHNIQUE FOR INTEGRATED BIPOLAR AND FIELD EFFECT TRANSISTORS
4032962 - HIGH DENSITY SEMICONDUCTOR INTEGRATED CIRCUIT LAYOUT
4035664 - CURRENT HOGGING INJECTION LOGIC
4038110 - PLANARIZATION OF INTEGRATED CIRCUIT SURFACES THROUGH SELECTIVE PHOTORESIST MASKING
4044452 - PROCESS FOR MAKING FIELD EFFECT AND BIPOLAR TRANSISTORS ON THE SAME SEMICONDUCTOR CHIP
4044454 - METHOD FOR FORMING INTEGRATED CIRCUIT REGIONS DEFINED BY RECESSED DIELECTRIC ISOLATION
4053925 - METHOD AND STRUCTURE FOR CONTROLLNG CARRIER LIFETIME IN SEMICONDUCTOR DEVICES
4055884 - FABRICATION OF POWER FIELD EFFECT TRANSISTORS AND THE RESULTING STRUCTURES

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

INTERNATIONAL BUSINESS MACHINES CORPORATION (CONTINUED)

4057823 - POROUS SILICON DIOXIDE MOISTURE SENSOR AND METHOD FOR MANUFACTURE OF A MOISTURE SENSOR
4068217 - ULTIMATE DENSITY NON-VOLATILE CROSS-POINT SEMICONDUCTOR MEMORY ARRAY
4072868 - FET INVERTER WITH ISOLATED SUBSTRATE LOAD
4075045 - METHOD FOR FABRICATING FET ONE-DEVICE MEMORY CELLS WITH TWO LAYERS OF POLYCRYSTALLINE SILICON AND FABRICATION OF INTEGRA TED CIRCUITS CONTAINING ARRAYS OF THE MEMORY CELLS CHARGE STORAGE CAPACITORS UTILIZING FIVE BASIC PATTERN DELIBERATING S
4078947 - METHOD FOR FORMING A NARROW CHANNEL LENGTH MOS FIELD EFFECT TRANSISTOR
4079408 - SEMICONDUCTOR STRUCTURE WITH ANNULAR COLLECTOR/SUBCOLLECTOR REGION
4085498 - FABRICATION OF INTEGRATED CIRCUITS CONTAINING ENHANCEMENT-MODE FETS AND DEPLETION-MODE FETS WITH TWO LAYERS OF POLYCRYST ALLINE SILICON UTILIZING FIVE BASIC PATTERN DELINEATING STEPS
4090254 - CHARGE INJECTOR TRANSISTOR MEMORY
4092548 - SUBSTRATE BIAS MODULATION TO IMPROVE MOSFET CIRCUIT PERFORMANCE
4095251 - FIELD EFFECT TRANSISTORS AND FABRICATION OF INTEGRATED CIRCUITS CONTAINING THE TRANSISTORS
4102714 - PROCESS FOR FABRICATING A LOW BREAKDOWN VOLTAGE DEVICE FOR POLYSILICON GATE TECHNOLOGY
4104086 - METHOD FOR FORMING ISOLATED REGIONS OF SILICON UTILIZING REACTIVE ION ETCHING
4104090 - TOTAL DIELECTRIC ISOLATION UTILIZING A COMBINATION OF REACTIVE ION ETCHING, ANODIC ETCHING, AND THERMAL OXIDATION
4106050 - INTEGRATED CIRCUIT STRUCTURE WITH FULLY ENCLOSED AIR ISOLATION
4110125 - METHOD FOR FABRICATING SEMICONDUCTOR DEVICES
4110126 - NPN/PNP FABRICATION PROCESS WITH IMPROVED ALIGNMENT
4111720 - METHOD FOR FORMING A NON-EPITAXIAL BIPOLAR INTEGRATED CIRCUIT
4113512 - TECHNIQUE FOR PREVENTING FORWARD BIASED EPI-ISOLATION DEGRADATION
4115794 - CHARGE PUMPING DEVICE WITH INTEGRATED REGULATING CAPACITOR AND METHOD FOR MAKING SAME
4118250 - PROCESS FOR PRODUCING INTEGRATED CIRCUIT DEVICES BY ION IMPLANTATION
4123300 - INTEGRATED CIRCUIT PROCESS UTILIZING LIFT-OFF TECHNIQUES
4131497 - METHOD OF MANUFACTURING SELF-ALIGNED SEMICONDUCTOR DEVICES
4135954 - METHOD FOR FABRICATING SELF-ALIGNED SEMICONDUCTOR DEVICES UTILIZING SELECTIVELY ETCHABLE MASKING LAYERS
4139442 - REACTIVE ION ETCHING METHOD FOR PRODUCING DEEP DIELECTRIC ISOLATION IN SILICON
4139935 - OVER VOLTAGE PROTECTIVE DEVICE AND CIRCUITS FOR INSULATED GATE TRANSISTORS
4144493 - INTEGRATED CIRCUIT TEST STRUCTURE
4145700 - POWER FIELD EFFECT TRANSISTORS
4149915 - PROCESS FOR PRODUCING DEFECT-FREE SEMICONDUCTOR DEVICES HAVING OVERLAPPING HIGH CONDUCTIVITY IMPURITY REGIONS
4151010 - FORMING ADJACENT IMPURITY REGIONS IN A SEMICONDUCTOR BY OXIDE MASKING
4155778 - FORMING SEMICONDUCTOR DEVICES HAVING ION IMPLANTED AND DIFFUSED REGIONS
4157268 - LOCALIZED OXIDATION ENHANCEMENT FOR AN INTEGRATED INJECTION LOGIC CIRCUIT
4157560 - PHOTO DETECTOR CELL
4158237 - MONOLITHICALLY INTEGRATED STORAGE CELLS
4158783 - CURRENT HOGGING INJECTION LOGIC WITH SELF-ALIGNED OUTPUT TRANSISTORS
4159915 - METHOD FOR FABRICATION VERTICAL NPN AND PNP STRUCTURES UTILIZING ION-IMPLANTATION
4160987 - FIELD EFFECT TRANSISTORS WITH POLYCRYSTALLINE SILICON GATE SELF-ALIGNED TO BOTH CONDUCTIVE AND NON-CONDUCTIVE REGIONS AN D FABRICATION OF INTEGRATED CIRCUITS CONTAINING THE TRANSISTORS
4160991 - HIGH PERFORMANCE BIPOLAR DEVICE AND METHOD FOR MAKING SAME
4164668 - METHOD OF CORRECTING THE VOLTAGE COEFFICIENT OF RESISTORS IMPLANTED OR DIFFUSED IN A SEMICONDUCTOR SUBSTRATE
4169000 - METHOD OF FORMING AN INTEGRATED CIRCUIT STRUCTURE WITH FULLY-ENCLOSED AIR ISOLATION
4170017 - HIGHLY INTEGRATED SEMICONDUCTOR STRUCTURE PROVIDING A DIODE-RESISTOR CIRCUIT CONFIGURATION

INTERNATIONAL COMPUTERS LIMITED
4092185 - METHOD OF MANUFACTURING SILICON INTEGRATED CIRCUITS UTILIZING SELECTIVELY DOPED OXIDES

INTERNATIONAL RECTIFIER CORPORATION
3462655 - SMICONDUCTOR WAFER FORMING A PLURALITY OF RECTIFIERS
3831067 - SEMICONDUCTOR DEVICE WITH PRESSURE CONNECTION ELECTRODES AND WITH HEADERS CEMENTED TO INSULATION RING

INTERNATIONAL STANDARD ELECTRIC CORPORATION
3428499 - SEMICONDUCTOR PROCESS INCLUDING REDUCTION OF THE SUBSTRATE THICKNESS
3445596 - CAPACITOR MICROPHONE EMPLOYING A FIELD EFFECT SEMICONDUCTOR

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

INTERNATIONAL STANDARD ELECTRIC CORPORATION (CONTINUED)
3473975 - SEMICONDUCTOR DEVICES
3518509 - COMPLEMENTARY FIELD-EFFECT TRANSISTORS ON COMMON SUBSTRATE BY MULTIPLE EPITAXY TECHNIQUES
3567964 - INTEGRATED CIRCUIT FOR REFERENCE AMPLIFIER
3567965 - TEMPERATURE COMPENSATED ZENDER DIODE
3594728 - DOUBLE INJECTION DIODE MATRIX SWITCH
3641390 - SOLID STATE LETTER DISPLAY DEVICE
3647580 - METHOD FOR THE MANUFACTURE OF A SOLID STATE CIRCUIT ADAPTABLE AS H.F. TUNER
3774989 - PATTERN DISPLAY APPARATUS
4132865 - ELECTRONIC SWITCH

INTERNATIONAL TELEPHONE AND TELEGRAPH CORPORATION
3546394 - ELECTRONICS SWITCHING TELEPHONE SYSTEM USING MOS DEVICES
3562040 - METHOD OF UNIFORMALLY AND RAPIDLY ETCHING NICHROME
3581164 - JUNCTION CAPACITANCE COMPONENT, ESPECIALLY FOR A MONOLITHIC MICROCIRCUIT
3584266 - DEPLETION LAYER CAPACITOR IN PARTICULAR FOR MONOLITHIC INTEGRATED CIRCUITS
3651489 - SECONDARY EMISSION FIELD EFFECT CHARGE STORAGE SYSTEM
3678300 - MONOLITHIC INTEGRABLE FLIP FLOP CIRCUIT
3684933 - SEMICONDUCTOR DEVICE SHOWING AT LEAST THREE SUCCESSIVE ZONES OF ALTERNATE OPPOSITE CONDUCTIVITY TYPE
3702947 - MONOLITHIC DARLINGTON TRANSISTORS WITH COMMON COLLECTOR AND SEPERATE SUBCOLLECTORS
3749610 - PRODUCTION OF SILICON INSULATED GATE AND ION IMPLANTED FIELD EFFECT TRANSISTOR
3820007 - MONOLITHIC INTEGRATED VOLTAGE STABILIZER CIRCUIT WITH TAPPED DIODE STRING
4005452 - METHOD FOR PROVIDING ELECTRICAL ISOLATING MATERIAL IN SELECTED REGIONS OF A SEMICONDUCTIVE MATERIAL AND THE PRODUCT PROD UCED THEREBY
4027322 - ZERO POINT SWITCHING THYRISTOR HAVING AN ISOLATED EMITTER REGION
4028563 - INTEGRATED ZENER DIODE
4036706 - METHOD FOR PROVIDING ELECTRICAL ISOLATION BETWEEN SPACED PORTIONS OF A LAYER OF SEMICONDUCTIVE MATERIAL AND THE PRODUCT PRODUCED THEREBY
4043849 - PLANAR DIFFUSION METHOD FOR AN I\2/ L CIRCUIT INCLUDING A BIPOLAR ANALOG CIRCUIT PART
4056415 - METHOD FOR PROVIDING ELECTRICAL ISOLATING MATERIAL IN SELECTED REGIONS OF A SEMICONDUCTIVE MATERIAL
4081823 - SEMICONDUCTOR DEVICE HAVING POROUS ANODIZED ALUMINUM ISOLATION BETWEEN ELEMENTS THEREOF
4144586 - SUBSTRATE-FED INJECTION-COUPLED MEMORY

INTERSIL, INC.
3733690 - DOUBLE JUNCTION READ ONLY MEMORY AND PROCESS OF MANUFACTURE
3742592 - ELECTRICALLY ALTERABLE INTEGRATED CIRCUIT READ ONLY MEMORY UNIT AND PROCESS OF MANUFACTURING
3848238 - DOUBLE JUNCTION READ ONLY MEMORY
3971058 - DUAL EMITTER PROGRAMMABLE MEMORY ELEMENT AND MATRIX
4020365 - INTEGRATED FIELD-EFFECT TRANSISTOR SWITCH
4064527 - INTEGRATED CIRCUIT HAVING A BURIED LOAD DEVICE

INVENTORS AND INVESTORS, INC.
3546469 - ELECTRO-OPTICAL DISPLACEMENT MEASURER USING ZONE PLATES
3569997 - PHOTOELECTRIC MICROCIRCUIT COMPONENTS MONOLYTHICALLY INTEGRATED WITH ZONE PLATE OPTICS

IWATSU ELECTRIC CO., LTD.
3655996 - PROTECTIVE CIRCUIT FOR INPUT CIRCUIT OF JUNCTION TYPE FIELD EFFECT TRANSISTOR

JOHNSON MATTHEY + CO., LIMITED
3520043 - SELF-REGULATING HEATING ELEMENTS

KABUSHIKI KAISHA KYODO DENSHI GIJUTSU KENKYUSHO
3770520 - PRODUCTION OF SEMICONDUCTOR INTEGRATED-CIRCUIT DEVICES
3894893 - METHOD FOR THE PRODUCTION OF MONOCRYSTAL-POLYCRYSTAL SEMICONDUCTOR DEVICES

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

KABUSHIKI KAISHA MEIDENSHA
4092703 - GATE CONTROLLED SEMICONDUCTOR DEVICE
4170020 - GATE TURN-OFF THYRISTOR FOR REDUCING THE ON CURRENT THEREOF

KABUSHIKI KAISHA SEIKOSHA
3934399 - ELECTRIC TIMEPIECE INCORPORATING RECTIFIER AND DRIVING CIRCUITS INTEGRATED IN A SINGLE CHIP
3938174 - SEMICONDUCTOR INTEGRATED CIRCUIT AND METHOD OF MANUFACTURE

KABUSHIKI KAISHA SUWA SEIKOSHA
3912559 - COMPLEMENTARY MIS-TYPE SEMICONDUCTOR DEVICES AND METHODS FOR MANUFACTURING SAME
3939642 - ELECTRONIC TIMEPIECE SEMICONDUCTOR INTERGRATED CIRCUIT
3967253 - DISPLAY DEVICE
4062039 - SEMI-CONDUCTOR INTEGRATED CIRCUIT
4106278 - ELECTRONIC TIMEPIECE UTILIZING SEMICONDUCTOR-INSULATING SUBSTRATE INTEGRATED CIRCUITRY
4112670 - ELECTRONIC TIMEPIECE

KISTLER INSTRUMENT CORPORATION
3454891 - CHARGE AMPLIFIER WITH PROTECTIVE DISCHARGE DEVICE

KOGYO GIJUTSUIN
3766446 - INTEGRATED CIRCUITS COMPRISING LATERAL TRANSISTORS AND PROCESS FOR FABRICATION THEREOF
3798514 - HIGH FREQUENCY INSULATED DATA FIELD EFFECT TRANSISTOR WITH PROTECTIVE DIODES
3821776 - DIFFUSION SELF ALIGNED MOSFET WITH PINCH-OFF ISOLATION
3946424 - HIGH FREQUENCY FIELD-EFFECT TRANSISTORS AND METHOD OF MAKING SAME
3950777 - FIELD-EFFECT TRANSISTOR

KOLLMORGEN CORPORATION
3703651 - TEMPERATURE-CONTROLLED INTEGRATED CIRCUITS

LABORATOIRES DE PHYSICOCHIMIE APPLIQUEE, ISSEC S.A.
4091375 - FLAT SCREEN SOLID STATE DISPLAY AND MEMORY DEVICE UTILIZING COLOR CENTERS

LEEDS + NORTHRUP COMPANY
3454894 - STABILIZATION OF DRAIN-ELECTRODE CURRENT OF INSULATED-GATE FIELD-EFFECT TRANSISTOR

LICENTIA PATENT-VERWALTUNGS-GMBH
3796931 - P-N JUNCTION SEMICONDUCTOR DEVICE PROVIDED WITH AN INSULATING LAYER HAVING TWO STABLE, RESISTANCE STATES
3803461 - SEMICONDUCTOR ARRANGEMENTS
3878406 - CIRCUIT ARRANGEMENT FOR DRIVING LIGHT EMITTING SEMICONDUCTOR COMPONENTS
4130826 - MONOLITHIC INTEGRATED SEMICONDUCTOR CIRCUIT
4164747 - SEMICONDUCTOR ARRANGEMENT

LITTON PRECISION PRODUCTS, INC.
3479572 - ACOUSTIC SURFACE WAVE DEVICE

LUCAS INDUSTRIES LIMITED
3756872 - METHOD OF MAKING NON-PLANAR SEMI-CONDUCTOR DEVICES

MARCONI COMPANY LIMITED
3827033 - SEMI-CONDUCTOR MEMORY DEVICE ARRANGEMENTS
3930912 - METHOD OF MANUFACTURING LIGHT EMITTING DIODES

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
3987474 - NON-VOLATILE CHARGE STORAGE ELEMENTS AND AN INFORMATION STORAGE APPARATUS EMPLOYING SUCH ELEMENTS
4067037 - TRANSISTOR HAVING HIGH F/T \ AT LOW CURRENTS
4101965 - SURFACE ACOUSTIC WAVE DEVICES FOR PROCESSING AND STORING SIGNALS

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

MASSACHUSETTS INSTITUTE OF TECHNOLOGY (CONTINUED)
4110122 - HIGH-INTENSITY, SOLID-STATE-SOLAR CELL DEVICE
4127900 - READING CAPACITOR MEMORIES WITH A VARIABLE VOLTAGE RAMP

MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.
3629724 - SEMI-CONDUCTOR OSCILLATING RESONANCE CIRCUIT DEVICE
3742318 - FIELD-EFFECT SEMICONDUCTOR DEVICE
3808473 - MULTI-COMPONENT SEMICONDUCTOR DEVICE HAVING ISOLATED PRESSURE SENSITIVE REGION
3811075 - MAGNETO-SENSITIVE DEVICE HAVING PN JUNCTION
3911289 - MOS TYPE SEMICONDUCTOR IC DEVICE
3924150 - TURNABLE PHOTOTRANSDUCERS
3931632 - SWITCHING DEVICE EQUIPPED WITH A SEMICONDUCTOR MEMORY ELEMENT
4064525 - NEGATIVE-RESISTANCE SEMICONDUCTOR DEVICE
4094007 - TEMPERATURE-COMPENSATED ANALOG VOLTAGE MEMORY DEVICE
4116102 - INTEGRATED CIRCUIT FOR AN ELECTRONIC MUSICAL INSTRUMENT
4143388 - MOS TYPE SEMICONDUCTOR DEVICE

MATSUSHITA ELECTRONICS CORPORATION
3436282 - METHOD OF MANUFACTURING SEMICONDUCTOR DEVICES
3600235 - METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE
3609412 - INTEGRATED IGFET SIGNAL CONVERTER CIRCUIT
3675161 - VARACTOR-CONTROLLED PN JUNCTION SEMICONDUCTOR MICROWAVE OSCILLATION DEVICE
3786319 - INSULATED-GATE FIELD-EFFECT TRANSISTOR
3865650 - METHOD FOR MANUFACTURING A MOS INTEGRATED CIRCUIT
3865651 - METHOD OF MANUFACTURING SERIES GATE TYPE MATRIX CIRCUITS
3874955 - METHOD OF MANUFACTURING AN MOS INTEGRATED CIRCUIT
3883772 - ELECTRIC LIGHT-EMITTING APPARATUS
3985591 - METHOD OF MANUFACTURING PARALLEL GATE MATRIX CIRCUITS
4053798 - NEGATIVE RESISTANCE DEVICE
4117587 - NEGATIVE-RESISTANCE SEMICONDUCTOR DEVICE
4136355 - DARLINGTON TRANSISTOR
4177096 - METHOD FOR MANUFACTURING A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

MCDONNELL DOUGLAS CORPORATION
3967305 - MULTICHANNEL JUNCTION FIELD-EFFECT TRANSISTOR AND PROCESS
4028562 - NEGATIVE IMPEDANCE TRANSISTOR DEVICE
4038563 - SYMMETRICAL INPUT NOR/NAND GATE CIRCUIT

MICRO COMPONENTS CORPORATION
3829709 - SUPPLY REVERSAL PROTECTION CIRCUIT

MICRO POWER SYSTEMS, INC.
4042953 - HIGH TEMPERATURE REFRACTORY METAL CONTACT ASSEMBLY AND MULTIPLE LAYER INTERCONNECT STRUCTURE

MICROSYSTEMS INTERNATIONAL LIMITED
3694673 - FIELD EFFECT DEVICE AND CIRCUIT HAVING HIGH CURRENT DRIVING CAPABILITIES UTILIZING SUCH DEVICE
3760238 - FABRICATION OF BEAM LEADS

MICROWAVE SEMICONDUCTOR CORP.
4161740 - HIGH FREQUENCY POWER TRANSISTOR HAVING REDUCED INTERCONNECTION INDUCTANCE AND THERMAL RESISTANCE

MITSUBISHI DENKI KABUSHIKI KAISHA
3819952 - SEMICONDUCTOR DEVICE
3979767 - MULTILAYER P-N JUNCTION SEMICONDUCTOR SWITCHING DEVICE HAVING A LOW RESISTANCE PATH ACROSS SAID P-N JUNCTION
3987478 - COMPOSITE TYPE SEMICONDUCTOR AND PREPARATION THEREOF
4080577 - SEMICONDUCTOR INTEGRATED CIRCUIT

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

MITSUBISHI DENKI KABUSHIKI KAISHA (CONTINUED)
4081697 - SEMICONDUCTOR MEMORY DEVICE
4084311 - PROCESS FOR PREPARING COMPLEMENTARY MOS INTEGRATED CIRCUIT

MITSUBISHI MINING + CEMENT COMPANY LTD.
3906425 - OXIDE SEMICONDUCTOR-METAL CONTACT RESISTANCE ELEMENTS

MITSUSHITA ELECTRONICS CORPORATION
3764864 - INSULATED-GATE FIELD-EFFECT TRANSISTOR WITH PUNCH-THROUGH EFFECT ELEMENT

MOHAWK DATA SCIENCES CORP.
3435295 - INTEGRATED POWER DRIVER CIRCUIT

MONOLITHIC MEMORIES, INC.
4152627 - LOW POWER WRITE-ONCE, READ-ONLY MEMORY ARRAY

MONSANTO COMPANY
3440883 - ELECTRONIC SEMICONDUCTOR THERMOMETER
3443151 - ELECTRICAL CONTROL CIRCUITS
3443172 - LOW CAPACITANCE FIELD EFFECT TRANSISTOR
3597287 - LOW CAPACITANCE FIELD EFFECT TRANSISTOR
3947840 - INTEGRATED SEMICONDUCTOR LIGHT-EMITTING DISPLAY ARRAY

MOS TECHNOLOGY, INC.
3855581 - SEMICONDUCTOR DEVICE AND CIRCUITS

MOSTEK CORPORATION
3775693 - MOSFET LOGIC INVERTER FOR INTEGRATED CIRCUITS
3881121 - DYNAMIC RANDOM ACCESS MEMORY INCLUDING CIRCUIT MEANS TO PREVENT DATA LOSS CAUSED BY BIPOLAR INJECTION RESULTING FROM CAP ACITIVE COUPLING
3898105 - METHOD FOR MAKING FET CIRCUITS
4125854 - SYMMETRICAL CELL LAYOUT FOR STATIC RAM

MOTOROLA INC.
3431468 - BURIED INTEGRATED CIRCUIT RADIATION SHIELDS
3434022 - SEMICONDUCTOR CONTROLLED RECTIFIER DEVICE
3439414 - METHOD FOR MAKING SEMICONDUCTOR STRUCTURE WITH LAYERS OF PRESELECTED RESISTIVITY AND CONDUCTIVITY TYPE
3445925 - METHOD FOR MAKING THIN SEMICONDUCTOR DICE
3446994 - HIGH THRESHOLD DIODE TRANSISTOR LOGIC CIRCUITRY
3452219 - VOLTAGE CONTROLLED DIGITAL CIRCUITS
3454846 - HIGH FREQUENCY TRANSISTOR HAVING A BASE REGION SUBSTRATE
3457123 - METHODS FOR MAKING SEMICONDUCTOR STRUCTURES HAVING GLASS INSULATED ISLANDS
3461003 - METHOD OF FABRICATING A SEMICONDUCTOR STRUCTURE WITH AN ELECTRICALLY ISOLATED REGION OF SEMI- CONDUCTOR MATERIAL
3462317 - THERMOCOUPLE ASSEMBLY
3486950 - LOCALIZED CONTROL OF CARRIER LIFETIMES IN P-N JUNCTION DEVICES AND INTEGRATED CIRCUITS
3496037 - SEMICONDUCTOR GROWTH ON DIELECTRIC SUBSTRATES
3502997 - INTEGRATED SEMICONDUCTOR CASCODE AMPLIFIER
3506887 - SEMICONDUCTOR DEVICE AND METHOD OF MAKING SAME
3508980 - METHOD OF FABRICATING AN INTEGRATED CIRCUIT STRUCTURE WITH DIELECTRIC ISOLATION
3510728 - ISOLATION OF MULTIPLE LAYER METAL CIRCUITS WITH LOW TEMPERATURE PHOSPHORUS SILICATES
3511727 - VAPOR PHASE ETCHING AND POLISHING OF SEMICONDUCTORS
3538397 - DISTRIBUTED SEMICONDUCTOR POWER SUPPLIES AND DECOUPLING CAPACITOR THEREFOR
3538449 - LATERAL DIFFERENTIAL AMPLIFIER
3540955 - METHOD FOR SELECTIVELY ETCHING SILICON SURFACES
3544863 - MONOLITHIC INTEGRATED CIRCUIT SUBSTRUCTURE WITH EPITAXIAL DECOUPLING CAPACITANCE
3559282 - METHOD FOR MAKING THIN SEMICONDUCTOR DICE

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

MOTOROLA INC. (CONTINUED)

3560278 - ALIGNMENT PROCESS FOR FABRICATING SEMICONDUCTOR DEVICES
3574932 - THIN-FILM BEAM-LEAD RESISTORS
3581165 - VOLTAGE DISTRIBUTION SYSTEM FOR INTEGRATED CIRCUITS UTILIZING LOW RESISTIVITY SEMICONDUCTIVE PATHS FOR THE TRANSMISSION OF VOLTAGES
3624463 - METHOD OF AND APPARATUS FOR INDICATING SEMICONDUCTOR ISLAND THICKNESS AND FOR INCREASING ISOLATION AND DECREASING CAPACITY BETWEEN ISLANDS
3664893 - FABRICATION OF FOUR-LAYER SWITCH WITH CONTROLLED BREAKOVER VOLTAGE
3667009 - COMPLEMENTARY METAL OXIDE SEMICONDUCTOR GATE PROTECTION DIODE
3670219 - CURRENT LIMITING TRANSISTOR
3696276 - INSULATED GATE FIELD-EFFECT DEVICE AND METHOD OF FABRICATION
3700977 - DIFFUSED RESISTOR
3703669 - PHOTOCURRENT CROSS TALK ISOLATION
3706130 - VOLTAGE DISTRIBUTION FOR INTEGRATED CIRCUITS
3707765 - METHOD OF MAKING ISOLATED SEMICONDUCTOR DEVICES
3716425 - METHOD OF MAKING SEMICONDUCTOR DEVICES THROUGH OVERLAPPING DIFFUSIONS
3717514 - SINGLE CRYSTAL SILICON CONTACT FOR INTEGRATED CIRCUITS AND METHOD FOR MAKING SAME
3720848 - SOLID-STATE RELAY
3721588 - THIN SINGLE CRYSTAL SILICON ON AN INSULATING SUBSTRATE AND IMPROVED DIELECTRIC ISOLATION PROCESSING METHOD
3723830 - LOW CURRENT, LOW NOISE AVALANCHE DIODE
3737704 - SCANNABLE LIGHT EMITTING DIODE ARRAY AND METHOD
3738877 - SEMICONDUCTOR DEVICES
3745430 - THICK FILM FEED-THROUGH CAPACITOR
3746945 - SCHOTTKY DIODE CLIPPER DEVICE
3746946 - INSULATED GATE FIELD-EFFECT TRANSISTOR INPUT PROTECTION CIRCUIT
3747200 - INTEGRATED CIRCUIT FABRICATION METHOD
3748543 - HERMETICALLY SEALED SEMICONDUCTOR PACKAGE AND METHOD OF MANUFACTURE
3750268 - POLY-SILICON ELECTRODES FOR C-IGFETS
3753806 - INCREASING FIELD INVERSION VOLTAGE OF METAL OXIDE ON SILICON INTEGRATED CIRCUITS
3755012 - CONTROLLED ANISTROPIC ETCHING PROCESS FOR FABRICATING DIELECTRICALLY ISOLATED FIELD EFFECT TRANSISTOR
3759762 - METHOD OF FORMING INTEGRATED CIRCUITS UTILIZING LOW RESISTANCE VALUES, LOW TEMPERATURE DEPOSITED OXIDES AND SHALLOW JUNCTIONS
3759763 - METHOD OF PRODUCING LOW THRESHOLD COMPLEMENTARY INSULATED GATE FIELD EFFECT DEVICES
3760380 - SILICON GATE COMPLEMENTARY MOS DYNAMIC RAM
3761787 - METHOD AND APPARATUS FOR ADJUSTING TRANSISTOR CURRENT
3772097 - EPITAXIAL METHOD FOR THE FABRICATION OF A DISTRIBUTED SEMICONDUCTOR POWER SUPPLY CONTAINING A DECOUPLING CAPACITOR
3776786 - METHOD OF PRODUCING HIGH SPEED TRANSISTORS AND RESISTORS SIMULTANEOUSLY
3777216 - AVALANCHE INJECTION INPUT PROTECTION CIRCUIT
3780322 - MINIMIZED TEMPERATURE COEFFICIENT VOLTAGE STANDARD MEANS
3783052 - PROCESS FOR MANUFACTURING INTEGRATED CIRCUITS ON AN ALUMINA SUBSTRATE
3797102 - METHOD OF MAKING SEMICONDUCTOR DEVICES
3800195 - SEMICONDUCTOR DEVICES
3806371 - METHOD OF MAKING COMPLEMENTARY MONOLITHIC INSULATED GATE FIELD EFFECT TRANSISTORS HAVING LOW THRESHOLD VOLTAGE AND LOW LEAKAGE CURRENT
3812405 - STABLE THYRISTOR DEVICE
3812521 - BONDING PAD SUBSTRUCTURE FOR INTEGRATED CIRCUITS
3813588 - EFFICIENT POWER DARLINGTON DEVICE CONFIGURATION
3832247 - PROCESS FOR MANUFACTURING INTEGRATED CIRCUITS
3840412 - METHOD OF MAKING SEMICONDUCTOR DEVICES THROUGH OVERLAPPING DIFFUSIONS
3853633 - METHOD OF MAKING A SEMI PLANAR INSULATED GATE FIELD-EFFECT TRANSISTOR DEVICE WITH IMPLANTED FIELD
3858062 - SOLID STATE CURRENT DIVIDER
3868721 - DIFFUSION GUARDED METAL-OXIDE-SILICON FIELD EFFECT TRANSISTORS
3876480 - METHOD OF MANUFACTURING HIGH SPEED, ISOLATED INTEGRATED CIRCUIT
3877055 - SEMICONDUCTOR MEMORY DEVICE
3877059 - SINGLE DIFFUSED MONOLITHIC DARLINGTON CIRCUIT AND METHOD OF MANUFACTURE THEREOF
3881179 - ZENER DIODE STRUCTURE HAVING THREE TERMINALS

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

MOTOROLA INC. (CONTINUED)

3886583 - INSULATED GATE-FIELD-EFFECT TRANSISTOR
3889287 - MNOS MEMORY MATRIX
3892608 - METHOD FOR FILLING GROOVES AND MOATS USED ON SEMICONDUCTOR DEVICES
3893149 - SCANNABLE LIGHT EMITTING DIODE ARRAY AND METHOD
3898684 - DIFFUSION GUARDED METAL-OXIDE-SILICON FIELD EFFECT TRANSISTORS
3902936 - GERMANIUM BONDED SILICON SUBSTRATE AND METHOD OF MANUFACTURE
3903406 - ACOUSTIC WAVE CORRELATOR CONTROL CIRCUITRY
3906255 - MOS CURRENT LIMITING OUTPUT CIRCUIT
3911466 - DIGITALLY CONTROLLABLE ENHANCED CAPACITOR
3911472 - ISOLATED CONTACT
3912556 - METHOD OF FABRICATING A SCANNABLE LIGHT EMITTING DIODE ARRAY
3913124 - INTEGRATED SEMICONDUCTOR TRANSISTOR STRUCTURE WITH EPITAXIAL CONTACT TO THE BURIED SUB-COLLECTOR INCLUDING FABRICATION METHOD THEREFOR
3929528 - FABRICATION OF MONOCRIPTALLINE SILICON ON INSULATING SUBSTRATES UTILIZING SELECTIVE ETCHING AND DEPOSITION TECHNIQUES
3932927 - SCANNABLE LIGHT EMITTING DIODE ARRAY AND METHOD
3940846 - SCANNABLE LIGHT EMITTING DIODE ARRAY AND METHOD
3946423 - OPTO-COUPLER
3948694 - SELF-ALIGNED METHOD FOR INTEGRATED CIRCUIT MANUFACTURE
3953875 - CAPACITOR STRUCTURE AND CIRCUIT FACILITATING INCREASED FREQUENCY STABILITY OF INTEGRATED CIRCUITS
3954522 - INTEGRATED CIRCUIT PROCESS
3956033 -
3959040 - COMPOUND DIFFUSED REGIONS FOR EMITTER-COUPLED LOGIC CIRCUITS
3964941 - METHOD OF MAKING ISOLATED COMPLEMENTARY MONOLITHIC INSULATED GATE FIELD EFFECT TRANSISTORS
3967988 - DIFFUSION GUARDED METAL-OXIDE-SILICON FIELD EFFECT TRANSISTORS
3968478 - CHIP TOPOGRAPHY FOR MOS INTERFACE CIRCUIT
3969168 - METHOD FOR FILLING GROOVES AND MOATS USED ON SEMICONDUCTOR DEVICES
3974404 - INTEGRATED CIRCUIT INTERFACE STAGE FOR HIGH NOISE ENVIRONMENT
3987418 - CHIP TOPOGRAPHY FOR MOS INTEGRATED CIRCUITRY MICROPROCESSOR CHIP
3996603 - RF POWER SEMICONDUCTOR PACKAGE AND METHOD OF MANUFACTURE
4006491 - INTEGRATED CIRCUIT HAVING INTERNAL MAIN SUPPLY VOLTAGE REGULATOR
4012243 - METHOD OF FABRICATING MULTICOLOR LIGHT DISPLAYS UTILIZING ETCH AND REFILL TECHNIQUES
4021270 - DOUBLE MASTER MASK PROCESS FOR INTEGRATED CIRCUIT MANUFACTURE
4023198 - HIGH FREQUENCY, HIGH POWER SEMICONDUCTOR PACKAGE
4037243 - SEMI CONDUCTOR MEMORY CELL UTILIZING SENSING OF VARIATIONS IN PN JUNCTION CURRENT CONROLLED BY STORED DATA
4037306 - INTEGRATED CIRCUIT AND METHOD
4042949 - SEMICONDUCTOR DEVICES
4042952 - R. F. POWER TRANSISTOR DEVICE WITH CONTROLLED COMMON LEAD INDUCTANCE
4048629 - LOW POWER MOS RAM ADDRESS DECODE CIRCUIT
4053915 - TEMPERATURE COMPENSATED CONSTANT CURRENT SOURCE DEVICE
4053923 - INTEGRATED LOGIC ELEMENTS WITH IMPROVED SPEED-POWER CHARACTERISTICS
4065736 - AMPLITUDE AND PHASE PROGRAMMABLE ACOUSTIC SURFACE WAVE MATCHED FILTER
4075508 - I\2/ L INJECTOR CURRENT SOURCE
4075609 - ON-CHIP VOLTAGE SOURCE FOR INTEGRATED CIRCUITS
4079337 - WIDE BANDWIDTH FEEDBACK AMPLIFIER
4100563 - SEMICONDUCTOR MAGNETIC TRANSDUCERS
4118642 - HIGHER DENSITY INSULATED GATE FIELD EFFECT CIRCUIT
4125415 - METHOD OF MAKING HIGH VOLTAGE SEMICONDUCTOR STRUCTURE
4161662 - STANDARDIZED DIGITAL LOGIC CHIP
4168507 - STRUCTURE AND TECHNIQUE FOR ACHIEVING REDUCED INDUCTIVE EFFECT OF UNDESIRED COMPONENTS OF COMMON LEAD INDUCTANCE IN A SEMICONDUCTIVE RF POWER PACKAGE

MURATA MANUFACTURING CO., LTD.
4132573 - METHOD OF MANUFACTURING A MONOLITHIC INTEGRATED CIRCUIT UTILIZING EPITAXIAL DEPOSITION AND SIMULTANEOUS OUTDIFFUSION

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

NATIONAL SEMICONDUCTOR CORPORATION
3421025 - HIGH-SPEED AVALANCHE SWITCHING CIRCUIT
3440498 - CONTACTS FOR INSULATION ISOLATED SEMICONDUCTOR INTEGRATED CIRCUITRY
3518750 - METHOD OF MANUFACTURING A MISFET
3566218 - MULTIPLE BASE WIDTH INTEGRATED CIRCUIT
3571630 - TWO-THERMAL MONOLITHIC VOLTAGE REGULATOR AND REACH- THROUGH TRANSISTOR
3575609 - TWO PHASE ULTRA-FAST MICROPOWER DYNAMIC SHIFT REGISTER
3593069 - INTEGRATED CIRCUIT RESISTOR AND METHOD OF MAKING THE SAME
3597640 - SHORT CIRCUIT PROTECTION MEANS FOR SEMICONDUCTIVE CIRCUIT APPARATUS
3607469 - METHOD OF OBTAINING LOW CONCENTRATION IMPURITY PREDEPOSITION ON A SEMICONDUCTIVE WAFER
3633052 - LOW NOISE INTEGRATED CIRCUIT ZENER VOLTAGE REFERENCE DEVICE INCLUDING A MULTIPLE COLLECTOR LATERAL TRANSISTOR
3702955 - MULTIPLE EMITTER TRANSISTOR APPARATUS
3886001 - METHOD OF FABRICATING A VERTICAL CHANNEL FET RESISTOR
3901735 - INTEGRATED CIRCUIT DEVICE AND METHOD UTILIZING ION IMPLANTED AND UP DIFFUSION FOR ISOLATED REGION
3916222 - FIELD EFFECT TRANSISTOR SWITCHING CIRCUIT
3936862 - MISFET AND METHOD OF MANUFACTURE
3958267 - CURRENT SCALING IN LATERAL PNP STRUCTURES
3971059 - COMPLEMENTARY BIPOLAR TRANSISTORS HAVING COLLECTOR DIFFUSED ISOLATION
3972061 - MONOLITHIC LATERAL S.C.R. HAVING REDUCED "ON" RESISTANCE
3982263 - INTEGRATED CIRCUIT DEVICE COMPRISING VERTICAL CHANNEL FET RESISTOR
3983620 - SELF-ALIGNED CMOS PROCESS FOR BULK SILICON AND INSULATING SUBSTRATE DEVICE
4016595 - FIELD EFFECT TRANSISTOR SWITCHING CIRCUIT
4043025 - SELF-ALIGNED CMOS PROCESS FOR BULK SILICON AND INSULATING SUBSTRATE DEVICE
4046605 - METHOD OF ELECTRICALLY ISOLATING INDIVIDUAL SEMICONDUCTOR CIRCUITS IN A WAFER
4047091 - CAPACITIVE VOLTAGE MULTIPLIER
4047284 - SELF-ALIGNED CMOS PROCESS FOR BULK SILICON AND INSULATING SUBSTRATE DEVICE
4066917 - CIRCUIT COMBINING BIPOLAR TRANSISTOR AND JFET'S TO PRODUCE A CONSTANT VOLTAGE CHARACTERISTIC
4075509 - CMOS COMPARATOR CIRCUIT AND METHOD OF MANUFACTURE
4085417 - JFET SWITCH CIRCUIT AND STRUCTURE
4095252 - COMPOSITE JFET-BIPOLAR TRANSISTOR STRUCTURE
4103186 - LOW POWER JFET SWITCH
4104784 - MANUFACTURING A LOW VOLTAGE N-CHANNEL MOSFET DEVICE
4110782 - MONOLITHIC INTEGRATED CIRCUIT TRANSISTOR HAVING VERY LOW COLLECTOR RESISTANCE
4115871 - MOS RANDOM MEMORY ARRAY
4127859 - INTEGRATED CIRCUIT SUBSURFACE ZENER DIODE
4138614 - JFET SWITCH CIRCUIT
4153909 - GATED COLLECTOR LATERAL TRANSISTOR STRUCTURE AND CIRCUITS USING SAME
4168997 - METHOD FOR MAKING INTEGRATED CIRCUIT TRANSISTORS WITH ISOLATION AND SUBSTRATE CONNECTED COLLECTORS UTILIZING SIMULTANEOUS OUTDIFFUSION TO CONVERT AN EPITAXIAL LAYER
4176368 - JUNCTION FIELD EFFECT TRANSISTOR FOR USE IN INTEGRATED CIRCUITS
4177095 - PROCESS FOR FABRICATING AN INTEGRATED CIRCUIT SUBSURFACE ZENER DIODE UTILIZING CONVENTIONAL PROCESSING STEPS

NCR CORPORATION
3482111 - HIGH SPEED LOGICAL CIRCUIT
3515850 - THERMAL PRINTING HEAD WITH DIFFUSED PRINTING ELEMENTS
3609294 - THERMAL PRINTING HEAD WITH THIN FILM PRINTING ELEMENTS
3636385 - PROTECTION CIRCUIT
3653002 - NONVOLATILE MEMORY CELL
3721962 - BEAM ACCESSED MOS MEMORY WITH BEAM READING, WRITING, AND ERASING
4001050 - METHOD OF FABRICATING AN ISOLATED P-N JUNCTION
4032373 - METHOD OF MANUFACTURING DIELECTRICALLY ISOLATED SEMICONDUCTIVE DEVICE
4156249 - SOLID STATE TUNABLE CAPACITOR

NIPPONDENSO CO., LTD.
3629623 - COMPOSITE SEMICONDUCTOR DEVICE AND SEMICONDUCTOR VOLTAGE REGULATOR DEVICE FOR VEHICLES

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

NIPPON ELECTRIC CO., LTD.
3423647 - SEMICONDUCTOR DEVICE HAVING REGIONS WITH PRE- SELECTED DIFFERENT MINORITY CARRIER LIFETIMES
3467952 - FIELD EFFECT TRANSISTOR INFORMATION STORAGE CIRCUIT
3472688 - RESISTOR ELEMENT AND METHOD FOR MANUFACTURING THE SAME
3479571 - FIELD EFFECT SEMICONDUCTOR DEVICE
3539839 - SEMICONDUCTOR MEMORY DEVICE
3551221 - METHOD OF MANUFACTURING A SEMICONDUCTOR INTEGRATED CIRCUIT
3555443 - STRUCTURE OF INTEGRATED CIRCUIT
3577018 - HIGH-SPEED LOGIC DEVICE EMPLOYING A GUNN-EFFECT ELEMENT AND A SEMICONDUCTOR LASER ELEMENT
3582725 - SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND THE METHOD OF MANUFACTURING THE SAME
3604989 - STRUCTURE FOR RIGIDLY MOUNTING A SEMICONDUCTOR CHIP ON A LEAD-OUT BASE PLATE
3612961 - SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE
3617824 - MOS DEVICE WITH A METAL-SILICIDE GATE
3619740 - INTEGRATED CIRCUIT HAVING COMPLEMENTARY FIELD EFFECT TRANSISTORS
3639813 - COMPLEMENTARY ENHANCEMENT AND DEPLETION MOSFETS WITH COMMON GATE AND CHANNEL REGION, THE DEPLETION MOSFET ALSO BEING A J FET
3646527 - ELECTRONIC MEMORY CIRCUIT EMPLOYING SEMICONDUCTOR MEMORY ELEMENTS AND A METHOD FOR WRITING TO THE MEMORY ELEMENT
3651490 - THREE DIMENSIONAL MEMORY UTILIZING SEMICONDUCTOR MEMORY DEVICES
3659162 - SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE HAVING IMPROVED WIRING LAYER STRUCTURE
3663872 - INTEGRATED CIRCUIT LATERAL TRANSISTOR
3665265 - MOS INTEGRATED CIRCUIT SEMICONDUCTOR DEVICE
3665423 - MEMORY MATRIX USING MIS SEMICONDUCTOR ELEMENT
3702466 - SEMICONDUCTOR INTEGRATED CIRCUIT MEMORY DEVICE UTILIZING INSULATED GATE TYPE SEMICONDUCTOR ELEMENTS
3702790 - MONOLITHIC INTEGRATED CIRCUIT DEVICE AND METHOD OF MANUFACTURING THE SAME
3718916 - SEMICONDUCTOR MEMORY ELEMENT
3725754 - TRANSISTOR CIRCUIT OF COMPOUND CONNECTION
3731161 - SEMICONDUCTOR INTEGRATED CIRCUIT
3748547 - INSULATED-GATE FIELD EFFECT TRANSISTOR HAVING GATE PROTECTION DIODE
3763405 - SOLID STATE LUMINESCENT DISPLAY DEVICE
3767984 - SCHOTTKY BARRIER TYPE FIELD EFFECT TRANSISTOR
3869622 - LOGIC GATE CIRCUIT INCLUDING A SCHOTTKY BARRIER DIODE
3887993 - METHOD OF MAKING AN OHMIC CONTACT WITH A SEMICONDUCTOR SUBSTRATE
3900351 - METHOD OF PRODUCING SEMICONDUCTOR INTEGRATED CIRCUITS WITH IMPROVED ISOLATION STRUCTURE
3932884 - MIS TYPE INTEGRATED CIRCUIT DEVICE
4016588 - NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE
4045784 - PROGRAMMABLE READ ONLY MEMORY INTEGRATED CIRCUIT DEVICE
4074304 - SEMICONDUCTOR DEVICE HAVING A MINIATURE JUNCTION AREA AND PROCESS FOR FABRICATING SAME
4084108 - INTEGRATED CIRCUIT DEVICE
4092445 - PROCESS FOR FORMING POROUS SEMICONDUCTOR REGION USING ELECTROLYTE WITHOUT ELECTRICAL SOURCE
4104785 - LARGE-SCALE SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE
4115709 - GATE CONTROLLED DIODE PROTECTION FOR DRAIN OF IGFET
4125878 - MEMORY CIRCUIT

NIPPON GAKKI SEIZO KABUSHIKI KAISHA
3812478 - SEMICONDUCTOR STORAGE DEVICE
4107725 - COMPOUND FIELD EFFECT TRANSISTOR
4150392 - SEMICONDUCTOR INTEGRATED FLIP-FLOP CIRCUIT DEVICE INCLUDING MERGED BIPOLAR AND FIELD EFFECT TRANSISTORS

NIPPON TELEGRAPH AND TELEPHONE PUBLIC CORPORATION
3484658 - TEMPERATURE COMPENSATED SEMICONDUCTOR RESISTOR
3601889 - METHOD OF MANUFACTURING THIN FILM RESISTOR ELEMENTS
3640806 - SEMICONDUCTOR DEVICE AND METHOD OF PRODUCING THE SAME
3811074 - SEMICONDUCTOR DEVICE AND APPARATUS USING THE SAME
4128845 - SEMICONDUCTOR INTEGRATED CIRCUIT DEVICES HAVING INVERTED FRUSTUM-SHAPE CONTACT LAYERS
4146902 - IRREVERSIBLE SEMICONDUCTOR SWITCHING ELEMENT AND SEMICONDUCTOR MEMORY DEVICE UTILIZING THE SAME

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

NORTH AMERICAN PHILIPS CORPORATION
3430050 - JUNCTION PHOTOCELL HAVING INTERMEDIATE LEVEL AND AUXILIARY LIGHT SOURCE TO EXCITE INTERMEDIATE LEVEL
3430112 - INSULATED GATE FIELD EFFECT TRANSISTOR WITH CHANNEL PORTIONS OF DIFFERENT CONDUCTIVITY
3435514 - METHODS OF MANUFACTURING SEMICONDUCTOR DEVICES
3436279 - PROCESS OF MAKING A TRANSISTOR WITH AN INVERTED STRUCTURE
3443169 - SEMICONDUCTOR DEVICE
3459967 - TRANSISTOR SWITCHING USING A TUNNEL DIODE
3653978 - METHOD OF MAKING SEMICONDUCTOR DEVICES
3772576 - PLANAR SEMICONDUCTOR DEVICE WITH SCRIBE LINES AND CHANNEL STOPPER
3973146 - SIGNAL DETECTOR COMPRISING FIELD EFFECT TRANSISTORS

NORTHERN TELECOM LIMITED
3423822 - METHOD OF MAKING LARGE SCALE INTEGRATED CIRCUIT
3449825 - FABRICATION OF SEMICONDUCTOR DEVICES
3515945 - SURGE PROTECTION DEVICE
3897282 - METHOD OF FORMING SILICON GATE DEVICE STRUCTURES WITH TWO OR MORE GATE LEVELS
4048647 - SOLID STATE DISCONNECT DEVICE
4115150 - METHOD OF PRODUCING OPTOELECTRONIC DEVICES WITH CONTROL OF LIGHT PROPAGATION

NOVA DEVICES, INC.
3729660 - IC DEVICE ARRANGED TO MINIMIZE THERMAL FEEDBACK EFFECTS

OLIVETTI, ING. C., + C. S.P.A.
3512041 - DISPLAY DEVICE COMPRISING A MATRIX OF SELECTION ELECTRODES, FIELD EFFECT TRANSISTORS AND LUMINESCENT ELEMENTS

OPTRON, INC.
4124860 - OPTICAL COUPLER

OWENS-ILLINOIS INC.
3598761 - CONDUCTOR COMPOSITIONS FOR MICROCIRCUITRY
3614739 - INTEGRATED DRIVING CIRCUITRY FOR GAS DISCHARGE PANEL
3754161 - INTEGRATED CIRCUIT SYSTEM

PLESSEY HANDEL UND INVESTMENTS AG
3961351 - IMPROVEMENT IN OR RELATING TO INTEGRATED CIRCUIT ARRANGEMENTS
4027180 - INTEGRATED CIRCUIT TRANSISTOR ARRANGEMENT HAVING A LOW CHARGE STORAGE PERIOD
4090259 - MEANS FOR CONTROLLING THE GATE POTENTIAL OF MNOS TRANSISTORS IN A MEMORY

POWER HYBRIDS, INC.
3969752 - HYBRID TRANSISTOR

PRD ELECTRONICS INC.
3423527 - SOLID STATE SCANNING DEVICE

PRECISION MONOLITHICS, INC.
4068254 - INTEGRATED FET CIRCUIT WITH INPUT CURRENT CANCELLATION

P. R. MALLORY + CO., INC.
3440648 - INTEGRATED-CIRCUIT AMPLIFIER AND OSCILLATOR
3465214 - HIGH-CURRENT INTEGRATED-CIRCUIT POWER TRANSISTOR

RADIATION INCORPORATED
3722079 - PROCESS FOR FORMING BURIED LAYERS TO REDUCE COLLECTOR RESISTANCE IN TOP CONTACT TRANSISTORS

RAYTHEON COMPANY
4070748 - INTEGRATED CIRCUIT STRUCTURE HAVING SEMICONDUCTOR RESISTANCE REGIONS

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

RAYTHEON COMPANY (CONTINUED)
4155783 - SEMICONDUCTOR STRUCTURES AND METHODS FOR MANUFACTURING SUCH STRUCTURES
4164461 - SEMICONDUCTOR INTEGRATED CIRCUIT STRUCTURES AND MANUFACTURING METHODS
4180422 - METHOD OF MAKING SEMICONDUCTOR DIODES

RAYTHEON CORPORATION
3423651 - MICROCIRCUIT WITH COMPLEMENTARY DIELECTRICALLY ISOLATED MESA-TYPE ACTIVE ELEMENTS
3432919 - METHOD OF MAKING SEMICONDUCTOR DIODES
3445727 - SEMICONDUCTOR CONTACT AND INTERCONNECTION STRUCTURE
3447235 - ISOLATED CATHODE ARRAY SEMICONDUCTOR
3454835 - MULTIPLE SEMICONDUCTOR DEVICE
3471922 - MONOLITHIC INTEGRATED CIRCUITRY WITH DIELECTRIC ISOLATED FUNCTIONAL REGIONS
3486087 - SMALL CAPACITY SEMICONDUCTOR DIODE
3486892 - PREFERENTIAL ETCHING TECHNIQUE
3493820 - AIRGAP ISOLATED SEMICONDUCTOR DEVICE
3499158 - CIRCUITS UTILIZING THE THRESHOLD PROPERTIES OF RECOMBINATION RADIATION SEMICONDUCTOR DEVICES
3514845 - METHOD OF MAKING INTEGRATED CIRCUITS WITH COMPLEMENTARY ELEMENTS
3761898 - RANDOM ACCESS MEMORY
3818289 - SEMICONDUCTOR INTEGRATED CIRCUIT STRUCTURES
3878550 - MICROWAVE POWER TRANSISTOR
3947298 - METHOD OF FORMING JUNCTION REGIONS UTILIZING R.F. SPUTTERING
3979612 - V-GROOVE ISOLATED INTEGRATED CIRCUIT MEMORY WITH INTEGRAL PINCHED RESISTORS
4032949 - INTEGRATED CIRCUIT FUSING TECHNIQUE

RCA CORPORATION
3423650 - MONOLITHIC SEMICONDUCTOR MICROCIRCUITS WITH IMPROVED MEANS FOR CONNECTING POINTS OF COMMON POTENTIAL
3430110 - MONOLITHIC INTEGRATED CIRCUITS WITH A PLURALITY OF ISOLATION ZONES
3430155 - INTEGRATED CIRCUIT BIASING ARRANGEMENT FOR SUPPLYING VBE BIAS VOLTAGES
3435138 - SOLID STATE IMAGE PICKUP DEVICE UTILIZING INSULATED GATE FIELD EFFECT TRANSISTORS
3441748 - BIDIRECTIONAL IGFET WITH SYMMETRICAL LINEAR RESISTANCE WITH SPECIFIC SUBSTRATE VOLTAGE CONTROL
3443175 - PN-JUNCTION LAYER ON ONE
3453724 - METHOD OF FABRICATING SEMICONDUCTOR DEVICE
3460007 - SEMICONDUCTOR JUNCTION DEVICE
3460049 - SINGLE ENDED AND DIFFERENTIAL STABILIZED AMPLIFIER
3461361 - COMPLEMENTARY MOS TRANSISTOR INTEGRATED CIRCUITS WITH INVERSION LAYER FORMED BY IONIC DISCHARGE BOMBARDMENT
3465292 - FLEXODE CROSSPOINT ADAPTIVE MATRIX CIRCUITS
3471923 - METHOD OF MAKING DIODE ARRAYS
3473094 - INTEGRATED ARRANGEMENT FOR INTEGRATED CIRCUIT STRUCTURES
3476617 - ASSEMBLY HAVING ADJACENT REGIONS OF DIFFERENT SEMICONDUCTOR MATERIAL ON AN INSULATOR SUBSTRATE AND METHOD OF MANUFACTURE
3477872 - METHOD OF DEPOSITING REFRACTORY METALS
3483038 - INTEGRATED ARRAY OF THIN-FILM PHOTOVOLTAIC CELLS AND METHOD OF MAKING SAME
3488835 - TRANSISTOR FABRICATION METHOD
3493812 - INTEGRATED THIN FILM TRANSLATORS
3500062 - DIGITAL LOGIC APPARATUS
3504239 - TRANSISTOR WITH DISTRIBUTED RESISTOR BETWEEN EMITTER LEAD AND EMITTER REGION
3510736 - INTEGRATED CIRCUIT PLANAR TRANSISTOR
3512058 - HIGH VOLTAGE TRANSIENT PROTECTION FOR AN INSULATED GATE FIELD EFFECT TRANSISTOR
3513022 - METHOD OF FABRICATING SEMICONDUCTOR DEVICES
3513364 - FIELD EFFECT TRANSISTOR WITH IMPROVED INSULATIVE LAYER BETWEEN GATE AND CHANNEL
3513403 - INTEGRATED SEMICONDUCTOR STRUCTURE WITH FREQUENCY SELECTIVE TRANSMISSION LINE SECTIONS
3513405 - FIELD-EFFECT TRANSISTOR AMPLIFIER
3516004 - SIGNAL TRANSLATING CIRCUIT COMPRISING A PLURALITY OF IGFET AMPLIFIERS CASCADED IN DIRECT COUPLED FASHION
3521128 - MICROMINIATURE ELECTRICAL COMPONENT HAVING INTEGRAL INDEXING MEANS
3521244 - ELECTRICAL CIRCUIT FOR PROCESSING PERIODIC SIGNAL PULSES
3543106 - MICROMINIATURE ELECTRICAL COMPONENT HAVING INDEXABLE RELIEF PATTERN
3544860 - INTEGRATED POWER OUTPUT CIRCUIT
3556966 - PLASMA ANODIZING ALUMINUM COATINGS ON A SEMICONDUCTOR

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

RCA CORPORATION (CONTINUED)

3558992 - INTEGRATED CIRCUIT HAVING BONDING PADS OVER UNUSED ACTIVE AREA COMPONENTS
3560357 - ELECTROETCHING OF A CONDUCTIVE FILM ON AN INSULATING SUBSTRATE
3582727 - HIGH VOLTAGE INTEGRATED CIRCUIT INCLUDING AN INVERSION CHANNEL
3586925 - GALLIUM ARSENIDE DIODES AND ARRAY OF DIODES
3588635 - INTEGRATED CIRCUIT
3604987 - RADIATION SENSING DEVICE COMPRISING AN ARRAY OF PHOTODIODES AND SWITCHING DEVICES IN A BODY OF SEMICONDUCTOR MATERIAL
3616348 - PROCESS FOR ISOLATING SEMICONDUCTOR ELEMENTS
3617823 - SELF-SCANNED PHOTOTRANSISTOR ARRAY EMPLOYING COMMON SUBSTRATE
3619725 - ELECTRICAL FUSE LINK
3622906 - LIGHT-EMITTING DIODE ARRAY
3623219 - METHOD FOR ISOLATING SEMICONDUCTOR DEVICES FROM A WAFER OF SEMICONDUCTING MATERIAL
3624419 - BALANCED
3628070 - VOLTAGE REFERENCE AND VOLTAGE LEVEL SENSING CIRCUIT
3631411 - ELECTRICALLY AND OPTICALLY ACCESSIBLE MEMORY
3636418 - EPITAXIAL SEMICONDUCTOR DEVICE HAVING ADHERENT BONDING PADS
3639787 - INTEGRATED BUFFER CIRCUITS FOR COUPLING LOW OUTPUT IMPEDANCE DRIVER TO HIGH INPUT IMPEDANCE LOAD
3644802 - RATIO-COMPENSATED RESISTORS FOR INTEGRATED CIRCUIT
3649887 - AC LINE OPERATION OF MONOLITHIC CIRCUIT
3658586 - EPITAXIAL SILICON ON HYDROGEN MAGNESIUM ALUMINATE SPINEL SINGLE CRYSTALS
3659334 - HIGH POWER HIGH FREQUENCY DEVICE
3660667 - IMAGE SENSOR ARRAY IN WHICH EACH ELEMENT EMPLOYS TWO PHOTOTRANSISTORS ONE OF WHICH STORES CHARGE
3668484 - SEMICONDUCTOR DEVICE WITH MULTI-LEVEL METALIZATION AND METHOD OF MAKING THE SAME
3673428 - INPUT TRANSIENT PROTECTION FOR COMPLEMENTARY INSULATED GATE FIELD EFFECT TRANSISTOR INTEGRATED CIRCUIT DEVICE
3674551 - FORMATION OF OPENINGS IN INSULATING LAYERS IN MOS SEMICONDUCTOR DEVICES
3676705 - LOGIC CIRCUITS EMPLOYING SWITCHES SUCH AS FIELD-EFFECT DEVICES
3695956 - METHOD FOR FORMING ISOLATED SEMICONDUCTOR DEVICES
3699395 - SEMICONDUCTOR DEVICE INCLUDING FUSIBLE ELEMENTS
3699403 - FUSIBLE SEMICONDUCTOR DEVICE INCLUDING MEANS FOR REDUCING THE REQUIRED FUSING CURRENT
3700507 - METHOD OF MAKING COMPLEMENTARY INSULATED GATE FIELD EFFECT TRANSISTORS
3702943 - FIELD-EFFECT TRANSISTOR CIRCUIT FOR DETECTING CHANGES IN VOLTAGE LEVEL
3703667 - SHAPED RISER ON SUBSTRATE STEP FOR PROMOTING METAL FILM CONTINUITY
3712995 - INPUT TRANSIENT PROTECTION FOR COMPLEMENTARY INSULATED GATE FIELD EFFECT TRANSISTOR INTEGRATED CIRCUIT DEVICE
3714521 - SEMICONDUCTOR DEVICE OR MONOLITHIC INTEGRATED CIRCUIT WITH TUNGSTEN INTERCONNECTIONS
3714709 - METHOD OF MANUFACTURING THICK-FILM HYBRID INTEGRATED CIRCUITS
3723833 - HEAT SINKING OF SEMICONDUCTOR INTEGRATED CIRCUIT DEVICES
3727072 - INPUT CIRCUIT FOR MULTIPLE EMITTER TRANSISTOR
3727116 - INTEGRAL THYRISTOR-RECTIFIER DEVICE
3728591 - GATE PROTECTIVE DEVICE FOR INSULATED GATE FIELD-EFFECT TRANSISTORS
3735210 - ZENER DIODE FOR MONOLITHIC INTEGRATED CIRCUITS
3740280 - METHOD OF MAKING SEMICONDUCTOR DEVICE
3740621 - TRANSISTOR EMPLOYING VARIABLE RESISTANCE BALLASTING MEANS DEPENDENT ON THE MAGNITUDE OF THE EMITTER CURRENT
3745072 - SEMICONDUCTOR DEVICE FABRICATION
3749614 - FABRICATION OF SEMICONDUCTOR DEVICES
3749984 - ELECTROACOUSTIC SEMICONDUCTOR DEVICE EMPLOYING AN IGFET
3749985 - HIGH FREQUENCY INSULATED GATE FIELD EFFECT TRANSISTOR FOR WIDE FREQUENCY BAND OPERATION
3751726 - SEMICONDUCTOR DEVICE EMPLOYING DARLINGTON CIRCUIT
3763480 - DIGITAL AND ANALOG DATA HANDLING DEVICES
3766637 - METHOD OF MAKING MOS TRANSISTORS
3789246 - INSULATED DUAL GATE FIELD-EFFECT TRANSISTOR SIGNAL TRANSLATOR HAVING MEANS FOR REDUCING ITS SENSITIVITY TO SUPPLY VOLTAG
E VARIATIONS
3791024. - FABRICATION OF MONOLITHIC INTEGRATED CIRCUITS
3801477 - METHOD OF DEPOSITING ELECTRODE LEADS
3811055 - CHARGE TRANSFER FAN-IN CIRCUITRY
3836995 - SEMICONDUCTOR DARLINGTON CIRCUIT
3836996 - SEMICONDUCTOR DARLINGTON CIRCUIT

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

RCA CORPORATION (CONTINUED)

3836997 - SEMICONDUCTOR DARLINGTON CIRCUIT
3837071 - METHOD OF SIMULTANEOUSLY MAKING A SIGFET AND A MOSFET
3863331 - MATCHING OF SEMICONDUCTOR DEVICE CHARACTERISTICS
3879640 - PROTECTIVE DIODE NETWORK FOR MOS DEVICES
3890632 - STABILIZED SEMICONDUCTOR DEVICES AND METHOD OF MAKING SAME
3898107 - METHOD OF MAKING A JUNCTION-ISOLATED SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE
3902188 - HIGH FREQUENCY TRANSISTOR
3904931 - OVERVOLTAGE PROTECTION CIRCUIT
3916430 - SYSTEM FOR ELIMINATING SUBSTRATE BIAS EFFECT IN FIELD EFFECT TRANSISTOR CIRCUITS
3916431 - BIPOLAR INTEGRATED CIRCUIT TRANSISTOR WITH LIGHTLY DOPED SUBCOLLECTOR CORE
3922703 - ELECTROLUMINESCENT SEMICONDUCTOR DEVICE
3931634 - JUNCTION-ISOLATED MONOLITHIC INTEGRATED CIRCUIT DEVICE WITH MEANS FOR PREVENTING PARASITIC TRANSISTOR ACTION
3936863 - INTEGRATED POWER TRANSISTOR WITH BALLASTING RESISTANCE AND BREAKDOWN PROTECTION
3941940 - TRANSIENT SUPPRESSOR
3943551 - LSI ARRAY USING FIELD EFFECT TRANSISTORS OF DIFFERENT CONDUCTIVITY TYPE
3943555 - SOS BIPOLAR TRANSISTOR
3956820 - METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE HAVING A LEAD BONDED TO A SURFACE THEREOF
3958266 - DEEP DEPLETION INSULATED GATE FIELD EFFECT TRANSISTORS
3967295 - INPUT TRANSIENT PROTECTION FOR INTEGRATED CIRCUIT ELEMENT
3974515 - IGFET ON AN INSULATING SUBSTRATE
3974560 - METHOD OF MAKING A BIPOLAR TRANSISTOR
3978508 - PRESSURE SENSITIVE FIELD EFFECT DEVICE
3980507 - METHOD OF MAKING A SEMICONDUCTOR DEVICE
3990099 - PLANAR TRAPATT DIODE
3999205 - RECTIFIER STRUCTURE FOR A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE
4007297 - METHOD OF TREATING SEMICONDUCTOR DEVICE TO IMPROVE ITS ELECTRICAL CHARACTERISTICS
4015279 - EDGELESS TRANSISTOR
4016016 - METHOD OF SIMULTANEOUSLY FORMING A POLYCRYSTALLINE SILICON GATE AND A SINGLE CRYSTAL EXTENSION OF SAID GATE IN SILICON O N SAPPHIRE MOS DEVICES
4017882 - TRANSISTOR HAVING INTEGRATED PROTECTION
4034239 - CAPACITANCE MEMORIES OPERATED WITH INTERMITTENTLY-ENERGIZED INTEGRATED CIRCUITS
4034399 - INTERCONNECTION MEANS FOR AN ARRAY OF MAJORITY CARRIER MICROWAVE DEVICES
4035826 - REDUCTION OF PARASITIC BIPOLAR EFFECTS IN INTEGRATED CIRCUITS EMPLOYING INSULATED GATE FIELD EFFECT TRANSISTORS VIA THE USE OF LOW RESISTANCE SUBSTRATE CONTACTS EXTENDING THROUGH SOURCE REGION
4035827 - THERMALLY BALLASTED SEMICONDUCTOR DEVICE
4035828 - SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE
4035829 - SEMICONDUCTOR DEVICE AND METHOD OF ELECTRICALLY ISOLATING CIRCUIT COMPONENTS THEREON
4039857 - DYNAMIC BIASING OF ISOLATION BOAT INCLUDING DIFFUSED RESISTORS
4039869 - PROTECTION CIRCUIT
4045250 - METHOD OF MAKING A SEMICONDUCTOR DEVICE
4045811 - SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE INCLUDING AN ARRAY OF INSULATED GATE FIELD EFFECT TRANSISTORS
4051391 - CURRENT-OPERATED CIRCUITS AND STRUCTURES
4054894 - EDGELESS TRANSISTOR
4054895 - SILICON-ON-SAPPHIRE MESA TRANSISTOR HAVING DOPED EDGES
4057763 - CURRENT AMPLIFIERS
4057894 - CONTROLLABLY VALUED RESISTOR
4063274 - INTEGRATED CIRCUIT DEVICE INCLUDING BOTH N-CHANNEL AND P-CHANNEL INSULATED GATE FIELD EFFECT TRANSISTORS
4063277 - SEMICONDUCTOR THYRISTOR DEVICES HAVING BREAKOVER PROTECTION
4066918 - PROTECTION CIRCUITRY FOR INSULATED-GATE FIELD-EFFECT TRANSISTOR (IGFET) CIRCUITS
4072974 - SILICON RESISTIVE DEVICE FOR INTEGRATED CIRCUITS
4094582 - LIQUID CRYSTAL MATRIX DISPLAY DEVICE WITH TRANSISTORS
4097314 - METHOD OF MAKING A SAPPHIRE GATE TRANSISTOR
4100561 - PROTECTIVE CIRCUIT FOR MOS DEVICES
4100565 - MONOLITHIC RESISTOR FOR COMPENSATING BETA OF A LATERAL TRANSISTOR
4106048 - INTEGRATED CIRCUIT PROTECTION DEVICE COMPRISING DIODE HAVING LARGE CONTACT AREA IN SHUNT WITH PROTECTED BIPOLAR TRANSIST OR

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

RCA CORPORATION (CONTINUED)
4113516 - METHOD OF FORMING A CURVED IMPLANTED REGION IN A SEMICONDUCTOR BODY
4119992 - INTEGRATED CIRCUIT STRUCTURE AND METHOD FOR MAKING SAME
4122483 - SEMICONDUCTOR DEVICE HAVING REDUCED LEAKAGE CURRENT
4126879 - SEMICONDUCTOR DEVICE WITH BALLAST RESISTOR ADAPTED FOR A TRANSCALENT DEVICE
4127860 - INTEGRATED CIRCUIT MESA BIPOLAR DEVICE ON INSULATING SUBSTRATE INCORPORATING SCHOTTKY BARRIER CONTACT
4131496 - METHOD OF MAKING SILICON ON SAPPHIRE FIELD EFFECT TRANSISTORS WITH SPECIFICALLY ALIGNED GATES
4136353 - BIPOLAR TRANSISTOR WITH HIGH-LOW EMITTER IMPURITY CONCENTRATION
4137545 - GATE TURN-OFF THYRISTOR WITH ANODE RECTIFYING CONTACT TO NON-REGENERATIVE SECTION
4142197 - DRAIN EXTENSIONS FOR CLOSED COS/MOS LOGIC DEVICES
4159561 - METHOD OF MAKING A SUBSTRATE CONTACT FOR AN INTEGRATED CIRCUIT
4169746 - METHOD FOR MAKING SILICON ON SAPPHIRE TRANSISTOR UTILIZING PREDEPOSITION OF LEADS
4170501 - METHOD OF MAKING A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE UTILIZING SIMULTANEOUS OUTDIFFUSION AND AUTODOPING DURING EPI TAXIAL DEPOSITION
4178191 - PROCESS OF MAKING A PLANAR MOS SILICON-ON-INSULATING SUBSTRATE DEVICE
4178605 - COMPLEMENTARY MOS INVERTER STRUCTURE

RESEARCH CORPORATION
4084175 - DOUBLE IMPLANTED PLANAR MOS DEVICE WITH V-GROOVE AND PROCESS OF MANUFACTURE THEREOF

RICOH CO., LTD.
3761259 - ELECTROPHOTOGRAPHIC ELEMENT CONTAINING AN INTERMEDIATE LAYER

ROBERT BOSCH GMBH
3596115 - INTEGRATED MONOLITHIC SEMICONDUCTOR VOLTAGE REGULATOR ARRANGEMENT
3596150 - MONOLITHIC TRANSISTOR CIRCUIT
4004160 - SWITCHING SYSTEM TO SHORT-CIRCUIT A LOAD WITH MINIMUM RESIDUAL VOLTAGE
4024418 - INTEGRATED CIRCUIT CMOS INVERTER STRUCTURE
4028564 - COMPENSATED MONOLITHIC INTEGRATED CURRENT SOURCE
4038677 - COMPOSITE SEMICONDUCTOR UNIT AND METHOD
4054898 - SWITCHING SYSTEM TO SHORT-CIRCUIT A LOAD WITH MINIMUM RESIDUAL VOLTAGE
4104546 - INTEGRATED CIRCUIT FOR USE WITH VARIABLE VOLTAGES

ROCKWELL INTERNATIONAL CORPORATION
3484662 - THIN FILM TRANSISTOR ON AN INSULATING SUBSTRATE
3514676 - INSULATED GATE COMPLEMENTARY FIELD EFFECT TRANSISTORS GATE STRUCTURE
3584183 - LASER ENCODING OF DIODE ARRAYS
3591836 - FIELD EFFECT CONDITIONALLY SWITCHED CAPACITOR
3631261 - COMPACT LAYOUT FOR MULTIPHASE SHIFT REGISTER
3665473 - ADDRESS DECODE LOGIC FOR A SEMICONDUCTOR MEMORY
3698966 - PROCESSES USING A MASKING LAYER FOR PRODUCING FIELD EFFECT DEVICES HAVING OXIDE ISOLATION
3743552 - PROCESS FOR COPLANAR SEMICONDUCTOR STRUCTURE
3794862 - SUBSTRATE BIAS CIRCUIT
3969753 - SILICON ON SAPPHIRE ORIENTED FOR MAXIMUM MOBILITY
4002501 - HIGH SPEED, HIGH YIELD CMOS/SOS PROCESS
4047216 - HIGH SPEED LOW CAPACITANCE CHARGE COUPLED DEVICE IN SILICON-SAPPHIRE
4139401 - METHOD OF PRODUCING ELECTRICALLY ISOLATED SEMICONDUCTOR DEVICES ON COMMON CRYSTALLINE SUBSTRATE

RUCKER COMPANY
3865066 - TENSION MOORING DEVICE

SANYO ELECTRIC CO., LTD.
4004159 - ELECTRICALLY REPROGRAMMABLE NONVOLATILE FLOATING GATE SEMI-CONDUCTOR MEMORY DEVICE AND METHOD OF OPERATION

SCIENTIFIC DATA SYSTEMS
3510735 - TRANSISTOR WITH INTEGRAL PINCH RESISTOR

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

SCIENTIFIC MICRO SYSTEMS, INC.
3796612 - SEMICONDUCTOR ISOLATION METHOD UTILIZING ANISOTROPIC ETCHING AND DIFFERENTIAL THERMAL OXIDATION
4047195 - SEMICONDUCTOR STRUCTURE

SEMICONDUCTORS ELECTRONIC MEMORIES, INCORPORATED
3631309 - INTEGRATED CIRCUIT BIPOLAR MEMORY CELL

SEMIKRON GESELLSCHAFT FOR GLEICHRICHTERBAU UND ELEKTRONID M.
3673468 - SEMICONDUCTOR RECTIFYING ARRANGEMENT

SENSOR TECHNOLOGY, INC.
3925879 - PROCESS OF FABRICATING PHOTOSENSITIVE DARLINGTON DEVICE
3995308 - PHOTOSENSITIVE DARLINGTON DEVICE AND PROCESS OF FABRICATING SAME
4081820 - COMPLEMENTARY PHOTOVOLTAIC CELL

SESCOSEM-SOCIETE EUROPEENE DE SEMICONDUCTEURS ET DE MICROELE
3761784 - SEMI-CONDUCTOR STRAIN GAUGE DEVICE WITH FIELD EFFECT TRANSISTOR SYMMETRICAL PAIRS

SGS ATES COMPONENTI ELETTRONICI SPA
4072979 - INTEGRATED POWER AMPLIFIER
4117507 - DIODE FORMED IN INTEGRATED-CIRCUIT STRUCTURE
4157513 - PROTECTIVE SYSTEM FOR POWER STAGE OF MONOLITHIC CIRCUITRY

SHARP KABUSHIKI KAISHA
4058822 - HIGH VOLTAGE, LOW ON-RESISTANCE DIFFUSION-SELF-ALIGNMENT METAL OXIDE SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF
4115796 - COMPLEMENTARY-MOS INTEGRATED SEMICONDUCTOR DEVICE
4144106 - MANUFACTURE OF AN I+HU 2+B DEVICE UTILIZING STAGED SELECTIVE DIFFUSION THRU A POLYCRYSTALLINE MASK

SHELL OIL COMPANY
3533089 - SINGLE-RAIL MOSFET MEMORY WITH CAPACITIVE STORAGE
3577005 - TRANSISTOR INVERTER CIRCUIT
3614753 - SINGLE-RAIL SOLID STATE MEMORY WITH CAPACITIVE STORAGE
3686644 - GATED DIODE MEMORY
3699537 - SINGLE-RAIL MOSFET MEMORY WITH CAPACITIVE STORAGE

SIEMENS AKTIENGESELLSCHAFT
3421103 - SEMICONDUCTOR INTEGRATED TRANSISTOR CASCADE FOR AMPLIFYING PURPOSES
3424955 - METHOD FOR EPITAXIAL PRECIPITATION OF SEMICONDUC- TOR MATERIAL UPON A SPINEL-TYPE LATTICE SUBSTRATE
3445927 - METHOD OF MANUFACTURING INTEGRATED SEMICONDUCTOR CIRCUIT DEVICE
3453505 - INTEGRATED COMPLEMENTARY TRANSISTOR CIRCUIT
3466741 - METHOD OF PRODUCING INTEGRATED CIRCUITS AND THE LIKE
3477885 - METHOD FOR PRODUCING A STRUCTURE COMPOSED OF MUTUALLY INSULATED SEMICONDUCTOR REGIONS FOR INTEGRATED CIRCUITS
3487272 - VOLTAGE DEPENDENT SEMICONDUCTOR CAPACITOR OF MESA
3502516 - METHOD FOR PRODUCING PURE SEMICONDUCTOR MATERIAL FOR ELECTRONIC PURPOSES
3564358 - INTEGRATED CIRCUIT STRUCTURE CONTAINING MULTIPLE SANDWICH LAYERS OF MONO-CRYSTALLINE SEMICONDUCTOR AND INSULATOR MATERIA L
3636358 - INTEGRATED OPTICAL-ELECTRONIC SOLID STATE SYSTEM HAVING TWO SUPERIMPOSED CIRCUIT PLANES LINKED BY OPTICAL AND/OR ELECTRO NIC AND HORIZONTAL AND/OR VERTICAL CONNECTIONS
3655439 - METHOD OF PRODUCING THIN LAYER COMPONENTS WITH AT LEAST ONE INSULATING INTERMEDIATE LAYER
3674552 - METHOD OF PRODUCING SEMICONDUCTOR COMPONENTS ON A MAGNETIC SUBSTRATE
3707657 - TARGET STRUCTURE FOR VIDICON TUBE AND METHODS OF PRODUCING THE SAME
3713008 - SEMICONDUCTOR DEVICES HAVING AT LEAST FOUR REGIONS OF ALTERNATELY DIFFERENT CONDUCTANCE TYPE
3716804 - INTEGRATED OPTICAL-ELECTRONIC SOLID STATE SYSTEM
3760240 - LIGHT-SENSITIVE SEMICONDUCTOR DEVICE
3774170 - FIXED DATA MEMORY UTILIZING SCHOTTKY DIODES
3781825 - PROGRAMMABLE FIXED DATA MEMORY UTILIZING SCHOTTKY DIODES

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

SIEMENS AKTIENGESELLSCHAFT (CONTINUED)

3798080 - METHOD OF PRODUCING A SEMICONDUCTOR COMPONENT
3810049 - INTEGRATED ATTENUATION ELEMENTS
3810125 - INTEGRATED CIRCUIT ELECTRICAL CAPACITOR, PARTICULARLY AS A STORAGE ELEMENT FOR SEMICONDUCTOR MEMORIES
3846192 - METHOD OF PRODUCING SCHOTTKY DIODES
3859716 - PRODUCTION OF THIN LAYER COMPLEMENTARY CHANNEL MOS CIRCUITS
3885998 - METHOD FOR THE SIMULTANEOUS FORMATION OF SEMICONDUCTOR COMPONENTS WITH INDIVIDUALLY TAILORED ISOLATION REGIONS
3889358 - PROCESS FOR THE PRODUCTION OF HIGH VALUE OHMIC LOAD RESISTORS AND MOS TRANSISTORS HAVING A LOW STARTING VOLTAGE
3919765 - METHOD FOR THE PRODUCTION OF INTEGRATED CIRCUITS WITH COMPLEMENTARY CHANNEL FIELD EFFECT TRANSISTORS
3919766 - METHOD FOR THE PRODUCTION OF INTEGRATED CIRCUITS WITH FIELD EFFECT TRANSISTORS OF VARIABLE LINE CONDITION
3933529 - PROCESS FOR THE PRODUCTION OF A PAIR OF COMPLEMENTARY FIELD EFFECT TRANSISTORS
3939555 - STRIP TYPE RADIATION DETECTOR AND METHOD OF MAKING SAME
3949275 - ELECTRIC THIN-FILM CIRCUIT AND METHOD FOR ITS PRODUCTION
3956667 - LUMINOUS DISCHARGE DISPLAY DEVICE
3975718 - SEMICONDUCTOR ARRANGEMENT, PARTICULARLY A STORAGE ARRANGEMENT WITH FIELD EFFECT TRANSISTORS, AND METHOD OF OPERATING THE SAME
3997411 - METHOD FOR THE PRODUCTION OF A THIN FILM ELECTRIC CIRCUIT
3997908 - SCHOTTKY GATE FIELD EFFECT TRANSISTOR
4001465 - PROCESS FOR PRODUCING SEMICONDUCTOR DEVICES
4017769 - INTEGRATED CIRCUITS AND METHOD OF PRODUCING THE SAME
4029527 - METHOD OF PRODUCING A DOPED ZONE OF A GIVEN CONDUCTIVITY TYPE IN A SEMICONDUCTOR BODY
4032947 - CONTROLLABLE CHARGE-COUPLED SEMICONDUCTOR DEVICE
4038676 - PAIR OF BIPOLAR TRANSISTORS HAVING BASE ZONES WHICH ARE ELECTRICALLY CONDUCTIVELY CONNECTED TO ONE ANOTHER, AND A PROCESS FOR PRODUCING THE PAIR OF TRANSISTORS
4040082 - STORAGE ARRANGEMENT COMPRISING TWO COMPLEMENTARY FIELD-EFFECT TRANSISTORS
4047975 - PROCESS FOR THE PRODUCTION OF A BIPOLAR INTEGRATED CIRCUIT
4048517 - LOGIC ELEMENT
4055837 - DYNAMIC SINGLE-TRANSISTOR MEMORY ELEMENT FOR RELATIVELY PERMANENT MEMORIES
4063273 - FUNDAMENTAL LOGIC CIRCUIT
4064491 - INFORMATION MEMORY FOR STORING INFORMATION IN THE FORM OF ELECTRIC CHARGE CARRIERS AND METHOD OF OPERATING THEREOF
4072982 - SEMICONDUCTOR COMPONENT WITH DIELECTRIC CARRIER AND ITS MANUFACTURE
4082571 - PROCESS FOR SUPPRESSING PARASITIC COMPONENTS UTILIZING ION IMPLANTATION PRIOR TO EPITAXIAL DEPOSITION
4085339 - CIRCUIT ARRANGEMENT IN A COMPLEMENTARY CHL TECHNIQUE
4086612 - THYRISTOR
4107719 - INVERSE PLANAR TRANSISTOR
4109270 - SEMICONDUCTOR STORE
4109272 - LATERAL BIPOLAR TRANSISTOR
4109273 - CONTACT ELECTRODE FOR SEMICONDUCTOR COMPONENT
4110779 - HIGH FREQUENCY TRANSISTOR
4126881 - SEMICONDUCTOR MEMORY
4131806 - I.I.L. WITH INJECTOR BASE RESISTOR AND SCHOTTKY CLAMP
4143455 - METHOD OF PRODUCING A SEMICONDUCTOR COMPONENT
4148044 -
4150389 - N-CHANNEL MEMORY FIELD EFFECT TRANSISTOR
4163242 - MOS STORAGE INTEGRATED CIRCUIT USING INDIVIDUAL FET ELEMENTS
4178603 - SCHOTTKY TRANSISTOR WITH LOW RESIDUAL VOLTAGE

SIEMENS CORPORATION

4075649 - SINGLE CHIP TEMPERATURE COMPENSATED REFERENCE DIODE AND METHOD FOR MAKING SAME

SIGNETICS CORPORATION

3518494 - RADIATION RESISTANT SEMICONDUCTOR DEVICE AND METHOD
3564354 - SEMICONDUCTOR STRUCTURE WITH FUSIBLE LINK AND METHOD
3564434 - INTEGRATED FREQUENCY SELECTIVE CIRCUIT AND DEMODULATOR INCLUDING PHASE LOCKED LOOP
3566219 - PINCHED RESISTOR SEMICONDUCTOR STRUCTURE
3619739 - BULK RESISTOR AND INTEGRATED CIRCUIT USING THE SAME

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

SIGNETICS CORPORATION (CONTINUED)

3623218 - METHOD FOR DETERMINING DEPTH OF LAPPING OF DIELECTRICALLY ISOLATED INTEGRATED CIRCUITS
3628064 - VOLTAGE TO FREQUENCY CONVERTER WITH CONSTANT CURRENT SOURCES
3660732 - SEMICONDUCTOR STRUCTURE WITH DIELECTRIC AND AIR ISOLATION AND METHOD
3663223 - PROCESS FOR MAKING INTEGRATED CIRCUIT MASKS
3676742 - MEANS INCLUDING A SPARK GAP FOR PROTECTING AN INTEGRATED CIRCUIT FROM ELECTRICAL DISCHARGE
3696274 - AIR ISOLATED INTEGRATED CIRCUIT AND METHOD
3703650 - INTEGRATED CIRCUIT WITH TEMPERATURE COMPENSATION FOR A FIELD EFFECT TRANSISTOR
3711753 - ENHANCEMENT MODE N-CHANNEL MOS STRUCTURE AND METHOD
3748546 - PHOTOSENSITIVE DEVICE AND ARRAY
3758797 - SOLID STATE BISTABLE SWITCHING DEVICE AND METHOD
3761782 - SEMICONDUCTOR STRUCTURE, ASSEMBLY AND METHOD
3767981 - HIGH VOLTAGE PLANAR DIODE STRUCTURE AND METHOD
3778886 - SEMICONDUCTOR STRUCTURE WITH FUSIBLE LINK AND METHOD
3818583 - METHOD FOR FABRICATING SEMICONDUCTOR STRUCTURE HAVING COMPLEMENTARY DEVICES
3829889 - SEMICONDUCTOR STRUCTURE
3836998 - HIGH VOLTAGE BIPOLAR SEMICONDUCTOR DEVICE AND INTEGRATED CIRCUIT USING THE SAME AND METHOD
3845495 - HIGH VOLTAGE, HIGH FREQUENCY DOUBLE DIFFUSED METAL OXIDE SEMICONDUCTOR DEVICE
3852802 - INTEGRATED CIRCUIT HALL EFFECT DEVICE AND METHOD
3855612 - SCHOTTKY BARRIER DIODE SEMICONDUCTOR STRUCTURE AND METHOD
3869321 - METHOD FOR FABRICATING PRECISION LAYER SILICON-OVER-OXIDE SEMICONDUCTOR STRUCTURE
3877050 - INTEGRATED CIRCUIT HAVING GUARD RING SCHOTTKY BARRIER DIODE AND METHOD
3883948 - SEMICONDUCTOR STRUCTURE AND METHOD
3895392 - BIPOLAR TRANSISTOR STRUCTURE HAVING ION IMPLANTED REGION AND METHOD
3911562 - METHOD OF CHEMICAL POLISHING OF PLANAR SILICON STRUCTURES HAVING FILLED GROOVES THEREIN
3913121 - SEMICONDUCTOR STRUCTURE
3918079 - ENCAPSULATED BEAM LEAD CONSTRUCTION FOR SEMICONDUCTOR DEVICE AND ASSEMBLY AND METHOD
3920482 - METHOD FOR FORMING A SEMICONDUCTOR STRUCTURE HAVING ISLANDS ISOLATED BY ADJACENT MOATS
3926694 - DOUBLE DIFFUSED METAL OXIDE SEMICONDUCTOR STRUCTURE WITH ISOLATED SOURCE AND DRAIN AND METHOD
3940783 - MAJORITY CARRIERS-VARIABLE THRESHOLD RECTIFIER AND/OR VOLTAGE REFERENCE SEMICONDUCTOR STRUCTURE
3943554 - THRESHOLD SWITCHING INTEGRATED CIRCUIT AND METHOD FOR FORMING THE SAME
3947865 - COLLECTOR-UP SEMICONDUCTOR CIRCUIT STRUCTURE FOR BINARY LOGIC
3947866 - ION IMPLANTED RESISTOR HAVING CONTROLLED TEMPERATURE COEFFICIENT AND METHOD
3953866 - CROSS COUPLED SEMICONDUCTOR MEMORY CELL
3976512 - METHOD FOR REDUCING THE DEFECT DENSITY OF AN INTEGRATED CIRCUIT UTILIZING ION IMPLANTATION
3979765 - SILICON GATE MOS DEVICE AND METHOD
3986200 - SEMICONDUCTOR STRUCTURE AND METHOD
4001860 - DOUBLE DIFFUSED METAL OXIDE SEMICONDUCTOR STRUCTURE WITH ISOLATED SOURCE AND DRAIN AND METHOD
4003076 - SINGLE BIPOLAR TRANSISTOR MEMORY CELL AND METHOD
4005470 - TRIPLE DIFFUSED LOGIC ELEMENTS
4018627 - METHOD FOR FABRICATING SEMICONDUCTOR DEVICES UTILIZING OXIDE PROTECTIVE LAYER
4065680 - COLLECTOR-UP LOGIC TRANSMISSION GATES
4081822 - THRESHOLD INTEGRATED INJECTION LOGIC
4097888 - HIGH DENSITY COLLECTOR-UP STRUCTURE
4112511 - FOUR TRANSISTOR STATIC BIPOLAR MEMORY CELL USING MERGED TRANSISTORS
4122540 - MASSIVE MONOLITHIC INTEGRATED CIRCUIT
4143392 - COMPOSITE JFET-BIPOLAR STRUCTURE
4151635 - METHOD FOR MAKING A COMPLEMENTARY SILICON GATE MOS STRUCTURE
4160988 - INTEGRATED INJECTION LOGIC (I-SQUARED L) WITH DOUBLE-DIFFUSED TYPE INJECTOR

SILEC-SEMI-CONDUCTEURS

3970843 - PHOTOSENSITIVE JUNCTION DEVICES HAVING CONTROLLABLE SENSITIVITY

SILICONIX INCORPORATED

3708694 - VOLTAGE LIMITER
4161417 - METHOD OF MAKING CMOS STRUCTURE WITH RETARDED ELECTRIC FIELD FOR MINIMUM LATCH-UP

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

SINGER COMPANY
3486045 - REFERENCING ARRANGEMENT
3502951 - MONOLITHIC COMPLEMENTARY SEMICONDUCTOR DEVICE

SMC MICROSYSTEMS CORPORATION
3867196 - METHOD FOR SELECTIVELY ESTABLISHING REGIONS OF DIFFERENT SURFACE CHARGE DENSITIES IN A SILICON WAFER
4023195 - MOS FIELD-EFFECT TRANSISTOR STRUCTURE WITH MESA-LIKE CONTACT AND GATE AREAS AND SELECTIVELY DEEPER JUNCTIONS

SOCIETE EUROPEENNE DE SEMICONDUCTEURS ET DE
3715637 - LOGIC CIRCUITS EMPLOYING COMPLEMENTARY FIELD-EFFECT TRANSISTORS IN WHICH THE GATE IS INSULATED FROM THE SUBSTRATE

SOLID STATE SCIENTIFIC, INC.
4124807 - BISTABLE SEMICONDUCTOR FLIP-FLOP HAVING A HIGH RESISTANCE FEEDBACK

SONY CORPORATION
3471754 - ISOLATION STRUCTURE FOR INTEGRATED CIRCUIT
3475661 - SEMICONDUCTOR DEVICE INCLUDING POLYCRYSTALLINE AREAS AMONG MONOCRYSTALLINE AREAS
3492174 - METHOD OF MAKING A SEMICONDUCTOR DEVICE
3519899 - MAGNETO-RESISTANCE ELEMENT
3575731 - METHODS OF MANUFACTURING SEMICONDUCTOR DEVICES
3607466 - METHOD OF MAKING SEMICONDUCTOR WAFER
3617822 - SEMICONDUCTOR INTEGRATED CIRCUIT
3617826 - INTEGRATED TRANSISTOR WITH A POLYCRYSTALLINE CONTACT TO A BURIED COLLECTOR REGION
3648128 - INTEGRATED COMPLEMENTARY TRANSISTOR CIRCUIT CHIP WITH POLYCRYSTALLINE CONTACT TO BURIED COLLECTOR REGIONS
3651385 - SEMICONDUCTOR DEVICE INCLUDING A POLYCRYSTALLINE DIODE
3681668 - SEMICONDUCTOR DEVICE AND A METHOD OF MAKING THE SAME
3692574 - METHOD OF FORMING SEEDING SITES ON A SEMICONDUCTOR SUBSTRATE
3694276 - METHOD OF MAKING INTEGRATED CIRCUITS EMPLOYING SELECTIVE GOLD DIFFUSION THRU POLYCRYSTALLINE REGIONS
3694704 - SEMICONDUCTOR DEVICE
3725751 - SOLID STATE TARGET ELECTRODE FOR PICKUP TUBES
3754170 - INTEGRATED CIRCUIT DEVICE HAVING MONOLITHIC RF SHIELDS
3775196 - METHOD OF SELECTIVELY DIFFUSING CARRIER KILLERS INTO INTEGRATED CIRCUITS UTILIZING POLYCRYSTALLINE REGIONS
3806773 - FIELD EFFECT TRANSISTOR HAVING BACK-TO-BACK DIODES CONNECTED TO THE GATE ELECTRODE AND HAVING A PROTECTIVE LAYER BETWEEN THE SOURCE AND THE DIODES
3812517 - CONTINUOUSLY VARIABLE THRESHOLD TRANSISTOR
3868718 - FIELD EFFECT TRANSISTOR HAVING A PAIR OF GATE REGIONS
3871007 - SEMICONDUCTOR INTEGRATED CIRCUIT
3875567 - MEMORY CIRCUIT USING VARIABLE THRESHOLD LEVEL FIELD-EFFECT DEVICE
3877060 - SEMICONDUCTOR DEVICE HAVING AN INSULATING LAYER OF BORON PHOSPHIDE AND METHOD OF MAKING THE SAME
3882409 - DIFFERENTIAL AMPLIFIER CIRCUIT
3886458 - FREQUENCY CONVERTER CIRCUIT WITH INTEGRATED INJECTION CAPACITOR
3899793 - INTEGRATED CIRCUIT WITH CARRIER KILLER SELECTIVELY DIFFUSED THEREIN AND METHOD OF MAKING SAME
3900747 - DIGITAL CIRCUIT FOR AMPLIFYING A SIGNAL
3912555 - SEMICONDUCTOR INTEGRATED CIRCUIT AND METHOD FOR MANUFACTURING THE SAME
3925803 - ORIENTED POLYCRYSTAL JFET
3968452 - SIGNAL LEVEL CONTROL CIRCUIT
3968511 - SEMICONDUCTOR DEVICE WITH ADDITIONAL CARRIER INJECTING JUNCTION ADJACENT EMITTER REGION
3969747 - COMPLEMENTARY BIPOLAR TRANSISTORS WITH IIL TYPE COMMON BASE DRIVERS
3977019 - SEMICONDUCTOR INTEGRATED CIRCUIT
3979764 - CONTROLLED FADING SWITCHING CIRCUIT
3979766 - SEMICONDUCTOR DEVICE
3986195 - LIGHT RESPONSIVE FIELD EFFECT TRANSISTOR HAVING A PAIR OF GATE REGIONS
3988761 - FIELD-EFFECT TRANSISTOR AND METHOD OF MAKING THE SAME
4001762 - THIN FILM RESISTOR
4007474 - TRANSISTOR HAVING AN EMITTER WITH A LOW IMPURITY CONCENTRATION PORTION AND A HIGH IMPURITY CONCENTRATION PORTION
4007478 - FIELD EFFECT TRANSISTOR

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

SONY CORPORATION (CONTINUED)

4012762 - SEMICONDUCTOR FIELD EFFECT DEVICE HAVING OXYGEN ENRICHED POLYCRYSTALLINE SILICON
4027324 - BIDIRECTIONAL TRANSISTOR
4032953 - SENSING CIRCUITS
4032956 - TRANSISTOR CIRCUIT
4032957 - SEMICONDUCTOR DEVICE
4032958 - SEMICONDUCTOR DEVICE
4035824 - SEMICONDUCTOR DEVICE STABILIZED BY AN INSULATING LAYER FORMED ON A SEMICONDUCTOR REGION HAVING A LOW IMPURITY CONCENTRATION
4038680 - SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE
4072975 - INSULATED GATE FIELD EFFECT TRANSISTOR
4141023 - FIELD EFFECT TRANSISTOR HAVING A LINEAR ATTENUATION CHARACTERISTIC AND AN IMPROVED DISTORTION FACTOR WITH MULTIPLE GATE DRAIN CONTACTS
4157557 - CONTROL CIRCUIT FOR SIGNAL TRANSMISSION
4176372 - SEMICONDUCTOR DEVICE HAVING OXYGEN DOPED POLYCRYSTALLINE PASSIVATION LAYER

SPERRY RAND CORPORATION

3423646 - COMPUTER LOGIC DEVICE CONSISTING OF AN ARRAY OF TUNNELING DIODES, ISOLATORS AND SHORT CIRCUITS
3431438 - OPTICAL COMPUTER COMPRISING SEMICONDUCTOR P-N JUNCTION COMPONENTS
3691535 - SOLID STATE MEMORY ARRAY
3786316 - HIGH FREQUENCY DIODE ENERGY TRANSDUCER AND METHOD OF MANUFACTURE
3971001 - REPROGRAMMABLE READ ONLY VARIABLE THRESHOLD TRANSISTOR MEMORY WITH ISOLATED ADDRESSING BUFFER
4142112 - SINGLE ACTIVE ELEMENT CONTROLLED-INVERSION SEMICONDUCTOR STORAGE CELL DEVICES AND STORAGE MATRICES EMPLOYING SAME

SPRAGUE ELECTRIC COMPANY

3421936 - SILICON NITRIDE COATING ON SEMICONDUCTOR AND METHOD
3426254 - TRANSISTORS AND METHOD OF MANUFACTURING THE SAME
3471753 - SEMICONDUCTOR MOUNTING CHIP ASSEMBLY
3482149 - SINTERED GLASS INTEGRATED CIRCUIT STRUCTURE PRODUCT AND METHOD OF MAKING THE SAME
3504203 - TRANSISTOR WITH COMPENSATED DEPLETION-LAYER CAPACITANCE
3560866 - IF AMPLIFIER WITH COMPENSATED TRANSISTOR UNIT
3564355 - SEMICONDUCTOR DEVICE EMPLOYING A P-N JUNCTION BETWEEN INDUCED P- AND N- REGIONS
3585462 - SEMICONDUCTIVE MAGNETIC TRANSDUCER
3615873 - METHOD OF STABILIZING MOS DEVICES
3628046 - DOUBLE BALANCED
3660735 - COMPLEMENTARY METAL INSULATOR SILICON TRANSISTOR PAIRS
3755026 - METHOD OF MAKING A SEMICONDUCTOR DEVICE HAVING TUNNEL OXIDE CONTACTS
3816766 - INTERGRATED CIRCUIT WITH HALL CELL
3864817 - METHOD OF MAKING CAPACITOR AND RESISTOR FOR MONOLITHIC INTEGRATED CIRCUITS
3872491 - ASYMMETRICAL DUAL-GATE FET
3940785 - SEMICONDUCTOR I.C. WITH PROTECTION AGAINST REVERSED POWER SUPPLY
4001869 - MOS-CAPACITOR FOR INTEGRATED CIRCUITS
4027325 - INTEGRATED FULL WAVE DIODE BRIDGE RECTIFIER
4107762 - SOLID ELECTROLYTE CAPACITOR PACKAGE WITH AN EXOTHERMICALLY-ALLOYABLE FUSE

STANDARD MICROSYSTEMS CORPORATION

3751722 - MOS INTEGRATED CIRCUIT WITH SUBSTRATE CONTAINING SELECTIVELY FORMED RESISTIVITY REGIONS

TEKTRONIX INC.

3524998 - RESISTIVE CONVERSION DEVICE
3538399 - PN JUNCTION GATED FIELD EFFECT TRANSISTOR HAVING BURIED LAYER OF LOW RESISTIVITY
3564356 - HIGH VOLTAGE INTEGRATED CIRCUIT TRANSISTOR
3587052 - TRANSISTOR MATRIX
3594241 - MONOLITHIC INTEGRATED CIRCUIT INCLUDING FIELD EFFECT TRANSISTORS AND BIPOLAR TRANSISTORS, AND METHOD OF MAKING
3697785 - SOLID STATE SCANNING DEVICE
3708691 - LARGE SCALE INTEGRATED CIRCUIT OF REDUCED AREA INCLUDING COUNTER

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

TELEDYNE INDUSTRIES, INC.
3432792 - ISOLATED RESISTOR FOR INTEGRATED CIRCUIT
3442003 - METHOD FOR INTERCONNECTING THIN FILMS
3456166 - JUNCTION CAPACITOR
3517278 - SLIP CHIP STRUCTURE
3748499 - VOLTAGE VARIABLE NON-INDUCTION PHASE SHIFTER WITH MONOLITHIC IMPLEMENTATION
3995304 - D/A BIT SWITCH

TELEFONAKTIEBOLAGET LM ERICSSON
3860465 - METHOD FOR OBTAINING AN ACCURATELY DETERMINED HIGH RESISTANCE IN A RESISTOR PRODUCED IN A SINGLE CRYSTALLINE SUBSTRATE
3892596 - UTILIZING ION IMPLANTATION IN COMBINATION WITH DIFFUSION TECHNIQUES
4013971 - INTEGRATED AMPLIFIER
4128741 - ELECTRONIC CROSSPOINT ARRAY

TELEFUNKEN PATENTVERWERTUNGSGESELLSCHAFT MBH
3419955 - SEMICONDUCTOR FABRICATION
3427709 - PRODUCTION OF CIRCUIT DEVICE
3456335 - CONTACTING ARRANGEMENT FOR SOLID-STATE COMPONENTS
3461548 - PRODUCTION OF AN ELECTRICAL DEVICE
3462650 - ELECTRICAL CIRCUIT MANUFACTURE
3462656 - SEMICONDUCTOR COLLECTOR REGION
3466510 - INTEGRATED GRAETZ RECTIFIER CIRCUIT
3468018 - PRODUCTION OF CIRCUITS
3495141 - CONTROLLABLE SCHOTTKY DIODE
3504240 - SEMICONDUCTOR DEVICE UTILIZING HEAT INJECTION OF MAJORITY CARRIERS
3543102 - COMPOSITE SEMICONDUCTOR DEVICE COMPOSED OF A PLURALITY OF SIMILAR ELEMENTS AND MEANS CONNECTING TOGETHER ONLY THOSE ELEMENTS HAVING SUBSTANTIALLY IDENTICAL ELECTRICAL CHARACTERISTICS
3566166 - MECHANICAL RESONATOR FOR USE IN AN INTEGRATED SEMICONDUCTOR CIRCUIT
3631311 - SEMICONDUCTOR CIRCUIT ARRANGEMENT WITH INTEGRATED BASE LEAKAGE RESISTANCE
3633268 - METHOD OF PRODUCING ONE OR MORE LARGE INTEGRATED SEMI-CONDUCTOR CIRCUITS
3639814 - INTEGRATED SEMICONDUCTOR CIRCUIT HAVING INCREASED BARRIER LAYER CAPACITANCE
3657573 - UNIPOLAR DEVICE WITH MULTIPLE CHANNEL REGIONS OF DIFFERENT CROSS SECTION
3673016 - METHOD OF DIVIDING A SEMICONDUCTOR WAFER
3689992 - PRODUCTION OF CIRCUIT DEVICE
3705060 - METHOD OF PRODUCING A SEMICONDUCTOR OR THICK FILM DEVICE
3756873 - METHOD OF MAKING A SEMICONDUCTOR DEVICE
3817799 - PRODUCTION OF CIRCUIT DEVICE
3922706 - TRANSISTOR HAVING EMITTER WITH HIGH CIRCUMFERENCE-SURFACE AREA RATIO
3947869 - SEMICONDUCTOR DEVICE HAVING INTERNAL JUNCTION PASSSIVATING INSULATING LAYER

TELETYPE CORPORATION
3893146 - SEMICONDUCTOR CAPACITOR STRUCTURE AND MEMORY CELL, AND METHOD OF MAKING
4045310 - STARTING PRODUCT FOR THE PRODUCTION OF A READ-ONLY MEMORY AND A METHOD OF PRODUCING IT AND THE READ-ONLY MEMORY

TEXAS INSTRUMENTS, INCORPORATED
3421055 - STRUCTURE AND METHOD FOR PREVENTING SPURIOUS GROWTHS DURING EPITAXIAL DEPOSITION OF SEMICONDUCTOR MATERIAL
3425879 - METHOD OF MAKING SHAPED EPITAXIAL DEPOSITS
3432918 - METHOD OF MAKING A CAPACITOR BY VACUUM MANGANESE OXIDE AS THE
3434015 - CAPACITOR FOR MINIATURE ELECTRONIC CIRCUITS OR THE LIKE
3434020 - OHMIC CONTACTS CONSISTING OF A FIRST LEVEL OF MOLYBDENUM-GOLD MIXTURE OF GOLD AND VANADIUM AND A SECOND LEVEL OF MOLYBDENUM-GOLD
3434068 - INTEGRATED CIRCUIT AMPLIFIER UTILIZING FIELD- EFFECT TRANSISTORS HAVING PARALLEL REVERSE CONNECTED DIODES AS BIAS CIRCUITS THEREFOR
3435445 - INTEGRATED ELECTRO-OPTIC PASSIVE REFLECTIVE DISPLAY DEVICE
3436605 - PACKAGING PROCESS FOR SEMICONDUCTOR DEVICES AND ARTICLE OF MANUFACTURE
3436611 - INSULATION STRUCTURE FOR CROSSOVER LEADS IN INTEGRATED CIRCUITRY

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

TEXAS INSTRUMENTS, INCORPORATED (CONTINUED)

3436621 - LINEAR AMPLIFIER UTILIZING A PAIR OF FIELD EFFECT TRANSISTORS
3436622 - COMPOUND CHANNEL INSULATED GATE TRIODE
3440114 - SELECTIVE GOLD DOPING FOR HIGH RESISTIVITY REGIONS IN SILICON
3442011 - METHOD FOR ISOLATING INDIVIDUAL DEVICES IN AN INTEGRATED CIRCUIT MONOLITHIC BAR
3445793 - HIGH FREQUENCY STRIP TRANSMISSION LINE
3453722 - METHOD FOR THE FABRICATION OF INTEGRATED CIRCUITS
3453723 - ELECTRON BEAM TECHNIQUES IN INTEGRATED CIRCUITS
3454906 - BISECTED DIODE LOADED LINE PHASE SHIFTER
3454945 - MODULAR INTEGRATED ELECTRONICS RADAR
3458368 - INTEGRATED CIRCUITS AND FABRICATION THEREOF
3463975 - UNITARY SEMICONDUCTOR HIGH SPEED SWITCHING DEVICE UTILIZING A BARRIER DIODE
3465215 - PROCESS FOR FABRICATING MONOLITHIC CIRCUITS HAVING MATCHED COMPLEMENTARY TRANSISTORS AND PRODUCT
3466719 - METHOD OF FABRICATING THIN FILM CAPACITORS
3468728 - METHOD FOR FORMING OHMIC CONTACT FOR A SEMICONDUCTOR DEVICE
3473090 - INTEGRATED CIRCUIT HAVING MATCHED COMPLEMENTARY TRANSISTORS
3474308 - MONOLITHIC CIRCUITS HAVING MATCHED COMPLEMENTARY TRANSISTORS, SUB-EPITAXIAL AND SURFACE RESISTORS, AND N AND P CHANNEL F IELD EFFECT TRANSISTORS
3474309 - MONOLITHIC
3475664 - AMBIENT ATMOSPHERE ISOLATED SEMI- CONDUCTOR DEVICES
3475700 - MONOLITHIC MICROWAVE DUPLEXER SWITCH
3476941 - PHOTOTRANSISTOR HAVING LIGHT SENSITIVE DIODE CONNECTED ACROSS COLLECTOR-BASE JUNCTION TO INCREASE TURNOFF TIME
3476991 - INVERSION LAYER FIELD EFFECT DEVICE WITH AZIMUTHALLY DEPENDENT CARRIER MOBILITY
3484932 - METHOD OF MAKING INTEGRATED CIRCUITS
3488834 - MICROELECTRONIC CIRCUIT FORMED IN AN INSULATING SUBSTRATE AND METHOD OF MAKING SAME
3489953 - STABILIZED INTEGRATED CIRCUIT AND PROCESS FOR FABRICATING SAME
3491273 - SEMICONDUCTOR DEVICES HAVING FIELD RELIEF ELECTRODE
3492511 - HIGH INPUT IMPEDANCE CIRCUIT FOR A FIELD EFFECT TRANSISTOR INCLUDING CAPACITIVE GATE BIASING MEANS
3496333 - THERMAL PRINTER
3499213 - METHOD OF MAKING A MULTILAYER CONTACT SYSTEM FOR SEMICONDUCTOR DEVICES
3500144 - RANDOM WHISKER CONTACT METHOD FOR SEMICONDUCTOR DEVICES
3501342 - SEMICONDUCTORS HAVING SELECTIVELY FORMED CONDUCTIVE OR METALLIC PORTIONS AND METHODS OF MAKING SAME
3505107 - VAPOR DEPOSITION OF GERMANIUM SEMICONDUCTOR MATERIAL
3507766 - METHOD OF FORMING HETEROGENEOUS COMPOSITE INSULATING LAYER OF SILICON DIOXIDE IN MULTILEVEL INTEGRATING CIRCUITS
3508084 - ENHANCEMENT-MODE MOS CIRCUITRY
3508125 - MICROWAVE MIXER DIODE COMPRISING A SCHOTTKY BARRIER JUNCTION
3514345 - DIODE ARRAY AND PROCESS FOR MAKING SAME
3518449 - INTEGRATED LOGIC NETWORK
3519901 - BI-LAYER INSULATION STRUCTURE POLYCRYSTALLINE SEMICONDUCTOR MATERIAL FOR INTEGRATED CIRCUIT ISOLATION
3525025 - ELECTRICALLY ISOLATED SEMICONDUCTOR DEVICES IN INTEGRATED CIRCUITS
3528906 - RF SPUTTERING METHOD AND SYSTEM
3529256 - INTEGRATED BAND-PASS FILTER
3533160 - AIR-ISOLATED INTEGRATED CIRCUITS
3534234 - MODIFIED PLANAR PROCESS FOR MAKING SEMICONDUCTOR DEVICES HAVING ULTRAFINE MESA TYPE GEOMETRY
3534236 - SEMICONDUCTOR INTEGRATED CIRCUIT STRUCTURE
3535532 - INTERGRATED CIRCUIT INCLUDING LIGHT SOURCE, PHOTODIODE AND ASSOCIATED COMPONENTS
3536965 - METALLIC CONTACT AND INTERCONNECTION SYSTEM FOR SEMICONDUCTOR DEVICES
3541543 - BINARY DECODER
3549432 - MULTILAYER MICROELECTRONIC CIRCUITRY TECHNIQUES
3553533 - DIELECTRIC BODIES WITH SELECTIVELY FORMED CONDUCTIVE OR METALLIC PORTIONS, COMPOSITES THEREOF WITH SEMICONDUCTOR MATERIA L AND METHODS OF MAKING SAID BODIES AND COMPOSITES
3559005 - INTEGRATED PLANAR VARACTOR DIODE
3566153 - PROGRAMMABLE SEQUENTIAL LOGIC
3566220 - INTEGRATED SEMICONDUCTOR CIRCUIT HAVING COMPLEMENTARY TRANSISTORS PROVIDED WITH DIELECTRIC ISOLATION AND SURFACE COLLECT OR CONTACTS
3568097 - SWITCHED LINE LENGTH PHASE SHIFT NETWORK FOR STRIP TRANSMISSION LINE

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

TEXAS INSTRUMENTS, INCORPORATED (CONTINUED)

3571914 - SEMICONDUCTOR DEVICE STABILIZATION USING DOPED OXIDATIVE OXIDE
3571917 - INTEGRATED HEATER ELEMENT ARRAY AND DRIVE MATRIX AND METHOD OF MAKING SAME
3571918 - INTEGRATED CIRCUITS AND FABRICATION THEREOF
3571919 - SEMICONDUCTOR DEVICE FABRICATION
3573490 - CAPACITOR PULL-UP REGISTER BIT
3573509 - DEVICE FOR REDUCING BIPOLAR EFFECTS IN MOS INTEGRATED CIRCUITS
3573570 - TUNGSTEN METAL OHMIC CONTACT AND ELECTRICAL INTERCONNECTIONS FOR A SEMICONDUCTOR DEVICE
3573754 - INFORMATION TRANSFER SYSTEM
3575733 - ELECTRON BEAM TECHNIQUES IN INTEGRATED CIRCUITS
3576475 - FIELD EFFECT TRANSISTORS FOR INTEGRATED CIRCUITS AND METHODS OF MANUFACTURE
3577038 - SEMICONDUCTOR DEVICES
3578515 - PROCESS FOR FABRICATING PLANAR DIODES IN SEMI- INSULATING SUBSTRATES
3581161 - MOLYBDENUM-GOLD-MOLYBDENUM INTERCONNECTION SYSTEM FOR INTEGRATED CIRCUITS
3581385 - METHOD FOR FABRICATING LARGE SCALE INTEGRATED CIRCUITS WITH DISCRETIONARY WIRING
3587166 - INSULATED ISOLATION TECHNIQUES IN INTEGRATED CIRCUITS
3590479 - METHOD FOR MAKING AMBIENT ATOMSPHERE ISOLATED SEMI-CONDUCTOR DEVICES
3593070 - SUBMOUNT FOR SEMICONDUCTOR ASSEMBLY
3597834 - METHOD IN FORMING ELECTRICALLY CONTINUOUS CIRCUIT THROUGH INSULATING LAYER
3598664 - HIGH FREQUENCY TRANSISTOR AND PROCESS FOR FABRICATING SAME
3599010 - HIGH SPEED, LOW POWER, DYNAMIC SHIFT REGISTER WITH SYNCHRONOUS LOGIC GATES
3601625 - MOSIC WITH PROTECTION AGAINST VOLTAGE SURGES
3601628 - PRECHARGE MOS-BIPOLAR OUTPUT BUFFER
3601630 - MOS CIRCUIT WITH BIPOLAR EMITTER-FOLLOWER OUTPUT
3601669 - INTEGRATED HEATER ELEMENT ARRAY AND DRIVE MATRIX THEREFOR
3609252 - TRANSDUCER APPARATUS AND SYSTEM UTILIZING INSULATED GATE SEMICONDUCTOR FIELD EFFECT DEVICES
3613226 - THREE-DIMENSIONAL INTEGRATED CIRCUITS AND METHODS OF MAKING SAME
3614554 - MINIATURIZED THIN FILM INDUCTORS FOR USE IN INTEGRATED CIRCUITS
3615929 - METHOD OF FORMING EPITAXIAL REGION OF PREDETERMINED THICKNESS AND ARTICLE OF MANUFACTURE
3617399 - METHOD OF FABRICATING SEMICONDUCTOR POWER DEVICES WITHIN HIGH RESISTIVITY ISOLATION RINGS
3619741 - METHOD OF PROVIDING INTEGRATED DIFFUSED EMITTER BALLAST RESISTORS FOR IMPROVED POWER CAPABILITIES OF SEMICONDUCTOR DEVICES
3620833 - INTEGRATED CIRCUIT FABRICATION
3622812 - BIPOLAR-TO-MOS INTERFACE STAGE
3624467 - MONOLITHIC INTEGRATED CIRCUIT STRUCTURE AND METHOD OF FABRICATION
3634203 - THIN FILM METALLIZATION PROCESSES FOR MICROCIRCUITS
3641661 - METHOD OF FABRICATING INTEGRATED CIRCUIT ARRAYS
3643138 - SEMICONDUCTOR DEVICE
3643232 - LARGE SCALE INTEGRATION OF ELECTRONIC SYSTEMS IN MICROMINIATURE FORM
3649843 - MOS BIPOLAR PUSH-PULL OUTPUT BUFFER
3653999 - METHOD OF FORMING BEAM LEADS ON SEMICONDUCTOR DEVICES AND INTEGRATED CIRCUITS
3654526 - METALLIZATION SYSTEM FOR SEMICONDUCTORS
3659160 - INTEGRATED CIRCUIT PROCESS UTILIZING ORIENTATION DEPENDENT SILICON ETCH
3673679 - COMPLEMENTARY INSULATED GATE FIELD EFFECT DEVICES
3682724 - PROCESS FOR FABRICATING INTEGRATED CIRCUIT HAVING MATCHED COMPLEMENTARY TRANSISTORS
3691406 - SURFACE ACOUSTIC WAVE GENERATING SYSTEM
3697337 - PROCESS FOR FABRICATING A MONOLITHIC CIRCUIT WITH HIGH Q CAPACITOR
3698012 - MULTI-CHARACTER ELECTRONIC DISPLAY
3702985 - MOS TRANSISTOR INTEGRATED MATRIX
3714523 - MAGNETIC FIELD SENSOR
3725160 - HIGH DENSITY INTEGRATED CIRCUITS
3738883 - DIELECTRIC ISOLATION PROCESSES
3740276 - MULTI-COMPONENT SEMICONDUCTOR NETWORK AND METHOD FOR MAKING SAME
3740731 - ONE TRANSISTOR DYNAMIC MEMORY CELL
3740732 - DYNAMIC DATA STORAGE CELL
3748548 - THREE-DIMENSIONAL INTEGRATED CIRCUITS AND METHOD OF MAKING SAME

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

TEXAS INSTRUMENTS, INCORPORATED (CONTINUED)

3754168 - METAL CONTACT AND INTERCONNECTION SYSTEM AND NONHERMETIC ENCLOSED SEMICONDUCTOR DEVICES
3765747 - LIQUID CRYSTAL DISPLAY USING A MOAT, INTEGRAL DRIVER CIRCUIT AND ELECTRODES FORMED WITHIN A SEMICONDUCTOR SUBSTRATE
3769562 - DOUBLE ISOLATION FOR ELECTRONIC DEVICES
3771217 - INTEGRATED CIRCUIT ARRAYS UTILIZING DISCRETIONARY WIRING AND METHOD OF FABRICATING SAME
3772577 - GUARD RING MESA CONSTRUCTION FOR LOW AND HIGH VOLTAGE NPN AND PNP TRANSISTORS AND DIODES AND METHOD OF MAKING SAME
3778688 - MOS-BIPOLAR HIGH VOLTAGE DRIVER CIRCUIT
3781515 - INTEGRATED HEATER ELEMENT ARRAY AND DRIVE MATRIX
3789276 - MULTILAYER MICROELECTRONIC CIRCUITRY TECHNIQUES
3796597 - METHOD OF PRODUCING SEMICONDUCTING MONOCRYSTALLINE SILICON ON SPINEL SUBSTRATES
3798135 - ANODIC PASSIVATING PROCESSES FOR INTEGRATED CIRCUITS
3809928 - INTEGRATED STRUCTURE AMPLIFIER WITH THERMAL FEEDBACK
3814641 - PROCESS OF FABRICATING SILICON PHOTOMASK
3832576 - ENCODER CIRCUIT FOR REDUCE PIN COUNT FOR DATA ENTRY INTO INSULATED GATE FIELD EFFECT TRANSISTOR INTEGRATED CIRCUITS
3834958 - METHOD FOR ISOLATION OF CIRCUIT REGIONS IN MONOLITHIC INTEGRATED CIRCUIT STRUCTURE
3836991 - SEMICONDUCTOR DEVICE HAVING EPITAXIAL REGION OF PREDETERMINED THICKNESS
3838441 - SEMICONDUCTOR DEVICE ISOLATION USING SILICON CARBIDE
3844858 - PROCESS FOR CONTROLLING THE THICKNESS OF A THIN LAYER OF SEMICONDUCTOR MATERIAL AND SEMICONDUCTOR SUBSTRATE
3851280 - NON-LINEAR SIGNAL PROCESSING DEVICE USING SQUARE LAW DETECTION OF SURFACE ELASTIC WAVES WITH INSULATED GATE FIELD EFFECT TRANSISTOR
3851313 - MEMORY CELL FOR SEQUENTIALLY ADDRESSED MEMORY ARRAY
3855009 - ION-IMPLANTATION AND CONVENTIONAL EPITAXY TO PRODUCE DIELECTRICALLY ISOLATED SILICON LAYERS
3860461 - METHOD FOR FABRICATING SEMICONDUCTOR DEVICES UTILIZING COMPOSITE MASKING
3860466 - NITRIDE COMPOSED MASKING FOR INTEGRATED CIRCUITS
3878551 - SEMICONDUCTOR INTEGRATED CIRCUITS HAVING IMPROVED ELECTRICAL ISOLATION CHARACTERISTICS
3881180 - NON-VOLATILE MEMORY CELL
3882469 - NON-VOLATILE VARIABLE THRESHOLD MEMORY CELL
3882529 - PUNCH-THROUGH SEMICONDUCTOR DIODES
3884733 - DIELECTRIC ISOLATION PROCESS
3893017 - REGULATOR WITH BIPOLAR TRANSISTORS
3905037 - INTEGRATED CIRCUIT COMPONENTS IN INSULATED ISLANDS OF INTEGRATED SEMICONDUCTOR MATERIALS IN A SINGLE SUBSTRATE
3909837 - HIGH-SPEED TRANSISTOR WITH RECTIFYING CONTACT CONNECTED BETWEEN BASE AND COLLECTOR
3921282 - INSULATED GATE FIELD EFFECT TRANSISTOR CIRCUITS AND THEIR METHOD OF FABRICATION
3933528 - PROCESS FOR FABRICATING INTEGRATED CIRCUITS UTILIZING ION IMPLANTATION
3936929 - FET AND BIPOLAR DEVICE AND CIRCUIT PROCESS WITH MAXIMUM JUNCTION CONTROL
3938176 - PROCESS FOR FABRICATING DIELECTRICALLY ISOLATED SEMICONDUCTOR COMPONENTS OF AN INTEGRATED CIRCUIT
3946247 - ANALOGUE SHIFT REGISTER CORRELATORS
3947698 - CHARGE COUPLED DEVICE MULTIPLEXER
3954524 - SELF-ALIGNING PHOTORESIST PROCESS FOR SELECTIVELY OPENING TOPS OF MESAS IN MESA-DIODE-ARRAY STRUCTURES
3955181 - SELF-REFRESHING RANDOM ACCESS MEMORY CELL
3962713 - LARGE VALUE CAPACITOR
3965568 - PROCESS FOR FABRICATION AND ASSEMBLY OF SEMICONDUCTOR DEVICES
3969749 - SUBSTRATE FOR DIELECTRIC ISOLATED INTEGRATED CIRCUIT WITH V-ETCHED DEPTH GROOVES FOR LAPPING GUIDE
3971060 - TTL COUPLING TRANSISTOR
3982266 - INTEGRATED INJECTION LOGIC HAVING HIGH INVERSE CURRENT GAIN
3986199 - BIPOLAR LOGIC HAVING GRADED POWER
3999080 - TRANSISTOR COUPLED LOGIC CIRCUIT
4005318 - ELASTIC WAVE DETECTOR
4013901 - STACKED LOGIC DESIGN FOR I\2/ L WATCH
4017885 - LARGE VALUE CAPACITOR
4035666 - ANALOGUE SHIFT REGISTER CORRELATORS
4035820 - ADJUSTMENT OF AVALANCHE VOLTAGE IN DIFMOS MEMORY DEVICES BY CONTROL OF IMPURITY DOPING
4037217 - READ-ONLY MEMORY USING COMPLEMENTARY CONDUCTIVITY TYPE INSULATED GATE FIELD EFFECT TRANSISTORS
4037242 - DUAL INJECTOR, FLOATING GATE MOS ELECTRICALLY ALTERABLE, NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE
4042948 - INTEGRATED CIRCUIT ISOLATION WITH MESAS AND/OR INSULATING SUBSTRATE
4050979 - PROCESS FOR THINNING SILICON WITH SPECIAL APPLICATION TO PRODUCING SILICON ON INSULATOR

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

TEXAS INSTRUMENTS, INCORPORATED (CONTINUED)
4054899 - PROCESS FOR FABRICATING MONOLITHIC CIRCUITS HAVING MATCHED COMPLEMENTARY TRANSISTORS AND PRODUCT
4055444 - METHOD OF MAKING N-CHANNEL MOS INTEGRATED CIRCUITS
4063271 - FET AND BIPOLAR DEVICE AND CIRCUIT PROCESS WITH MAXIMUM JUNCTION CONTROL
4065742 - COMPOSITE SEMICONDUCTOR STRUCTURES
4070653 - RANDOM ACCESS MEMORY CELL WITH ION IMPLANTED RESISTOR ELEMENT
4072981 - FAST SWITCHING DARLINGTON CIRCUIT
4075039 - INTEGRATED LOGIC CIRCUIT AND METHOD OF FABRICATION
4084173 - INTERDIGITATED TRANSISTOR PAIR
4092735 - STATIC MEMORY CELL USING FIELD IMPLANTED RESISTANCE
4101350 - SELF-ALIGNED EPITAXIAL METHOD FOR THE FABRICATION OF SEMICONDUCTOR DEVICES
4104732 - STATIC RAM CELL
4104858 - BIPOLAR LOGIC HAVING GRADED POWER
4110776 - SEMICONDUCTOR INTEGRATED CIRCUIT WITH IMPLANTED RESISTOR ELEMENT IN POLYCRYSTALLINE SILICON LAYER
4112509 - ELECTRICALLY ALTERABLE FLOATING GATE SEMICONDUCTOR MEMORY DEVICE
4112575 - FABRICATION METHODS FOR THE HIGH CAPACITY RAM CELL
4120744 - METHOD OF FABRICATING A THERMAL DISPLAY DEVICE
4132059 - STACKED LOGIC DESIGN FOR I+HU 2+B L WATCH
4137109 - SELECTIVE DIFFUSION AND ETCHING METHOD FOR ISOLATION OF INTEGRATED LOGIC CIRCUIT
4139785 - STATIC MEMORY CELL WITH INVERTED FIELD EFFECT TRANSISTOR
4139786 - STATIC MOS MEMORY CELL USING INVERTED N-CHANNEL FIELD-EFFECT TRANSISTOR
4151020 - HIGH DENSITY N-CHANNEL SILICON GATE READ ONLY MEMORY
4151021 - METHOD OF MAKING A HIGH DENSITY FLOATING GATE ELECTRICALLY PROGRAMMABLE ROM
4152779 - MOS RAM CELL HAVING IMPROVED REFRESH TIME
4164751 - HIGH CAPACITY DYNAMIC RAM CELL
4173496 - INTEGRATED SOLAR CELL ARRAY

THOMSON-CSF
3750055 - INTEGRATED PHASE-SHIFTING MICROCIRCUIT
3775646 - MOSAIC OF M. O. S. TYPE SEMICONDUCTOR ELEMENTS
3805129 - FIELD EFFECT TRANSISTOR HAVING TWO GATES FOR FUNCTIONING AT EXTREMELY HIGH FREQUENCIES
4013896 - HIGH-SPEED LOGIC GATE WITH TWO COMPLEMENTARY TRANSISTORS AND SATURABLE RESISTORS
4069493 - NOVEL INTEGRATED CIRCUIT AND METHOD OF MANUFACTURING SAME
4121116 - COMPONENT FOR LOGIC CIRCUITS AND LOGIC CIRCUITS EQUIPPED WITH THIS COMPONENT
4122543 - NON-VOLATILE MEMORY FOR FAST SIGNALS
4143421 - TETRODE TRANSISTOR MEMORY LOGIC CELL

TOKO, INC.
4039358 - METHOD OF MANUFACTURING AN INSULATED GATE TYPE FIELD EFFECT SEMICONDUCTOR DEVICE

TOKYO SHIBAURA ELECTRIC CO., LTD.
3512099 - SEMICONDUCTOR AMPLIFIER WHEREIN SEVERAL METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTORS ARE COUPLED ON A SUBSTRATE
3603848 - COMPLEMENTARY FIELD-EFFECT TYPE SEMICONDUCTOR DEVICE
3617753 - SEMICONDUCTOR PHOTOELECTRIC CONVERTING DEVICE
3634929 - METHOD OF MANUFACTURING SEMICONDUCTOR INTEGRATED CIRCUITS
3694707 - SEMICONDUCTOR DEVICE
3739238 - SEMICONDUCTOR DEVICE WITH A FIELD EFFECT TRANSISTOR
3749619 - METHOD FOR MANUFACTURING A SEMICONDUCTOR INTEGRATED CIRCUIT ISOLATED BY DIELECTRIC MATERIAL
3756877 - METHOD FOR MANUFACTURING A SEMICONDUCTOR INTEGRATED CIRCUIT ISOLATED BY DIELECTRIC MATERIAL
3825945 - FIELD EFFECT SEMICONDUCTOR MEMORY APPARATUS WITH A FLOATING GATE
3846766 - ASSOCIATIVE MEMORIES INCLUDING MOS TRANSISTORS
3858237 - SEMICONDUCTOR INTEGRATED CIRCUIT ISOLATED THROUGH DIELECTRIC MATERIAL
3868187 - AVALANCHE INJECTION TYPE MOS MEMORY
3886581 - DISPLAY DEVICE USING LIGHT-EMITTING SEMICONDUCTOR ELEMENTS
4011653 - METHOD FOR MANUFACTURING A SEMICONDUCTOR INTEGRATED CIRCUIT INCLUDING AN INSULATING GATE TYPE SEMICONDUCTOR TRANSISTOR
4041517 - VERTICAL TYPE JUNCTION FIELD EFFECT SEMICONDUCTOR DEVICE

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

TOKYO SHIBAURA ELECTRIC CO., LTD. (CONTINUED)

4054900 - I.I.L. WITH REGION CONNECTING BASE OF DOUBLE DIFFUSED INJECTOR TO SUBSTRATE/EMITTER OF SWITCHING TRANSISTOR
4058419 - METHOD OF MANUFACTURING INTEGRATED INJECTION LOGIC SEMICONDUCTOR DEVICES UTILIZING SELF-ALIGNED DOUBLE-DIFFUSION TECHNIQUES
4064526 - I.I.L. WITH GRADED BASE INVERSELY OPERATED TRANSISTOR
4065187 - SEMICONDUCTOR LATCH CIRCUIT USING INTEGRATED LOGIC UNITS AND SCHOTTKY DIODE IN COMBINATION
4069495 - SEMICONDUCTOR DEVICE FOR INTEGRATED INJECTION LOGIC
4071774 - INTEGRATED INJECTION LOGIC WITH BOTH FAN IN AND FAN OUT SCHOTTKY DIODES, SERIALLY CONNECTED BETWEEN STAGES
4080618 - INSULATED-GATE FIELD-EFFECT TRANSISTOR
4091296 - SEMICONDUCTOR R-S FLIP-FLOP CIRCUIT
4096522 - MONOLITHIC SEMICONDUCTOR MASK PROGRAMMABLE ROM AND A METHOD FOR MANUFACTURING THE SAME
4106049 - SEMICONDUCTOR DEVICE
4115795 - SEMICONDUCTOR MEMORY DEVICE
4119998 - INTEGRATED INJECTION LOGIC WITH BOTH GRID AND INTERNAL DOUBLE-DIFFUSED INJECTORS
4123771 - NONVOLATILE SEMICONDUCTOR MEMORY
4127863 - GATE TURN-OFF TYPE THYRISTOR WITH SEPARATE SEMICONDUCTOR RESISTIVE WAFER PROVIDING EMITTER BALLAST
4131906 - DYNAMIC RANDOM ACCESS MEMORY USING MOS FETS AND METHOD FOR MANUFACTURING SAME
4131909 - SEMICONDUCTOR INTEGRATED CIRCUIT ISOLATED THROUGH DIELECTRIC MATERIAL AND A METHOD FOR MANUFACTURING THE SAME
4138690 - DARLINGTON CIRCUIT SEMICONDUCTOR DEVICE
4143390 - SEMICONDUCTOR DEVICE AND A LOGICAL CIRCUIT FORMED OF THE SAME
4143391 - INTEGRATED CIRCUIT DEVICE
4144587 - COUNTING LEVEL +37 1+38 +0 BITS TO MINIMIZE ROM ACTIVE ELEMENTS
4149176 - COMPLEMENTARY MOSFET DEVICE
4151019 - METHOD OF MANUFACTURING INTEGRATED INJECTION LOGIC SEMICONDUCTOR DEVICES UTILIZING SELF-ALIGNED DOUBLE-DIFFUSION TECHNIQUES
4151610 - HIGH DENSITY SEMICONDUCTOR MEMORY DEVICE FORMED IN A WELL AND HAVING MORE THAN ONE CAPACITOR
4152717 - COMPLEMENTARY MOSFET DEVICE
4153487 - METHOD OF MANUFACTURING INTERGRATED INJECTION LOGIC SEMICONDUCTOR DEVICES UTILIZING SELF-ALIGNED DOUBLE-DIFFUSION TECHNIQUES
4161743 - SEMICONDUCTOR DEVICE WITH SILICON CARBIDE-GLASS-SILICON CARBIDE PASSIVATING OVERCOAT
4162506 - SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE WITH DUAL THICKNESS POLY-SILICON WIRING
4163245 - INTEGRATED CIRCUIT DEVICE
4167747 - COMPLEMENTARY MOSFET DEVICE AND METHOD OF MANUFACTURING THE SAME
4168442 - CMOS FET DEVICE WITH ABNORMAL CURRENT FLOW PREVENTION
4169271 - SEMICONDUCTOR DEVICE INCLUDING A THERMAL FUSE ENCAPSULATED IN A DROPLET OF SILICONE RUBBER
4173734 - VOLTAGE DIVIDING INTEGRATED CIRCUIT DEVICE
4173819 - METHOD OF MANUFACTURING A DYNAMIC RANDOM ACCESS MEMORY USING MOS FETS

TRANSITRON ELECTRONIC CORPORATION

4048649 - SUPERINTEGRATED V-GROOVE ISOLATED BIPOLAR AND VMOS TRANSISTORS

TRW INC.

3475665 - ELECTRODE LEAD FOR SEMICONDUCTOR ACTIVE DEVICES
3579391 - METHOD OF PRODUCING DIELECTRIC ISOLATION FOR MONOLITHIC CIRCUIT
3609375 - SOLID STATE LINEAR PHOTO SENSOR
3624894 - SEALING TECHNIQUE FOR TRANSPARENT LIDS ON INTEGRATED CIRCUIT PACKAGES
3737742 - BI-POLAR SEMICONDUCTOR DEVICE EMPLOYING CERMET FOR BOTH SCHOTTKY BARRIER AND OHMIC CONTACT
3772536 - DIGITAL CELL FOR LARGE SCALE INTEGRATION
3874918 - STRUCTURE AND PROCESS FOR SEMICONDUCTOR DEVICE USING BATCH PROCESSING
3891936 - LOW FREQUENCY FIELD EFFECT AMPLIFIER
3913213 - INTEGRATED CIRCUIT TRANSISTOR SWITCH
3966577 - DIELECTRICALLY ISOLATED SEMICONDUCTOR DEVICES
3981072 - BIPOLAR TRANSISTOR CONSTRUCTION METHOD

TRW SEMICONDUCTORS INC.

3452256 - HIGH FREQUENCY MULTI-CELL TRANSISTOR STRUCTURE

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

TRW SEMICONDUCTORS INC. (CONTINUED)
3574008 - MUSHROOM EPITAXIAL GROWTH IN TIER-TYPE SHAPED HOLES
3585712 - SELECTION AND INTERCONNECTION OF DEVICES ON A MULTI-DEVICE WAFER
3620932 - BEAM LEADS AND METHOD OF FABRICATION

TZENTRALEN INSTITUT ZI ELEMENTI
3726726 - METHOD OF PRODUCING DIFFUSED HIGH-RESISTIVITY MICRORESISTORS

UNION CARBIDE CORPORATION
3469147 - DIELECTRICALLY ISOLATED STRUCTURES AND METHOD

UNISEM CORPORATION
3708731 - GALLIUM ARSENIDE INTERGRATED CIRCUIT

UNITED STATES OF AMERICA, AIR FORCE
3436817 - METHOD OF MAKING FRINGING FIELD CONTROLLED THIN FILM ACTIVE DEVICE
3965462 - SERPENTINE CHARGE-COUPLED-DEVICE MEMORY CIRCUIT
4017887 - METHOD AND MEANS FOR PASSIVATION AND ISOLATION IN SEMICONDUCTOR DEVICES
4050965 - SIMULTANEOUS FABRICATION OF CMOS TRANSISTORS AND BIPOLAR DEVICES
4095331 - FABRICATION OF AN EPITAXIAL LAYER DIODE IN ALUMINUM NITRIDE ON SAPPHIRE

UNITED STATES OF AMERICA, ARMY
3813586 - MATCHED PAIR OF ENHANCEMENT MODE MOS TRANSISTORS
3999142 - VARIABLE TUNING AND FEEDBACK ON HIGH POWER MICROWAVE TRANSISTOR CARRIER AMPLIFIER
4096509 - MNOS MEMORY TRANSISTOR HAVING A REDEPOSITED SILICON NITRIDE GATE DIELECTRIC
4117588 - METHOD OF MANUFACTURING THREE DIMENSIONAL INTEGRATED CIRCUITS
4142925 - METHOD OF MAKING SILICON-INSULATOR-POLYSILICON INFRARED IMAGE DEVICE UTILIZING EPITAXIAL DEPOSITION AND SELECTIVE ETCHING
4152715 - SILICON BASE CCD-BIPOLAR TRANSISTOR COMPATIBLE METHODS AND PRODUCTS

UNITED STATES OF AMERICA, ATOMIC ENERGY COMMISSION
3634731 - GENERALIZED CIRCUIT
3823350 - PROTECTIVE CARRIER FOR SEMICONDUCTOR CHIPS

UNITED STATES OF AMERICA, NATIONAL AERONAUTICS AND SPACE ADM
3616528 - SOLID STATE MATRICES
3623030 - SEMICONDUCTOR-FERROELECTRIC MEMORY DEVICE
3694700 - INTEGRATED CIRCUIT INCLUDING FIELD EFFECT TRANSISTOR AND CERMENT RESISTOR
3714526 - PHOTOTRANSISTOR
3760239 - COAXIAL INVERTED GEOMETRY TRANSISTOR HAVING BURIED EMITTER
3882530 - RADIATION HARDENING OF MOS DEVICES BY BORON
4087902 - FIELD EFFECT TRANSISTOR AND METHOD OF CONSTRUCTION THEREOF
4119996 - COMPLEMENTARY DMOS-VMOS INTEGRATED CIRCUIT STRUCTURE
4156309 - METHOD OF CONSTRUCTION OF A MULTI-CELL SOLAR ARRAY

UNITED STATES OF AMERICA, NAVY
3430114 - FIELD EFFECT TRANSISTOR IN AN INTEGRATED CIRCUIT HAVING AN EMBEDDED GRID
3447093 - ADDITIVE SEMICONDUCTOR AMPLIFIER
3591465 - SELECTIVE SILICON GROOVE ETCHING USING A TANTALUM OXIDE MASK FORMED AT ROOM TEMPERATURES
3615949 - CROSSOVER FOR LARGE SCALE ARRAYS
3663308 - METHOD OF MAKING ION IMPLANTED DIELECTRIC ENCLOSURES
3666967 - SELF-DESTRUCT ALUMINUM-TUNGSTIC OXIDE FILMS
3769561 - CURRENT LIMITING INTEGRATED CIRCUIT
4039833 - HIGH DENSITY INFRARED DETECTOR ARRAY
4104087 - METHOD FOR FABRICATING MNOS MEMORY CIRCUITS

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

UNITED TECHNOLOGIES CORPORATION
3478418 - FABRICATION OF THIN SILICON DEVICE CHIPS
3501829 - METHOD OF APPLYING CONTACTS TO A MICROCIRCUIT
3502952 - PLANAR PNPN SWITCHING DEVICE
3507713 - MONOLITHIC CIRCUIT CHIP CONTAINING NONCOMPATIBLE OXIDE-ISOLATED REGIONS
3516914 - ALUMINUM MASKING OF ACTIVE COMPONENTS DURING TANTALUM/NITRIDE SPUTTERING
3541678 - METHOD OF MAKING A GALLIUM ARSENIDE INTEGRATED CIRCUIT
3577043 - MOSFET WITH IMPROVED VOLTAGE BREAKDOWN CHARACTERISTICS

UNIVERSITY OF MINNESOTA, THE REGENTS OF
3994012 - PHOTOVOLTAIC SEMI-CONDUCTOR DEVICES

UNIVERSITY OF TOLEDO
3995174 - CHOPPER AND CHOPPER-MULTIPLEXER CIRCUITRY FOR MEASUREMENT OF REMOTE LOW-LEVEL SIGNALS

U. S. AUTOMATICS CORPORATION
3448298 - SEMICONDUCTOR CONTROLLED SWITCH CIRCUIT COMPONENT

U.S. PHILIPS CORPORATION
3456169 - INTEGRATED CIRCUITS USING HEAVILY DOPED SURFACE TO PREVENT CHANNELS
3456312 - METHOD OF MANUFACTURING A TARGET PLATE FOR USE IN A CAMERA TUBE
3458831 - SEMICONDUCTOR DEVICE FOR PRODUCING AND AMPLIFYING ELECTRICAL SIGNALS OF VERY HIGH FREQUENCIES
3484865 - INTEGRATED WITH INTERDIGITATED STRUCTURE
3488528 - INTEGRATED CIRCUIT
3497821 - COUPLING DEVICE FOR CASCADED TRANSISTOR AMPLIFIERS
3500139 - INTEGRATED CIRCUIT UTILIZING DIELECTRIC PLUS JUNCTION ISOLATION
3508127 - SEMICONDUCTOR INTEGRATED CIRCUITS
3518510 - PLANAR TRANSISTOR WITH SUBSTRATE-BASE CONNECTION PROVIDING AUTOMATIC GAIN CONTROL
3520052 - METHOD OF MANUFACTURING MATRIX ARRANGEMENTS
3522494 - HALL ELEMENT
3525020 - INTEGRATED CIRCUIT ARRANGEMENT HAVING GROUPS OF CROSSING CONNECTIONS
3525083 - INTEGRATED CIRCUIT READING STORE MATRICES
3529217 - PHOTOSENSITIVE SEMICONDUCTOR DEVICE
3536600 - METHOD OF MANUFACTURING SEMICONDUCTOR DEVICES USING AN ELECTROLYTIC ETCHING PROCESS AND SEMICONDUCTOR DEVICE MANUFACTURE D BY THIS METHOD
3544861 - STABILIZED SEMICONDUCTOR DEVICE
3562032 - METHOD OF MANUFACTURING AN INTEGRATED SEMICONDUCTOR DEVICE
3562607 - OVERLAY TYPE TRANSISTOR WITH BALLAST RESISTOR
3564291 - ELECTRONIC RELAY ARRANGEMENT
3576682 - METHOD OF MAKING COMPLEMENTARY TRANSISTORS IN MONOLITHIC INTEGRATED CIRCUIT
3579056 - SEMICONDUCTOR CIRCUIT HAVING ACTIVE DEVICES EMBEDDED IN FLEXIBLE SHEET
3580745 - SEMICONDUCTOR DEVICE
3582723 - TRANSISTOR
3586928 - INTEGRATED TRANSVERSE AND TRIGGERING LATERAL THYRISTORS
3586930 - HIGH FREQUENCY, HIGH POWER IGFET WITH INTERDIGITAL ELECTRODES AND PLURAL LOOPED GATE
3590273 - FOUR PHASE LOGIC SYSTEMS
3595713 - METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE COMPRISING COMPLEMENTARY TRANSISTORS
3595714 - METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE COMPRISING A FIELD-EFFECT TRANSISTOR
3595715 - METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE COMPRISING A JUNCTION FIELD-EFFECT TRANSISTOR
3602779 - EPITAXIAL TRANSISTOR WITH LIMITED AREA BURIED LAYER AND LIFETIME KILLERS
3602781 - INTEGRATED SEMICONDUCTOR CIRCUIT COMPRISING ONLY LOW TEMPERATURE PROCESSED ELEMENTS
3602981 - METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE OBTAINED BY CARRYING OUT SAID METHOD
3602982 - METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE AND DEVICE MANUFACTURED BY SAID METHOD
3607465 - METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE COMPRISING A MANUFACTURED BY SAID METHOD
3614558 - SEMICONDUCTOR DEVICES WITH MORE THAN ONE SEMICONDUCTOR CIRCUIT ELEMENT IN ONE BODY
3616345 - METHOD OF MANUFACTURING SEMICONDUCTOR DEVICES IN WHICH A SELECTIVE ELECTROLYTIC ETCHING PROCESS IS USED

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

U.S. PHILIPS CORPORATION (CONTINUED)

3621345 - SEMICONDUCTOR DEVICE HAVING A BISTABLE CIRCUIT ELEMENT
3621347 - SEMICONDUCTOR DEVICE COMPRISING A FIELD EFFECT TRANSISTOR HAVING AN INSULATED GATE ELECTRODE AND CIRCUIT ARRANGEMENT COMPRISING SUCH A SEMICONDUCTOR DEVICE
3624468 - INSULATED GATE FIELD EFFECT TRANSISTOR WITH OPPOSITE TYPE GATE CONNECTED REGION INSET IN SOURCE OR DRAIN
3635773 - METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE COMPRISING A ZENER DIODE AND SEMICONDUCTOR DEVICE MANUFACTURED BY USING THIS METHOD
3640807 - METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE MANUFACTURED BY SAID METHOD
3643139 - INTEGRATED CIRCUIT HAVING FOUR MOSFET DEVICES ARRANGED IN A CIRCLE SURROUNDING A GUARD DIFFUSION
3648129 - INSULATED GATE FIELD EFFECT TRANSISTOR WITH INTEGRATED SAFETY DIODE
3649885 - TETRODE MOSFET WITH GATE SAFETY DIODE WITHIN ISLAND ZONE
3649886 - SEMICONDUCTOR DEVICE HAVING A SEMICONDUCTOR BODY OF WHICH A SURFACE IS AT LEAST LOCALLY COVERED WITH AN OXIDE FILM AND METHOD OF MANUFACTURING A PLANAR
3654498 - SEMICONDUCTOR DEVICE HAVING AN INTEGRATED PULSE GATE CIRCUIT AND METHOD OF MANUFACTURING SAID DEVICE
3656010 - TRANSISTORIZED MASTER SLAVE FLIP-FLOP CIRCUIT
3665330 - TRANSISTOR AMPLIFIER INSENSITIVE TO THE POLARITY OF THE SUPPLY VOLTAGE
3666995 - INTEGRATED SEMICONDUCTOR DEVICE
3667000 - INTEGRATED HALL-EFFECT DEVICE
3667006 - SEMICONDUCTOR DEVICE HAVING A LATERAL TRANSISTOR
3676714 - SEMICONDUCTOR DEVICE
3676755 - SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING SAID DEVICE
3677838 - METHOD OF MANUFACTURING A ZENER DIODE
3677846 - MANUFACTURING SEMICONDUCTOR DEVICES
3678347 - DEEP DEPLETION SEMICONDUCTOR DEVICE WITH SURFACE INVERSION PREVENTING MEANS
3683306 - TEMPERATURE COMPENSATED SEMICONDUCTOR RESISTOR CONTAINING NEUTRAL INACTIVE IMPURITIES
3697784 - SEMICONDUCTOR INTEGRATED CIRCUITS
3702428 - MONOLITHIC IC WITH COMPLEMENTARY TRANSISTORS AND PLURAL BURIED LAYERS
3714527 - INTEGRATED MONOLITHIC SEMICONDUCTOR CIRCUIT WITH CONTROLLED CRYSTAL TEMPERATURE
3717775 - COUPLING OF BISTABLE ELEMENTS BY CONDUCTIVITY MODULATION
3717800 - DEVICE AND BASE PLATE FOR A MOSAIC OF SEMICONDUCTOR ELEMENTS
3718843 - SEMICONDUCTOR DEVICE FOR MONOLITHIC INTEGRATED CIRCUITS COMPACT
3721839 - SOLID STATE IMAGING DEVICE WITH FET SENSOR
3737701 - CAMERA TUBE HAVING A SEMICONDUCTOR TARGET WITH PN ORGANIC REGIONS COVERED BY A CONTINUOUS PERFORATED CONDUCTIVE LAYER
3737702 - CAMERA TUBE TARGET WITH PROJECTING P-TYPE REGIONS SEPARATED BY GROOVES COVERED WITH SILICON OXIDE LAYER APPROXIMATELY ONE-SEVENTH GROOVE DEPTH
3739239 - SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE DEVICE
3748545 - SEMICONDUCTOR DEVICE WITH INTERNAL CHANNEL STOPPER
3753005 - INTEGRATED CIRCUIT COMPRISING STRIP-LIKE CONDUCTORS
3755001 - METHOD OF MAKING SEMICONDUCTOR DEVICES WITH SELECTIVE DOPING AND SELECTIVE OXIDATION
3755014 - METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE EMPLOYING SELECTIVE DOPING AND SELECTIVE OXIDATION
3758387 - ION DISPLACEMENT CRYSTAL GROWTH
3759760 - PREVENTION OF AUTODOPING DURING THE MANUFACTURING OF A SEMICONDUCTOR DEVICE
3761319 - METHODS OF MANUFACTURING SEMICONDUCTOR DEVICES
3761900 - CAPACITIVE MATRIX STORE
3766444 - SEMICONDUCTOR DEVICE HAVING AN INTEGRATED THERMOCOUPLE
3767487 - METHOD OF PRODUCING IGFET DEVICES HAVING OUTDIFFUSED REGIONS AND THE PRODUCT THEREOF
3777230 - SEMICONDUCTOR DEVICE WITH ISOLATED CIRCUIT ELEMENTS
3783047 - METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE MANUFACTURE BY USING SUCH A METHOD
3787822 - METHOD OF PROVIDING INTERNAL CONNECTIONS IN A SEMICONDUCTOR DEVICE
3808463 - INTEGRATED FUNCTION GENERATOR
3822387 - CIRCUIT FOR RE-GENERATING A CURRENT
3823354 - HALL ELEMENT
3829718 - INTEGRATED CIRCUIT COMPRISING SUPPLY POLARITY INDEPENDENT CURRENT INJECTOR
3849216 - METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE MANUFACTURED BY USING THE METHOD
3868722 - SEMICONDUCTOR DEVICE HAVING AT LEAST TWO TRANSISTORS AND METHOD OF MANUFACTURING SAME
3873383 - INTEGRATED CIRCUITS WITH OXIDATION-JUNCTION ISOLATION AND CHANNEL STOP

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

U.S. PHILIPS CORPORATION (CONTINUED)

3879745 - SEMICONDUCTOR DEVICE
3887936 - RADIATION SENSITIVE SOLID STATE DEVICES
3890634 - TRANSISTOR CIRCUIT
3892033 - METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE
3893151 - SEMICONDUCTOR MEMORY DEVICE AND FIELD EFFECT TRANSISTOR SUITABLE FOR USE IN THE DEVICE
3896483 - SWITCH
3900350 - METHOD OF MANUFACTURING SEMICONDUCTOR DEVICES IN WHICH SILICON OXIDE REGIONS INSET IN SILICON ARE FORMED BY A MASKING OX IDATION, WHEREIN AN INTERMEDIATE LAYER OF POLYCRYSTALLINE SILICON IS PROVIDED BETWEEN THE SUBSTRATE AND THE OXIDATION MA
3909318 - METHOD OF FORMING COMPLEMENTARY DEVICES UTILIZING OUTDIFFUSION AND SELECTIVE OXIDATION
3911269 - CIRCUIT ARRANGEMENT HAVING AT LEAST ONE CIRCUIT ELEMENT WHICH IS ENERGISED BY MEANS OF RADIATION AND SEMICONDUCTOR DEVIC E SUITABLE FOR USE IN SUCH A CIRCUIT ARRANGEMENT
3911470 - INTEGRATED CIRCUIT FOR LOGIC PURPOSES HAVING TRANSISTORS WITH DIFFERENT BASE THICKNESSES AND METHOD OF MANUFACTURING
3911471 - SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING SAME
3912944 - INTEGRATED BUCKET BRIGADE MEMORY USING TRANSISTOR BARRIER CAPACITORS FOR STORAGE
3918070 - SEMICONDUCTOR DEVICES
3918080 - MULTIEMITTER TRANSISTOR WITH CONTINUOUS BALLAST RESISTOR
3918081 - INTEGRATED SEMICONDUCTOR DEVICE EMPLOYING CHARGE STORAGE AND CHARGE TRANSPORT FOR MEMORY OR DELAY LINE
3921283 - SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE DEVICE
3930909 - METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE UTILIZING SIMULTANEOUS OUTDIFFUSION DURING EPITAXIAL GROWTH
3931633 - ELECTRON TUBE INCLUDING A PHOTOCATHODE
3940784 - SEMICONDUCTOR DEVICE
3947299 - METHOD OF MANUFACTURING SEMICONDUCTOR DEVICES
3958040 - SEMICONDUCTOR DEVICE MANUFACTURE
3959039 - METHOD OF MANUFACTURING VERTICAL COMPLEMENTARY BIPOLAR TRANSISTORS EACH WITH EPITAXIAL BASE ZONES
3961340 - INTEGRATED CIRCUIT HAVING BIPOLAR TRANSISTORS AND METHOD OF MANUFACTURING SAID CIRCUIT
3961356 - INTEGRATED CIRCUIT WITH OXIDATION-JUNCTION ISOLATION AND CHANNEL STOP
3964092 - SEMICONDUCTOR DEVICES WITH CONDUCTIVE LAYER STRUCTURE
3965481 - CHARGE TRANSFER DEVICE WITH J FET ISOLATION AND MEANS TO DRAIN STRAY CHARGE
3969744 - SEMICONDUCTOR DEVICES
3970486 - METHODS OF PRODUCING A SEMICONDUCTOR DEVICE AND A SEMICONDUCTOR DEVICE PRODUCED BY SAID METHOD
3974516 - METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE HAVING AT LEAST ONE INSULATED GATE FIELD EFFECT TRANSISTOR, AND SEMICONDU CTOR DEVICE MANUFACTURED BY USING THE METHOD
3977016 - ELECTROLUMINESCENT DEVICE AND METHOD OF MANUFACTURING SAME
3977020 - SEMICONDUCTOR DEVICE, METHOD OF MANUFACTURING SAME AND CIRCUIT ARRANGEMENT COMPRISING THE DEVICE
3992639 - SCANNING DEVICE
3993512 - METHOD OF MANUFACTURING AN INTEGRATED CIRCUIT UTILIZING OUTDIFFUSION AND MULTIPLE LAYER EPITAXY
3993918 - INTEGRATED CIRCUITS
3993991 - DEVICE FOR DRIVING OR ENERGIZING A DISPLAY DEVICE
3999213 - SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE DEVICE
3999215 - INTEGRATED SEMICONDUCTOR DEVICE COMPRISING MULTI-LAYER CIRCUIT ELEMENT AND SHORT-CIRCUIT MEANS
4000019 - METHOD OF RETAINING SUBSTRATE PROFILES DURING EPITAXIAL DEPOSITION
4001862 - CHARGE TRANSFER DEVICE
4005453 - SEMICONDUCTOR DEVICE WITH ISOLATED CIRCUIT ELEMENTS AND METHOD OF MAKING
4007385 - SERIALLY-CONNECTED CIRCUIT GROUPS FOR INTERGRATED INJECTION LOGIC
4009057 - METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE
4009397 - LOGIC CIRCUIT
4011580 - INTEGRATED CIRCUIT
4013918 - ELECTROLUMINESCENT DIODE HAVING THRESHOLD EFFECT
4016594 - SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE DEVICE
4017750 - CIRCUIT ARRANGEMENT FOR EFFECTIVELY MAKING INTEGRATED IMPEDANCES ACCURATE
4032944 - SEMICONDUCTOR DEVICE FOR GENERATING INCOHERENT RADIATION AND METHOD OF MANUFACTURING SAME
4041474 - MEMORY MATRIX CONTROLLER
4056810 - INTEGRATED INJECTION LOGIC MEMORY CIRCUIT
4058825 - COMPLEMENTARY TRANSISTOR STRUCTURE HAVING TWO EPITAXIAL LAYERS AND METHOD OF MANUFACTURING SAME

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

U.S. PHILIPS CORPORATION (CONTINUED)
4078208 - LINEAR AMPLIFIER CIRCUIT WITH INTEGRATED CURRENT INJECTOR
4078244 - SEMICONDUCTOR DEVICE
4086613 - SEMICONDUCTOR DEVICE HAVING A PASSIVATED SURFACE AND METHOD OF MANUFACTURING THE DEVICE
4101344 - METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE
4113513 - METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE BY NON-SELECTIVELY IMPLANTING A ZONE OF PRE-DETERMINED LOW RESISTIVITY
4113515 - SEMICONDUCTOR MANUFACTURING METHOD USING BURIED NITRIDE FORMED BY A NITRIDATION TREATMENT IN THE PRESENCE OF ACTIVE NITROGEN
4115711 - THRESHOLD CIRCUIT WITH HYSTERESIS
4122482 - VERTICAL COMPLEMENTARY BIPOLAR TRANSISTOR DEVICE WITH EPITAXIAL BASE ZONES
4123672 - CIRCUIT ARRANGEMENT FOR FREQUENCY DIVISION OF HIGH-FREQUENCY PULSES
4123772 - MULTISEGMENT HALL ELEMENT FOR OFFSET VOLTAGE COMPENSATION
4126899 - JUNCTION FIELD EFFECT TRANSISTOR RANDOM ACCESS MEMORY
4126900 - RANDOM ACCESS JUNCTION FIELD-EFFECT FLOATING GATE TRANSISTOR MEMORY
4127864 - SEMICONDUCTOR DEVICE
4131809 - SYMMETRICAL ARRANGEMENT FOR FORMING A VARIABLE ALTERNATING-CURRENT RESISTANCE
4131908 - SEMICONDUCTOR PROTECTION DEVICE HAVING A BIPOLAR LATERAL TRANSISTOR
4139402 - METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE UTILIZING DOPED OXIDES AND CONTROLLED OXIDATION
4142196 - POLYCHROMATIC MONOLITHIC SEMICONDUCTOR ASSEMBLY
4143387 - SIGNAL MIXER INCLUDING RESISTIVE AND NORMAL GATE FIELD-EFFECT TRANSISTOR
4146905 - SEMICONDUCTOR DEVICE HAVING COMPLEMENTARY TRANSISTOR STRUCTURES AND METHOD OF MANUFACTURING SAME
4148053 -
4148054 -
4148055 -
4157563 - SEMICONDUCTOR DEVICE
4160989 - INTEGRATED CIRCUIT HAVING COMPLEMENTARY BIPOLAR TRANSISTORS
4161741 - SEMICONDUCTOR MEMORY DEVICE

VARIAN ASSOCIATES, INC.
4141021 - FIELD EFFECT TRANSISTOR HAVING SOURCE AND GATE ELECTRODES ON OPPOSITE FACES OF ACTIVE LAYER

WESCOM, INC.
3725683 - DISCRETE AND INTEGRATED-TYPE CIRCUIT

WESTERN DIGITAL CORPORATION
4062699 - METHOD FOR FABRICATING DIFFUSION SELF-ALIGNED SHORT CHANNEL MOS DEVICE

WESTERN ELECTRIC COMPANY, INC.
3487522 - MULTILAYERED THIN-FILM INTERMEDIATES EMPLOYING PARTING LAYERS TO PERMIT SELECTIVE, SEQUENTIAL ETCHING
3489656 - METHOD OF PRODUCING AN INTEGRATED CIRCUIT CONTAINING MULTILAYER TANTALUM COMPOUNDS
3809627 - ANODIZED CERMET FILM COMPONENTS AND THEIR MANUFACTURE
4131487 - GETTERING SEMICONDUCTOR WAFERS WITH A HIGH ENERGY LASER BEAM

WESTINGHOUSE BRAKE-ENGLISH ELECTRIC SEMI-CONDUCTORS -
3725753 -

WESTINGHOUSE BRAKE + SIGNAL CO. LTD.
3693054 - SEMICONDUCTOR HAVING A TRANSISTOR, A THRISTOR AND A DIODE IN ONE BODY
3725752 - SEMICONDUCTOR DEVICE

WESTINGHOUSE ELECTRIC CORP.
3421205 - FABRICATION OF STRUCTURES FOR SEMICONDUCTOR INTEGRATED CIRCUITS
3421943 - SOLAR CELL PANEL HAVING CELL EDGE AND BASE METAL ELECTRICAL CONNECTIONS
3423255 - SEMICONDUCTOR INTEGRATED CIRCUITS AND METHOD OF MAKING THE SAME
3423653 - INTEGRATED COMPLEMENTARY TRANSISTOR STRUCTURE WITH EQUIVALENT PERFORMANCE CHARACTERISTICS
3427559 - TUNABLE SIGNAL TRANSLATION SYSTEM USING SEMICONDUCTOR DRIFT FIELD DELAY LINE

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

WESTINGHOUSE ELECTRIC CORP. (CONTINUED)

3430104 - CONDUCTIVE INTERCONNECTIONS AND CONTACTS ON SEMICONDUCTOR DEVICES
3440502 - INSULATED GATE FIELD EFFECT TRANSISTOR STRUCTURE WITH REDUCED CURRENT LEAKAGE
3440503 - INTEGRATED COMPLEMENTARY MOS-TYPE TRANSISTOR STRUCTURE AND METHOD OF MAKING SAME
3441815 - SEMICONDUCTOR STRUCTURES FOR INTEGRATED CIRCUITRY AND METHOD OF MAKING THE SAME
3447046 - INTEGRATED COMPLEMENTARY MOS TYPE TRANSISTOR STRUCTURE AND METHOD OF MAKING SAME
3448256 - SEMICONDUCTOR POTENTIOMETRIC DEVICE FOR MULTIPLICATION AND DIVISION
3448344 - MOSAIC OF SEMICONDUCTOR ELEMENTS INTERCONNECTED IN AN XY MATRIX
3448397 - MOS FIELD EFFECT TRANSISTOR AMPLIFIER APPARATUS
3450961 - SEMICONDUCTOR DEVICES WITH A REGION HAVING PORTIONS OF DIFFERING DEPTH AND CONCENTRATION
3450963 - FIELD EFFECT SEMICONDUCTOR DEVICES OF THE JUNCTION TYPE AND METHOD OF MAKING
3460050 - INTEGRATED CIRCUIT AMPLIFIER
3466511 - INSULATED GATE FIELD EFFECT TRANSISTORS WITH MEANS PREVENTING OVERVOLTAGE FEEDTHROUGH BY AUXILIARY STRUCTURE PROVIDING B IPOLAR TRANSISTOR ACTION THROUGH SUBSTRATE
3469155 - PUNCH-THROUGH MEANS INTEGRATED WITH MOS TYPE DEVICES FOR PROTECTION AGAINST INSULATION LAYER BREAKDOWN
3470390 - INTEGRATED BACK-TO-BACK DIODES TO PREVENT BREAKDOWN OF MIS GATE DIELECTRIC
3473977 - SEMICONDUCTOR FABRICATION TECHNIQUE PERMITTING EXAMINATION OF EPITAXIALLY GROWN LAYERS
3480780 - RADIATION SENSITIVE SWITCHING SYSTEM FOR AN ARRAY OF ELEMENTS
3483446 - SEMICONDUCTOR INTEGRATED CIRCUIT INCLUDING A BIDIRECTIONAL TRANSISTOR AND METHOD OF MAKING THE SAME
3486046 - THIN FILM PIEZOELECTRIC RESONATOR
3497773 - PASSIVE CIRCUIT ELEMENTS
3504114 - PHOTOSENSITIVE IMAGE SYSTEM
3504242 - SWITCHING POWER TRANSISTOR WITH THYRISTOR OVERLOAD CAPACITY
3504293 - AMPLIFIER APPARATUS INCLUDING FIELD EFFECT AND BIPOLAR TRANSISTORS SUITABLE FOR INTEGRATION
3505542 - SURFACE WAVE PIEZOELECTRIC RESONATOR
3513356 - ELECTROMECHANICAL TUNING APPARATUS PARTICULARLY FOR MICROELECTRONIC COMPONENTS
3519852 - LOW POWER ANALOG SWITCH
3519891 - THIN FILM RESISTOR AND METHOD FOR
3523200 - SURFACE WAVE PIEZOELECTRIC RESONATOR
3525911 - SEMICONDUCTOR INTEGRATED CIRCUIT INCLUDING IMPROVED DIODE STRUCTURE
3539705 - MICROELECTRONIC CONDUCTOR CONFIGURATIONS AND METHOD OF MAKING THE SAME
3539880 - MIS-FET PERMANENT REPAIR PHYSICAL DEVICE
3544862 - INTEGRATED SEMICONDUCTOR AND PN JUNCTION CAPACITOR
3546542 - INTEGRATED HIGH VOLTAGE SOLAR CELL PANEL
3548346 - TUNING INTEGRATED CIRCUIT COMPRISING A LAYER OF PIEZOELECTRIC MATERIAL ABOVE A SEMICONDUCTOR BODY
3560886 - VARIABLE COUPLING MICROSTRIP PARALLEL-LINE DIRECTIONAL COUPLER
3568012 - LOW THERMAL EXPANSION BINDER
3575646 - INTEGRATED CIRCUIT STRUCTURES INCLUDING CONTROLLED RECTIFIERS
3584270 - HIGH SPEED SWITCHING RECTIFIER
3585461 - HIGH RELIABILITY SEMICONDUCTIVE DEVICES AND INTEGRATED CIRCUITS
3590339 - GATE CONTROLLED SWITCH TRANSISTOR DRIVE INTEGRATED CIRCUIT (THYTRAN)
3590343 - RESONANT GATE TRANSISTOR WITH FIXED POSITION ELECTRICALLY FLOATING GATE ELECTRODE IN ADDITION TO RESONANT MEMBER
3590345 - DOUBLE WALL P-N JUNCTION ISOLATION FOR MONOLITHIC INTEGRATED CIRCUIT COMPONENTS
3590346 - HIGH D/D, FAST TURN-ON DARLINGTON CONTROLLED SEMICONDUCTOR SWITCH
3593174 - SOLID STATE AMPLIFIER FOR MICROWAVE FREQUENCY SIGNALS
3609479 - SEMICONDUCTOR INTEGRATED CIRCUIT HAVING MIS BIPOLAR TRANSISTOR ELEMENTS
3611146 - INTEGRATED MICROWAVE RADIATOR AND GENERATOR
3615938 - METHOD FOR DIFFUSION OF ACCEPTOR IMPURITES INTO SEMICONDUCTORS
3634787 - ELECTROMECHANICAL TUNING APPARATUS PARTICULARLY FOR MICROELECTRONIC COMPONENTS
3641511 - COMPLEMENTARY MOSFET INTEGRATED CIRCUIT MEMORY
3652907 - THIN FILM POWER FET
3657614 - MIS ARRAY UTILIZING FIELD INDUCED JUNCTIONS
3663869 - BIPOLAR-UNIPOLAR TRANSISTOR STRUCTURE
3671819 - METAL-INSULATOR STRUCTURES AND METHOD FOR FORMING
3681134 - MICROELECTRONIC CONDUCTOR CONFIGURATIONS AND METHODS OF MAKING THE SAME
3683335 - NON-VOLATILE MEMORY ELEMENT AND ARRAY

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

WESTINGHOUSE ELECTRIC CORP. (CONTINUED)

3684902 - SEMICONDUCTOR SWITCH DEVICE
3702465 - ELECTRO-OPTIC MASS MEMORY
3710205 - ELECTRONIC COMPONENTS HAVING IMPROVED IONIC STABILITY
3733591 - NON-VOLATILE MEMORY ELEMENT
3781574 - COHERENT SAMPLED READOUT CIRCUIT AND SIGNAL PROCESSOR FOR A CHARGE COUPLED DEVICE ARRAY
3796930 - THIN FILM HIGH VOLTAGE SWITCH
3808674 - EPITAXIAL GROWTH OF THERMICALLY EXPANDABLE FILMS AND PARTICULARLY ANISOTROPIC FERRO-ELECTRIC FILMS
3821566 - METHOD AND APPARATUS FOR ELECTRONICALLY RECOVERING METAL-NITRIDE-OXIDE SEMICONDUCTOR DEVICES EXPOSED TO RADIATION
3836894 - MNOS/SOS RANDOM ACCESS MEMORY
3846820 - MOSAIC FOR IR IMAGING USING PYROELECTRIC SENSORS IN A BIPOLAR TRANSISTOR ARRAY
3851379 - SOLID STATE COMPONENTS
3866310 - METHOD FOR MAKING THE SELF-ALIGNED GATE CONTACT OF A SEMICONDUCTOR DEVICE
3893147 - MULTISTATE VARACTOR
3908182 - NON-VOLATILE MEMORY CELL
3925804 - STRUCTURE OF AND THE METHOD OF PROCESSING A SEMICONDUCTOR MATRIX OR MNOS MEMORY ELEMENTS
4013904 - DARLINGTON TRANSISTOR SWITCHING CIRCUIT FOR REACTIVE LOAD
4042945 - N-CHANNEL MOS TRANSISTOR
4057820 - DUAL GATE MNOS TRANSISTOR
4065781 - INSULATED-GATE THIN FILM TRANSISTOR WITH LOW LEAKAGE CURRENT
4106046 - RADIANT ENERGY SENSOR
4115799 - THIN FILM COPPER TRANSITION BETWEEN ALUMINUM AND INDIUM COPPER FILMS

XEROX CORPORATION

3543031 - DEVICE AND PROCESS FOR IMAGE STORAGE
4133611 - TWO-PAGE INTERWEAVED RANDOM ACCESS MEMORY CONFIGURATION
4163988 - SPLIT GATE V GROOVE FET

ZENITH RADIO CORPORATION

3501676 - SOLID STATE MATRIX HAVING AN INJECTION LUMINESCENT DIODE AS THE LIGHT SOURCE
3600710 - ACOUSTIC SURFACE WAVE FILTER
3699375 - IMAGE DETECTOR INCLUDING SENSOR MATRIX OF FIELD EFFECT ELEMENTS

UNASSIGNED PATENTS(1/75-12/79) INVENTORS(ALPHA LISTING)

INVENTOR NAME			STREET	CITY	ST	ZIP/CNTRY
AKIMOV	JURY	STEPANOVI	ULITSA KOSMONAVTOV, 4, KV. 30	MOSCOW		SU
4055443 - METHOD FOR PRODUCING SEMICONDUCTOR MATRIX OF LIGHT-EMITTING ELEMENTS UTILIZING ION IMPLANTATION AND DIFFUSION HEATING						
BAKER	ROGER	T.	BOX 240	MOUNT TABOR	NJ	07878
4074239 - MEMORY CELL WITH NONDESTRUCTIVE RECALL						
BAKER	ROGER	T.	BOX 240	PARSIPPANY TROY HILL	NJ	07878
3997799 - SEMICONDUCTOR-DEVICE FOR THE STORAGE OF BINARY DATA						
BORDINA	NINEL	MINEEVNA	BOLSHAYA CHERKIZOVSKAYA ULITSA	MOSCOW		SU
3948682 - SEMICONDUCTOR PHOTOELECTRIC GENERATOR						
BUCKLEY	WILLIAM	D.	1035 KIRK RD.	TROY	MI	48084
3877049 - ELECTRODES FOR AMORPHOUS SEMICONDUCTOR SWITCH DEVICES AND METHOD OF MAKING THE SAME						
CHIKOVANI	NODARI	MIKHAILOV	ULITSA KRYLOVA 10	TBILISI		SU
3895272 - THIN-FILM MICROCIRCUIT						
CHOW	PEL		539 KEELSON CIRCLE	REDWOOD CITY	CA	94065
3998673 - METHOD FOR FORMING ELECTRICALLY-ISOLATED REGIONS IN INTEGRATED CIRCUITS UTILIZING SELECTIVE EPITAXIAL GROWTH						
FESTA	THOMAS	A.	5250 ROUND MEADOW RD.	HIDDEN HILLS	CA	91302
4110775 - SCHOTTKY DIODE WITH VOLTAGE LIMITING GUARD BAND						
GARYAINOV	STANISLAV	ALEXANDRO	K-482, KORPUS 328, KV. 75	MOSCOW		SU
3949413 - SEMICONDUCTOR DIODE MATRIX						
HERRMANN	HANS		HEINRICH-HEINE-STRASSE 9	D-783 EMMENDINGEN		DT
3956035 - PLANAR DIFFUSION PROCESS FOR MANUFACTURING MONOLITHIC INTEGRATED CIRCUITS						
HUTSON	JEARLD	L.	P.O. BOX 34235	DALLAS	TX	75234
4079407 - SINGLE CHIP ELECTRONIC SWITCHING CIRCUIT RESPONSIVE TO EXTERNAL STIMULI						
HUTSON	JEARLD	L.	2019 W. VALLEY VIEW LANE	DALLAS	TX	75234
3972014 - FOUR QUADRANT SYMMETRICAL SEMICONDUCTOR SWITCH						
HUTSON	JEARLD	L.	907 NEWBERRY	RICHARDSON	TX	75080
3896477 - MULTILAYER SEMICONDUCTOR SWITCHING DEVICES						
3918082 - SEMICONDUCTOR SWITCHING DEVICE						
INGEBRIGTSEN	KJELL	A.	EINAR OFSTIS VEI 27	7000 TRONDHEIM		NO
4066984 - SURFACE ACOUSTIC WAVE DEVICES FOR PROCESSING AND STORING SIGNALS						
ISITOVSKY	ILYA	LEONIDOVI	15 PARKOVAYA ULITSA, 43, KORPU	MOSCOW		SU
3870576 - METHOD OF MAKING A PROFILED P-N JUNCTION IN A PLATE OF SEMICONDUCTIVE MATERIAL						
KHRENOV	EVGENY	NIKOLAEVI	K-482, KORPUS 323, KV. 30	MOSCOW		SU
3949413 - SEMICONDUCTOR DIODE MATRIX						
KURINNY	VLADIMIR	IVANOVICH	ULITSA VAVILOVA, 58, KORPUS 2,	MOSCOW		SU
4055443 - METHOD FOR PRODUCING SEMICONDUCTOR MATRIX OF LIGHT-EMITTING ELEMENTS UTILIZING ION IMPLANTATION AND DIFFUSION HEATING						

UNASSIGNED PATENTS(1/75-12/79) INVENTORS(ALPHA LISTING)

INVENTOR NAME			STREET	CITY	ST	ZIP/CNTRY
LANDSMAN	ARKADY	PAVLOVICH	RIZHSKY PROEZD, 3, KV. 140	MOSCOW		SU
3948682 - SEMICONDUCTOR PHOTOELECTRIC GENERATOR						
LICHTBLAU	GEORGE	JAY	106 W. WOOSTER ST.	DANBURY	CT	06810
4021705 - RESONANT TAG CIRCUITS HAVING ONE OR MORE FUSIBLE LINKS						
LIN	HUNG	CHANG	8 SCHINDLER CT.	SILVER SPRING	MD	20903
3893152 - METAL NITRIDE OXIDE SEMICONDUCTOR INTEGRATED CIRCUIT STRUCTURE						
MELEN	ROGER	D.	565 ARASTRADERO, NO. 304	PALO ALTO	CA	94306
4041519 - LOW TRANSIENT EFFECT SWITCHING DEVICE AND METHOD						
NISHIZAWA	JUN-ICHI		NO. 6-16, KOMEGAFUKURO 1-CHOME	SENDAI		JA
3896484 - INTRINSIC SEMICONDUCTOR CHARGE TRANSFER DEVICE USING ALTERNATE TRANSFER OF ELECTRONS AND HOLES						
OUYANG	PAUL	H.	936 JUNESONG WAY	SAN JOSE	CA	95133
4131907 - SHORT-CHANNEL V-GROOVE COMPLEMENTARY MOS DEVICE						
OUYANG	PAUL	HSIUNG	950 LARKSPUR AVE.	SUNNYVALE	CA	94086
4065783 - SELF-ALIGNED DOUBLE IMPLANTED SHORT CHANNEL V-GROOVE MOS DEVICE						
RODGERS	THURMAN	J.	271 LELAND ST	PALO ALTO	CA	94306
3878552 - BIPOLAR INTEGRATED CIRCUIT AND METHOD						
RUDIN	MARVIN	B.	SUITE R101, 555 MIDDLEFIELD RO	MOUNT VIEW	CA	94040
4016483 - MICROMINIATURE INTEGRATED CIRCUIT IMPEDANCE DEVICE INCLUDING WEIGHTED ELEMENTS AND CONTACTLESS SWITCHING MEANS FOR FIXIN G THE IMPE						
RZHANOV	VENIAMIN	GAVRILOVI	K-460, KORPUS 212, KV. 57	MOSCOW		SU
3949413 - SEMICONDUCTOR DIODE MATRIX						
SHIBA	HIROSHI		C/O NIPPON ELECTRIC COMPANY, L	TOKYO		JA
3862017 - METHOD FOR PRODUCING A THIN FILM PASSIVE CIRCUIT ELEMENT						
SHIER	JOHN	S.	519 N. CASTLEROCK TER.	SUNNYVALE	CA	94087
4116732 - METHOD OF MANUFACTURING A BURIED LOAD DEVICE IN AN INTEGRATED CIRCUIT						
SMOLKO	GENNADY	GRIGORIEV	K-482, KORPUS 501, KV. 19	MOSCOW		SU
3895272 - THIN-FILM MICROCIRCUIT						
STERN	ERNEST		31 OXBOW ROAD	CONCORD	MA	01742
4066984 - SURFACE ACOUSTIC WAVE DEVICES FOR PROCESSING AND STORING SIGNALS						
STREBKOV	DMITRY	SEMENOVIC	KIROVOGRADSKY PROEZD, 3, KORPU	MOSCOW		SU
3948682 - SEMICONDUCTOR PHOTOELECTRIC GENERATOR						
SUSHKOV	VALERY	PETROVICH	ULITSA ONEZHSKAY, 45/19, KV. 1	MOSCOW		SU
4055443 - METHOD FOR PRODUCING SEMICONDUCTOR MATRIX OF LIGHT-EMITTING ELEMENTS UTILIZING ION IMPLANTATION AND DIFFUSION HEATING						
TAKAMIYA	SABURO			ITAMI, HYOGO		JA
3911468 - MAGNETIC-TO-ELECTRIC CONVERSION SEMICONDUCTOR DEVICE						

UNASSIGNED PATENTS(1/75-12/79) INVENTORS(ALPHA LISTING)

INVENTOR NAME			STREET	CITY	ST	ZIP/CNTRY
TSUNEMITSU	HIDEO		C/O NIPPON ELECTRIC COMPANY, L	TOKYO		JA
3862017 - METHOD FOR PRODUCING A THIN FILM PASSIVE CIRCUIT ELEMENT						
UNISHKOV	VADIM	ALEXEEVIC	ULITSA BAZHOVA, 15, KORPUS 1,	MOSCOW		SU
3948682 - SEMICONDUCTOR PHOTOELECTRIC GENERATOR						
ZELIKMAN	GRIGORY	AVRUMOVIC	ULITSA ALEXEYA TOLSTOGA, 26, K	MOSCOW		SU
3870576 - METHOD OF MAKING A PROFILED P-N JUNCTION IN A PLATE OF SEMICONDUCTIVE MATERIAL						

PATENTS (1/63-12/79) WITH NEITHER ASSIGNMENT NOR INVENTOR INFORMATION IN DATABASE

3430109 - SOLID-STATE DEVICE WITH DIFFERENTIALLY EXPANDED JUNCTION SURFACE
3437876 - AUTOMOTIVE SEMICONDUCTOR IGNITION CONTROL APPARATUS
3457475 - SEMICONDUCTOR DEVICE WITH INTEGRAL ELECTRODES, CONSTITUTING A UNITARY VITREOUS STRUCTURE
3460006 - WESTINGHOUSE ELECTRIC CORPORATION SEMICONDUCTOR INTEGRATED CIRCUITS WITH IMPROVED ISOLATION
3465213 - SELF COMPENSATING STRUCTURE FOR LIMITING BASE DRIVE CURRENT IN TRANSISTORS
3475666 - INTEGRATED SEMICONDUCTOR SWITCH SYSTEM
3480830 - MULTI-LAYER PN JUNCTION SEMICONDUCTIVE FLYING SPOT GENERATOR
3482151 - BISTABLE SEMICONDUCTOR INTEGRATED DEVICE
3488542 - LIGHT EMITTING HETEROJUNCTION SEMICONDUCTOR DEVICES
3492513 - MESA T-BAR PIEZORESISTOR
3510094 - METHOD AND MEANS FOR REDUCING THE SKIN FRICTION OF BODIES MOVING IN A FLUID MEDIUM
3513365 - FIELD-EFFECT INTEGRATED CIRCUIT AND METHOD OF FABRICATION
3535599 - FIELD EFFECT SEMICONDUCTOR DEVICE WITH MULTIPLE CHANNEL REGIONS SELECTIVELY SWITCHED FROM CONDUCTING TO NONCONDUCTING
3558897 - P-N CONDUCTORS DISPOSED ON DEVICE WITH FIELD EFFECT LAYERS FOR CONTROLLING POSITION OF SCANNING SPOT
3560963 - FIELD EFFECT A/D CONVERTER
3574926 - PROCESS FOR SERIES PRODUCTION OF AN ELECTRIC RESISTANCE FOR A HYBRID MINIATURISED CIRCUIT AND THE RESISTANCE THUS OBTAINED
3576476 - MESH EMITTER TRANSISTOR WITH SUBDIVIDED EMITTER REGIONS
3585714 - METHOD FOR MAKING SOLID-STATE DEVICES
3590173 - BUS BAR HOUSING AND RUNWAY FOR ELECTRICAL COLLECTOR HEAD
3617827 - SEMICONDUCTOR DEVICE WITH COMPLEMENTARY TRANSISTORS
3620851 - METHOD FOR MAKING A BURIED LAYER SEMICONDUCTOR DEVICE
3624315 - TRANSDUCER APPARATUS AND TRANSDUCER AMPLIFIER SYSTEM UTILIZING INSULATED GATE SEMICONDUCTOR FIELD EFFECT DEVICES
3631251 - ARRAY COMPRISING ROW OF ELECTRO-OPTICAL ELEMENTS AND ASSOCIATED ROW OF SEMICONDUCTING MICROCIRCUITS LOCATED ON ADJOINING FACES OF
3646408 - SEMICONDUCTOR WIRELESS VOLTAGE AMPLIFIER MOUNTED ON A DIELECTRIC SUBSTRATE
3649837 - DIFFRACTIVE IMAGE-FORMING MEANS INTEGRATED INTO SEMICONDUCTING DEVICES
3652906 - MOSFET DECODER TOPOLOGY
3656146 - INTEGRATED CIRCUIT CHARACTER GENERATOR
3659159 - OPTOELECTRONIC DISPLAY PANEL
3665263 - AIR-ISOLATED INTEGRATED CIRCUIT DEVICES TO FACILITATE THE CONNECTION THEREOF TO CIRCUIT BOARDS
3668404 - ELECTRO-OPTICAL MICROTRANSDUCER COMPRISING DIFFRACTIVE ELEMENT MONOLITHICALLY INTEGRATED WITH PHOTOELECTRIC DEVICE
3688132 - HIGH FREQUENCY INTEGRATED CIRCUIT HAVING CIRCUIT ELEMENTS IN SEPARATE AND MUTUALLY SPACED ISOLATION REGIONS
3688165 - FIELD EFFECT SEMICONDUCTOR DEVICES
3694670 - EASILY SWITCHED SILICON CONTROLLED RECTIFIER
3715633 - SEMICONDUCTOR UNIT WITH INTEGRATED CIRCUIT
3725148 - INDIVIDUAL DEVICE TUNING USING LOCALIZED SOLID-STATE REACTIONS
3748479 - ARRAYS OF ELECTRO-OPTICAL ELEMENTS AND ASSOCIATED ELECTRIC CIRCUITRY
3757175 - COMPOSITE INTEGRATED CIRCUITS WITH COPLANAR CONNECTIONS TO SEMICONDUCTOR CHIPS MOUNTED ON A SINGLE SUBSTRATE

PATENTS (1/63-12/79) WITH NEITHER ASSIGNMENT NOR INVENTOR INFORMATION IN DATABASE

3768150 - INTEGRATED CIRCUIT PROCESS UTILIZING ORIENTATION DEPENDENT SILICON ETCH
3771030 - LARGE SCALE INTEGRATED CIRCUIT OF REDUCED AREA INCLUDING COUNTER
3781610 - THIN FILM CIRCUITS AND METHOD FOR MANUFACTURE
3786560 - ELECTRICAL ISOLATION OF CIRCUIT COMPONENTS OF INTEGRATED CIRCUITS
3787710 - INTEGRATED CIRCUIT STRUCTURE HAVING ELECTRICALLY ISOLATED CIRCUIT COMPONENTS
3794883 - PROCESS FOR FABRICATING GE:HG INFRARED DETECTOR ARRAYS AND RESULTING ARTICLE OF MANUFACTURE
3796929 - JUNCTION ISOLATED INTERGRATED CURCUIT RESISTOR WITH CRYSTAL DAMAGE NEAR ISOLATION JUNCTION
3805130 - SEMICONDUCTOR DEVICE
3813584 - SOLID STATE INTEGRATED CIRCUITS
3815106 - FLIP-FLOP MEMORY CELL ARRANGEMENT
3821782 - HIGH VOLTAGE SEMICONDUCTOR DEVICE WITH PLURAL GROOVES
3878549 - SEMICONDUCTOR MEMORIES

3074003	3077578	3079484	3079512	3090873	3092733	3094634	3097336	3100276	3100838	3103599	3109942
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3315248	3316128	3316466	3317653	3317746	3317850	3319140	3319174	3320439	3320484	3320485	3320550
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3374408	3377215	3377258	3377513	3377528	3378688	3378783	3379577	3379584	3379931	3379937	3379940
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3383760	3384556	3384792	3384832	3384879	3385729	3386008	3386015	3386016	3386163	3386864	3386865
3387133	3387193	3387286	3388255	3388301	3388302	3388394	3390012	3390019	3390022	3390273	3390280
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3397370	3397447	3397448	3398337	3399353	3399390	3400271	3400309	3400310	3400335	3401055	3401294
3401319	3401349	3401357	3401450	3402081	3402330	3402331	3402332	3403270	3403306	3403439	3404321
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3409483	3411048	3411051	3411052	3411054	3411200	3412295	3412296	3412460	3413573	3413712	3414434
3414441	3414737	3414740	3414779	3414782	3414783	3414832	3415680	3416008	3416036	3416042	3416043
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3418592	3419765	3419767	3872450								

INTEGRATED CIRCUIT STRUCTURE

PATENTING UPDATE

ASSIGNEES WITH 2 OR MORE PATENTS (1/80-10/80)

INTERNATIONAL BUSINESS MACHINES CORPORATION	19
RCA CORPORATION	12
TEXAS INSTRUMENTS, INC.	11
TOKYO SHIBAURA ELECTRIC CO., LTD.	9*
SIEMENS AKTIENGESELLSCHAFT	8
U.S. PHILIPS CORPORATION	6
FUJITSU LIMITED	5
NATIONAL SEMICONDUCTOR CORPORATION	5
BELL TELEPHONE LABORATORIES INCORPORATED	4
HARRIS CORPORATION	4
NIPPON GAKKI SEIZO KABUSHIKI KAISHA	4
FAIRCHILD CAMERA AND INSTRUMENT CORPORATION	3
MOTOROLA INC.	3
NIPPON ELECTRIC CO., LTD.	3
ROCKWELL INTERNATIONAL CORPORATION	3
TEKTRONIX INC.	3
AMERICAN MICROSYSTEMS, INC.	2
BURROUGHS CORPORATION	2
HITACHI, LTD.	2
MASSACHUSETTS INSTITUTE OF TECHNOLOGY	2
MICROWAVE SEMICONDUCTOR CORP	2
NCR CORPORATION	2
SANYO ELECTRIC CO., LTD.	2

*COMPOSITE TOTAL, SEE APPENDIX A

United States Patent [19]

Burke et al.

[11] **4,183,034**

[45] **Jan. 8, 1980**

[54] **PIN PHOTODIODE AND INTEGRATED CIRCUIT INCLUDING SAME**

[75] Inventors: **Richard G. Burke**, Raleigh; **James S. Kolodzey**, Chapel Hill, both of N.C.

[73] Assignee: **International Business Machines Corp.**, Armonk, N.Y.

[21] Appl. No.: **896,872**

[22] Filed: **Apr. 17, 1978**

[51] **Int. Cl.**[2] **H01L 27/14**

[52] **U.S. Cl.** **357/30**; 357/58; 357/40; 357/19

[58] **Field of Search** 357/30, 58, 40, 19

[56] **References Cited**

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3,959,646	5/1976	deCremoux	250/211 J

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Melchior et al., *Proceedings of the IEEE*, vol. 58, No. 10, Oct. 1970, pp. 1466–1486.

Mathur et al., International Electron Device Meeting, (abstract), Wash., D.C. Oct. 1968.

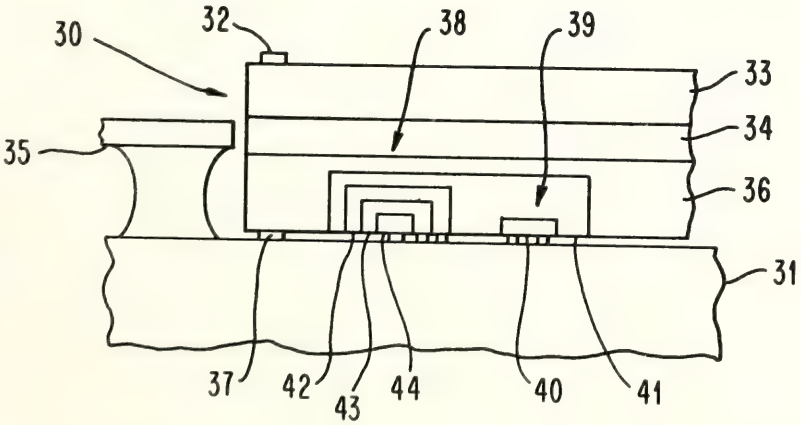
Primary Examiner—Martin H. Edlow

Attorney, Agent, or Firm—John B. Frisone

[57] **ABSTRACT**

A PIN photodiode structure uses direct side entry into the I region, thus permitting the use of thicker P and N regions with a comparatively thin I region without sacrificing speed and results in more constant spatial distribution upon carrier generation and longer wave length devices with conventional speeds or smaller devices at faster speeds, and may be integrated on the same chip with associated circuits.

10 Claims, 7 Drawing Figures



United States Patent [19]

Rideout

[11] **4,183,040**

[45] **Jan. 8, 1980**

[54] **MOS RAM WITH IMPLANT FORMING PERIPHERAL DEPLETION MOSFET CHANNELS AND CAPACITOR BOTTOM ELECTRODES**

[75] Inventor: **Vincent L. Rideout**, Mohegan Lake, N.Y.

[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[21] Appl. No.: **874,006**

[22] Filed: **Jan. 31, 1978**

Related U.S. Application Data

[60] Division of Ser. No. 702,247, Jul. 2, 1976, Pat. No. 4,085,498, which is a continuation-in-part of Ser. No. 656,756, Feb. 9, 1976, Pat. No. 4,075,045.

[51] **Int. Cl.**[2] **H01L 27/04**; H01L 29/78; H01L 29/94

[52] **U.S. Cl.** **357/41**; 357/23; 357/45; 357/59; 357/89; 357/51

[58] **Field of Search** 357/23, 41, 45, 91; 307/238

[56] **References Cited**

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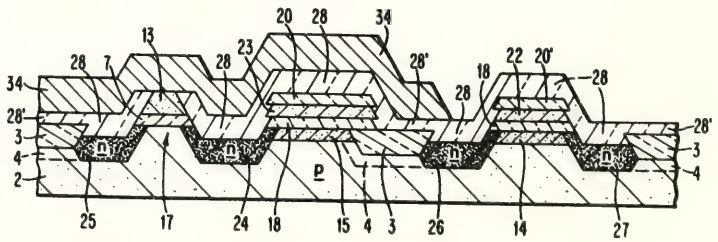
Primary Examiner—William D. Larkins

Attorney, Agent, or Firm—Pollock, Vande Sande and Priddy

[57] **ABSTRACT**

In a one transistor, one capacitor N-channel polysilicon gate MOSFET RAM, having self-aligned contacts to silicon gates, an N-implant is used to both form bottom electrodes of the capacitors and to form depletion mode FET channels in peripheral circuits. Separate polysilicon layers are used for the gates of enhancement mode FETs and for the capacitor upper electrodes and depletion FET gates.

7 Claims, 18 Drawing Figures



United States Patent [19]

Esch et al.

[11] **4,186,408**

[45] **Jan. 29, 1980**

[54] **IGFET WITH PARTIAL PLANAR OXIDE**

[75] Inventors: **Ronald P. Esch; Patrick C. Huang,** both of Manassas, Va.

[73] Assignee: **International Business Machines Corporation,** Armonk, N.Y.

[21] Appl. No.: **819,641**

[22] Filed: **Jul. 27, 1977**

Related U.S. Application Data

[60] Continuation of Ser. No. 579,102, May 20, 1975, abandoned, which is a division of Ser. No. 411,518, Oct. 31, 1973, Pat. No. 3,899,372.

[51] **Int. Cl.**[2] **H01L 29/78**

[52] **U.S. Cl.** **357/23;** 357/50; 357/52; 357/54

[58] **Field of Search** 357/23, 50, 52

[56] **References Cited**

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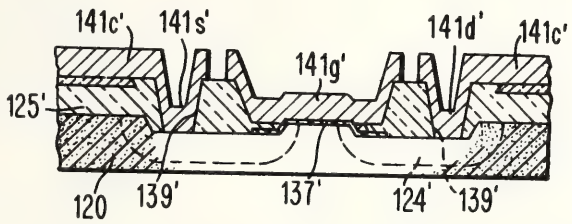
4,043,848	8/1977	Bazin	357/23

Primary Examiner—William D. Larkins
Attorney, Agent, or Firm—Maurice H. Klitzman

[57] **ABSTRACT**

The invention is a process of fabricating semiconductor devices including an insulating film across the surface that has a planar configuration. Alternatively, the film may be of uniform thickness and non-planar configuration. Both the planar and uniform thickness characteristics of the insulating film permit openings to be formed therein without over etching a defined surface area and conductors to be formed thereon without broadening. An important feature of the invention is utilizing the differential growth rate of films on semiconductor surfaces and/or selection of a suitable initial film thickness as a diffusion mask. The initial film thickness also contributes to a planar or uniform film thickness or other configuration across the device.

1 Claim, 9 Drawing Figures



United States Patent [19]

Bhattacharyya et al.

[11] **4,190,466**

[45] **Feb. 26, 1980**

[54] **METHOD FOR MAKING A BIPOLAR TRANSISTOR STRUCTURE UTILIZING SELF-PASSIVATING DIFFUSION SOURCES**

[75] Inventors: **Arup Bhattacharyya,** Essex Center; **Francis W. Wiedman, III,** Stowe, both of Vt.

[73] Assignee: **International Business Machines Corporation,** Armonk, N.Y.

[21] Appl. No.: **863,182**

[22] Filed: **Dec. 22, 1977**

[51] **Int. Cl.**[2] **H01L 21/265;** H01L 21/225; H01L 21/31

[52] **U.S. Cl.** **148/1.5;** 29/578; 29/590; 29/591; 148/187; 148/188; 148/190; 148/174; 156/653; 156/657; 156/662; 357/34; 357/36; 357/45; 357/50; 357/51; 357/59; 357/91; 427/86

[58] **Field of Search** ..... 148/1.5, 187, 174, 188, 148/190; 29/576 B, 578, 590, 591; 357/34, 36, 45, 50, 51, 59, 91; 427/85, 86; 156/653, 657, 662; 307/238

[56] **References Cited**

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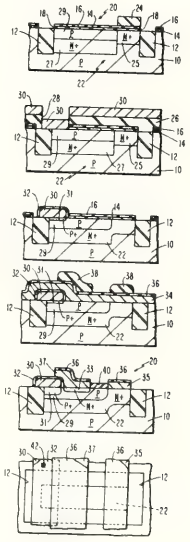
Primary Examiner—L. Dewayne Rutledge
Assistant Examiner—W. G. Saba
Attorney, Agent, or Firm—Stephen J. Limanek

[57] **ABSTRACT**

A semiconductor structure, formed within a recessed oxide isolation region, includes a semiconductor substrate of a first conductivity type within which a collector of opposite conductivity type is formed below the surface of the substrate and extending in part to the surface of the substrate for ease of contact. A first layer of doped polycrystalline silicon or polysilicon is formed on a first portion of the surface of the substrate and in electrical contact with the substrate which acts as the base of a transistor. The first polysilicon layer is oxidized to form an outer insulating layer thereover. A second doped polysilicon layer is disposed over the outer insulating layer onto a second portion of the surface of the substrate so as to be spaced from the first portion by only the thickness of the outer insulating layer on the first polysilicon layer. The dopant in the second polysilicon layer is driven into the surface of the semiconductor substrate to form an emitter therein. Means, which may include a portion of the second polysilicon layer, are provided for electrically contacting the collector to thus form a completed compact bipolar transistor which has very high performance.

28 Claims, 12 Drawing Figures



United States Patent [19]

Anantha et al.

[11] **4,196,440**

[45] **Apr. 1, 1980**

[54] **LATERAL PNP OR NPN WITH A HIGH GAIN**

[75] Inventors: **Narasipur G. Anantha**, Hopewell Junction; **Harsaran S. Bhatia**; **Santosh P. Gaur**, both of Wappingers Falls; **Hans B. Pogge**, Hopewell Junction, all of N.Y.

[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[21] Appl. No.: **909,338**

[22] Filed: **May 25, 1978**

[51] **Int. Cl.**[2] **H01L 29/06**

[52] **U.S. Cl.** **357/35**; 357/49; 357/44; 357/55

[58] **Field of Search** 357/35, 44, 49, 40, 357/55

[56] **References Cited**

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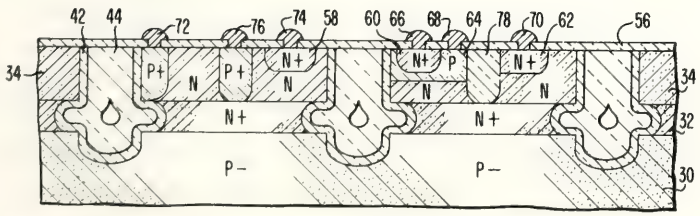
4,051,506	9/1977	Horie	357/55
4,110,779	8/1978	Rathbone	357/34

Primary Examiner—Martin H. Edlow
Attorney, Agent, or Firm—George O. Saile

[57] **ABSTRACT**

Lateral PNP or NPN devices in isolated monocrystalline silicon pockets wherein silicon dioxide isolation surrounds the pocket and partially, below the surface, within the isolated monocrystalline region are described. The P emitter or N emitter diffusion is made over the portion of the silicon dioxide that partially extends into the monocrystalline isolated pocket. This structure reduces the vertical current injection which will give relatively high (beta) gain even at low base to emitter voltages.

10 Claims, 6 Drawing Figures



United States Patent [19]

Harris

[11] **4,204,130**

[45] **May 20, 1980**

[54] **MULTICOLLECTOR TRANSISTOR LOGIC CIRCUIT**

[75] Inventor: **James H. Harris**, Danbury, Conn.

[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[21] Appl. No.: **891,240**

[22] Filed: **Mar. 29, 1978**

[51] **Int. Cl.**[2] **H01L 27/04**; H03K 19/08

[52] **U.S. Cl.** **307/215**; 307/213; 357/36; 357/44; 357/46; 357/92

[58] **Field of Search** 357/44, 46, 35, 36; 357/92; 307/213, 215

[56] **References Cited**

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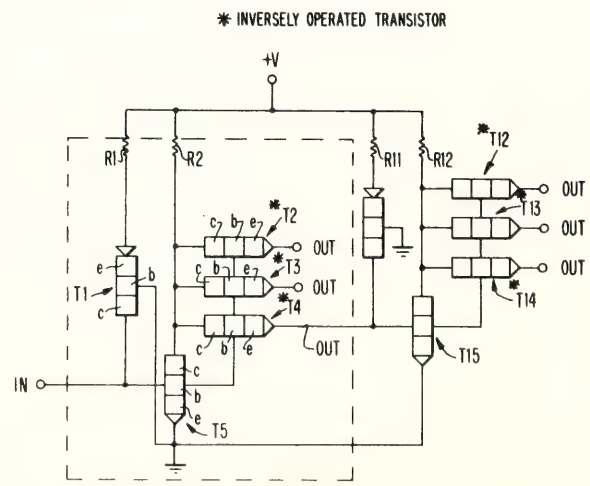
Primary Examiner—William D. Larkins
Attorney, Agent, or Firm—Theodore E. Galanthay

[57] **ABSTRACT**

Disclosed is an integrated transistor logic circuit (ITL) comprising complementary bipolar transistors. A PNP transistor injects current into the base of an NPN transistor when this current is not steered away. The base of the PNP transistor and the emitter of the NPN transistor are connected in common to a fixed source of potential. The collector of the NPN transistor is formed in common with the collector regions of one or more output transistors while the base region of the NPN transistor is formed in common with the base regions of the output transistors. The one or more output transistors are operated in the inverted mode providing an output signal at their respective emitter regions.

11 Claims, 3 Drawing Figures



United States Patent [19]
Ho et al.
[11] **4,209,349**
[45] **Jun. 24, 1980**

[54] **METHOD FOR FORMING A NARROW DIMENSIONED MASK OPENING ON A SILICON BODY UTILIZING REACTIVE ION ETCHING**

[75] Inventors: **Irving T. Ho; Jacob Riseman,** both of Poughkeepsie, N.Y.

[73] Assignee: **International Business Machines Corp.,** Armonk, N.Y.

[21] Appl. No.: **957,605**

[22] Filed: **Nov. 3, 1978**

[51] **Int. Cl.**[2] **H01L 21/302;** H01L 21/76

[52] **U.S. Cl.** ..... **148/187;** 29/578; 148/1.5; 148/174; 148/175; 156/643; 156/653; 156/657; 156/662; 204/192 E; 357/20; 357/49; 357/50; 357/54; 357/56

[58] **Field of Search** ..... 148/1.5, 174, 175, 187; 204/192 E; 156/643, 644, 653, 657, 662; 427/93; 29/578; 357/20, 49, 50, 54, 56

[56] **References Cited**

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4,037,307	7/1977	Smith	29/578 X
4,042,726	8/1977	Kaji et al.	357/50 X
4,063,992	12/1977	Hosack	156/653
4,103,415	8/1978	Hayes	29/578 X
4,124,933	11/1978	Nicholas	148/187 X
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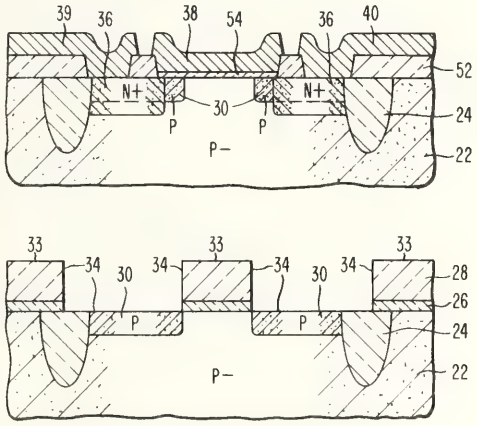
Jambotkar, C. G., "Method for Reducing Emitter-Base Contact . . . " I.B.M. Tech. Discl. Bull., vol. 19, No. 12, May 1977, pp. 4601-4604.

Primary Examiner—L. Dewayne Rutledge
Assistant Examiner—W. G. Saba
Attorney, Agent, or Firm—George O. Saile

[57] **ABSTRACT**

A method for forming a narrow, such as a submicrometer, dimensioned mask opening on a silicon body involving forming a first insulator region having substantially a horizontal surface and a substantially vertical surface. A second insulator is applied on both the horizontal surface and substantially vertical surfaces. The second insulator is composed of a material different from that of the first insulator layer. Reactive ion etching of the second layer removes the horizontal layer and provides a narrow dimensioned second insulator region on the silicon body. The surface of the silicon body is then thermally oxidized. The narrow dimensioned second insulator region is removed to form a narrow dimensioned mask opening.

20 Claims, 17 Drawing Figures



United States Patent [19]
Ho et al.
[11] **4,209,350**
[45] **Jun. 24, 1980**

[54] **METHOD FOR FORMING DIFFUSIONS HAVING NARROW DIMENSIONS UTILIZING REACTIVE ION ETCHING**

[75] Inventors: **Irving T. Ho; Jacob Riseman,** both of Poughkeepsie, N.Y.

[73] Assignee: **International Business Machines Corp.,** Armonk, N.Y.

[21] Appl. No.: **957,599**

[22] Filed: **Nov. 3, 1978**

[51] **Int. Cl.**[2] **H01L 21/302;** H01L 21/225; H01L 21/76

[52] **U.S. Cl.** ..... **148/188;** 29/578; 29/580; 148/1.5; 148/174; 148/175; 148/187; 156/643; 156/653; 156/657; 156/662; 204/192 E; 357/20; 357/48; 357/49; 357/50; 357/54; 357/56; 357/59

[58] **Field of Search** ..... 148/1.5, 174, 175, 187, 148/188; 204/192 E; 156/643, 644, 653, 657, 662; 427/93; 29/578, 580; 357/20, 48, 50, 49, 54, 56, 59

[56] **References Cited**

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4,037,307	7/1977	Smith	29/587 X
4,103,415	8/1978	Hayes	29/578 X
4,124,933	11/1978	Nicholas	148/187 X
4,139,442	2/1979	Bondur et al.	204/192 E
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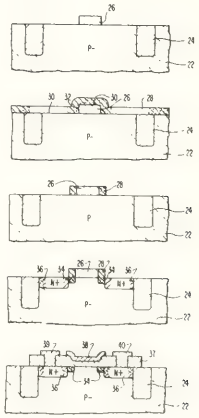
Pogge, H. B., ", Narrow Line With Masking Method" I.B.M. Tech. Discl. Bull., Nov. 1976, vol. 19, No. 6, 1976.
Abbas et al., "Extending Minimal Dimensions . . . Fabrication Processing" Ibid., vol. 20, No. 4, Sep. 1977, pp. 1376-1378.
Bersin, R. L., "Survey of Plasma Etching Processes" Solid-State Tech., May 1976, pp. 31-36.
Jambotkar, C. G., "Method for Reducing Emitter-Base Contact . . . "I.B.M. Tech. Discl. Bull., vol. 19, No. 12, May 1977, pp. 4601-4604.

Primary Examiner—R. Dean
Assistant Examiner—W. G. Saba
Attorney, Agent, or Firm—George O. Saile

[57] **ABSTRACT**

A method for forming diffusions having narrow, for example, submicrometer dimensions in a silicon body which involves forming insulator regions on a silicon body, which insulator regions have substantially horizontal surfaces and substantially vertical surfaces. A layer having a desired dopant concentration is formed thereon, both on the substantially horizontal surfaces and the substantially vertical surfaces. Reactive ion etching of the layer acts to substantially remove only the horizontal layer and provides a narrow dimensioned layer having a desired dopant concentration in the substantially vertical surfaces. Heating of the body at a suitable temperature is accomplished so as to produce the movement of the dopant into the silicon body by diffusion to form diffusions having narrow, such as submicrometer dimensions, therein.

18 Claims, 19 Drawing Figures



United States Patent [19]

Horng et al.

[11] **4,211,582**

[45] **Jul. 8, 1980**

[54] **PROCESS FOR MAKING LARGE AREA ISOLATION TRENCHES UTILIZING A TWO-STEP SELECTIVE ETCHING TECHNIQUE**

[75] Inventors: **Cheng T. Horng**, Fishkill, N.Y.; **Robert O. Schwenker**, San Jose, Calif.

[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[21] Appl. No.: **52,997**

[22] Filed: **Jun. 28, 1979**

[51] **Int. Cl.**[2] **H01L 21/76**; H01L 21/306

[52] **U.S. Cl.** ..... **148/1.5**; 29/576 W; 29/578; 29/580; 148/175; 148/187; 156/643; 156/644; 156/653; 156/657; 156/662; 204/192 E; 357/49; 357/50; 357/55; 357/56

[58] **Field of Search** ..... 148/1.5, 175, 187; 204/192 E; 156/643, 644, 653, 657, 662; 29/576 W, 578, 580; 357/49, 50, 55, 56

[56] **References Cited**

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4,042,726	8/1977	Kaji et al.	156/653 X
4,044,452	8/1977	Abbas et al.	357/50 X
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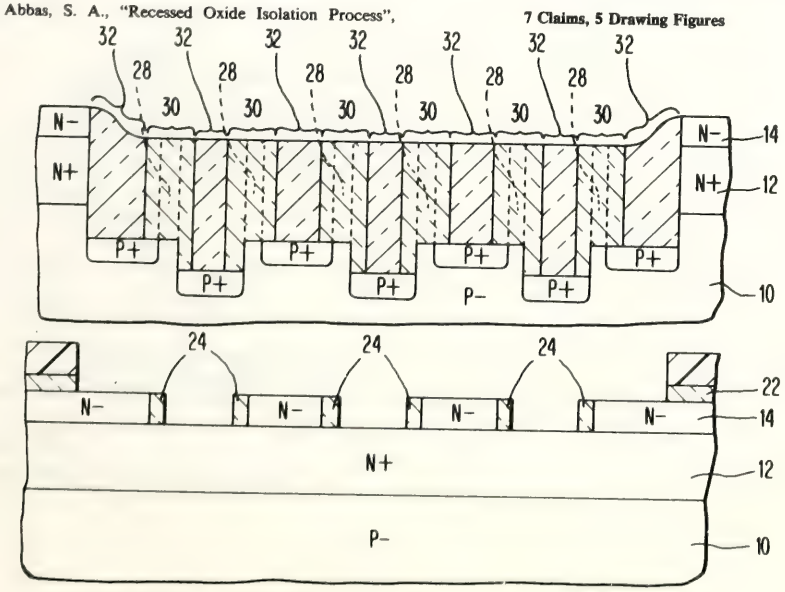
Primary Examiner—R. Dean
Assistant Examiner—W. G. Saba
Attorney, Agent, or Firm—Robert J. Haase

[57] **ABSTRACT**

A method for making wide, deep recessed oxide isolation trenches in silicon semiconductor substrates. A semi-conductor substrate is selectively etched to produce a spaced succession of narrow, shallow trenches separated by narrow silicon mesas. Silicon oxide is chemical-vapor-deposited on the horizontal and vertical surfaces of the etched structure to a thickness equalling the width of a desired silicon oxide mask. The mask is used for etching multiple deep trenches in the substrate, the trenches being separated by thin walls of silicon. The thickness of the walls is uniformly equal to and determined by the thickness of the deposited silicon oxide mask.

The deposited silicon oxide is reactively ion etched away from the horizontal surfaces, leaving the oxide only on the sidewalls of the shallow trenches. The silicon is deeply etched, using the remaining oxide as a mask. Boron is ion implanted and the resulting structure is thermally oxidized sufficiently to completely oxidize the silicon under the deposited oxide mask and to oxidize the silicon surfaces at the bottoms of the trenches. The remaining trench volume is filled in with chemical-vapor-deposited silicon dioxide.

7 Claims, 5 Drawing Figures



United States Patent [19]

Fang et al.

[11] **4,211,586**

[45] **Jul. 8, 1980**

[54] **METHOD OF FABRICATING MULTICOLOR LIGHT EMITTING DIODE ARRAY UTILIZING STEPPED GRADED EPITAXIAL LAYERS**

[75] Inventors: **Frank F. Fang; Kwang K. Shih**, both of Yorktown Heights, N.Y.

[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[21] Appl. No.: **957,966**

[22] Filed: **Nov. 6, 1978**

Related U.S. Application Data

[62] Division of Ser. No. 835,097, Sep. 21, 1977, Pat. No. 4,148,045.

[51] **Int. Cl.**[2] **H01L 21/20**; H01L 29/205

[52] **U.S. Cl.** ..... **148/175**; 29/569 L; 29/577 R; 29/578; 29/580; 148/171; 148/173; 313/500; 357/16; 357/17; 357/45; 357/46; 357/88; 357/90

[58] **Field of Search** ..... 148/171–173, 148/175; 29/569 L, 577, 578, 580; 357/16, 17, 45, 46, 88, 90; 250/211 J; 307/311; 313/500

[56] **References Cited**

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Murray et al., "Lighting Up in a Group" Electronics, Mar. 4, 1968, pp. 104–110.

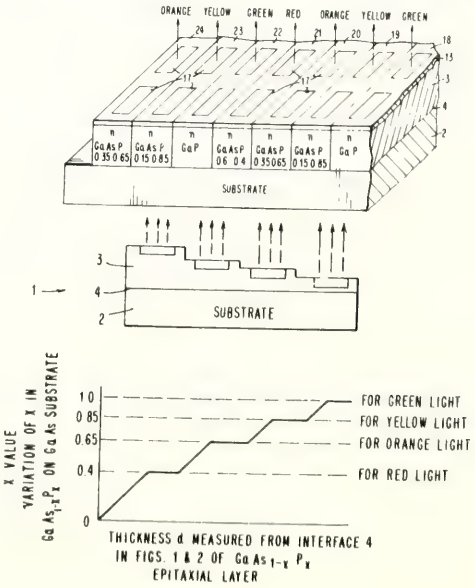
Craford et al., "LED Technology" Solid State Technology, Jan. 1974, pp. 39–58.

Primary Examiner—L. Dewayne Rutledge
Assistant Examiner—W. G. Saba
Attorney, Agent, or Firm—Alvin J. Riddles

[57] **ABSTRACT**

Multicolor light emitting diode arrays can be made using a binary semiconductor substrate on which is grown a graded epitaxial region of an $AB_{1-x}C_x$ semiconductor. Diodes emitting various light colors can selectively be formed in different regions of the gradient by etching away a portion of the graded region. Arrays of colored light emitting diodes can be made by the techniques of diffusion and selective etching of the graded material.

5 Claims, 7 Drawing Figures



United States Patent [19]

Balasubramanian et al.

[11] **4,212,026**

[45] **Jul. 8, 1980**

[54] **MERGED ARRAY PLA DEVICE, CIRCUIT, FABRICATION METHOD AND TESTING TECHNIQUE**

[75] Inventors: **P. S. Balasubramanian**, Manassas; **Claude R. Bertin**, Oakton; **Stephen B. Greenspan**, Reston, all of Va.

[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[21] Appl. No.: **945,745**

[22] Filed: **Sep. 25, 1978**

Related U.S. Application Data

[62] Division of Ser. No. 809,877, Jun. 24, 1977.

[51] **Int. Cl.**[2] **H01L 27/02**

[52] **U.S. Cl.** **357/41**; 357/44; 357/45; 357/46; 357/59; 357/68

[58] **Field of Search** 357/41, 44, 45, 46, 357/59, 68

[56] **References Cited**

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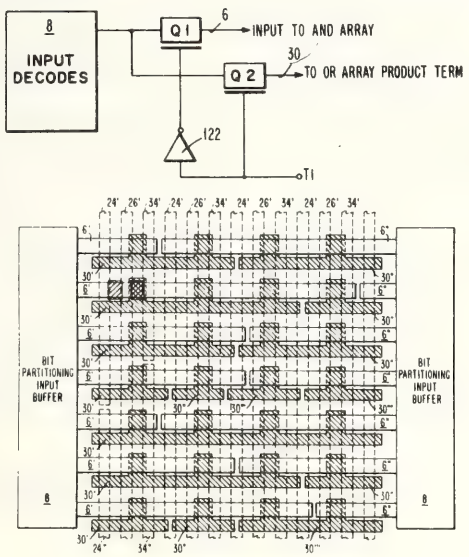
IBM-TDB-vol. 19, No. 3, Aug. 1976, pp. 993-995.

Primary Examiner—Edward J. Wojciechowicz
Attorney, Agent, or Firm—John E. Hoel

[57] **ABSTRACT**

A merged AND/OR array PLA is disclosed wherein the merger is accomplished by forming the gates of the FET devices in the AND array by means of an upper conductor layer and the gates of the FET devices in the OR array, which are connected to the drain of the devices in the AND array, by means of lower level conductor layer, so that the devices are contiguous. The PLA structure uses a polysilicon layer for interconnection between AND array FET drains and OR array FET gates, with the AND array FETs and OR array FETs being intermixed in a single array. The OR array outputs are oriented vertically, alternating between the AND product terms and ground diffusions. All PLA outputs are oriented vertically within the same array. Orienting the polycrystalline silicon line parallel to the input line and orienting the axes of the centroids for the AND FETs and the OR FETs parallel to the input line allows a retention of the high density for the array by permitting the placement of output latches on the top and bottom edges of the array and the placement of the input driver/decoder circuits on the lateral edges of the array so that the close pitch of the array can be maintained. Several alternate device structures and their methods of fabrication are disclosed for implementing the merged array PLA. A testing technique and special testing circuitry is disclosed which makes use of the existing bit partitioning input buffer as the source of test patterns and the existing output latches as the storage for the test response bits for individually testing both the AND components and the OR components in the merged array PLA.

17 Claims, 33 Drawing Figures



United States Patent [19]

Anantha et al.

[11] **4,214,315**

[45] **Jul. 22, 1980**

[54] **METHOD FOR FABRICATING VERTICAL NPN AND PNP STRUCTURES AND THE RESULTING PRODUCT**

[75] Inventors: **Narasipur G. Anantha**, Hopewell Junction; **Harsaran S. Bhatia**, Wappingers Falls; **James L. Walsh**, Hyde Park, all of N.Y.

[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[21] Appl. No.: **21,123**

[22] Filed: **Mar. 16, 1979**

Related U.S. Application Data

[62] Division of Ser. No. 844,767, Oct. 25, 1977, Pat. No. 4,159,915.

[51] **Int. Cl.**[2] **H01L 27/02**

[52] **U.S. Cl.** **357/44**; 357/49; 357/50; 357/15; 357/92

[58] **Field of Search** 357/44, 49, 50, 15, 357/92

[56] **References Cited**

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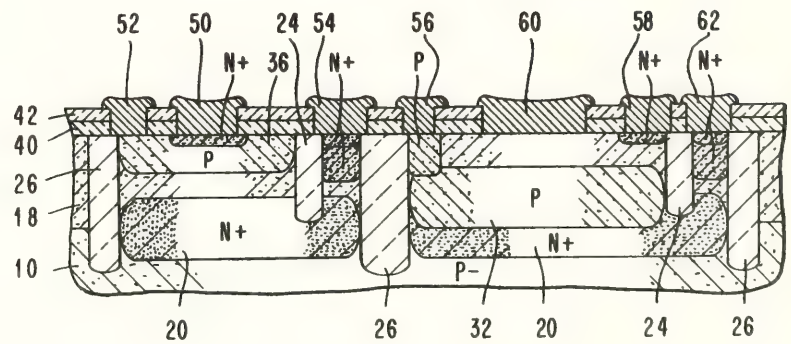
4,160,991	10/1979	Anantha	357/49

Primary Examiner—Martin H. Edlow
Attorney, Agent, or Firm—George O. Saile

[57] **ABSTRACT**

A method is given for fabricating vertical NPN and PNP structures on the same semiconductor body. The method involves providing a monocrystalline semiconductor substrate having regions of monocrystalline silicon isolated from one another by isolation regions. Buried regions are formed overlapping the juncture of the substrate and epitaxial layer and are located in at least one of the regions of isolated monocrystalline silicon. The P base region in the NPN designated regions and a P reach-through in the PNP designated regions are formed simultaneously. The emitter region in the NPN regions and base contact region in the PNP regions are then formed simultaneously. The P emitter region in the PNP regions is then implanted by suitable ion implantation techniques. A Schottky Barrier collector contact in the PNP regions are formed. Electrical contacts are then made to the PNP and NPN transistor elements. A PNP device may be fabricated without the formation of an NPN device if it is so desired.

12 Claims, 14 Drawing Figures



United States Patent [19]

Joshi et al.

[11] **4,216,573**

[45] **Aug. 12, 1980**

[54] **THREE MASK PROCESS FOR MAKING FIELD EFFECT TRANSISTORS**

[75] Inventors: **Madhukar L. Joshi**, Essex Junction; **Richard K. Mason**, Colchester; **Wilbur D. Pricer**, Burlington, all of Vt.

[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[21] Appl. No.: **904,182**

[22] Filed: **May 8, 1978**

[51] **Int. Cl.**[2] **B01J 17/00**

[52] **U.S. Cl.** ..... **29/571**; 29/577 R; 29/578; 29/589; 357/41

[58] **Field of Search** 29/571, 577, 578; 357/41, 45

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,533,158 10/1970 Bower 29/571

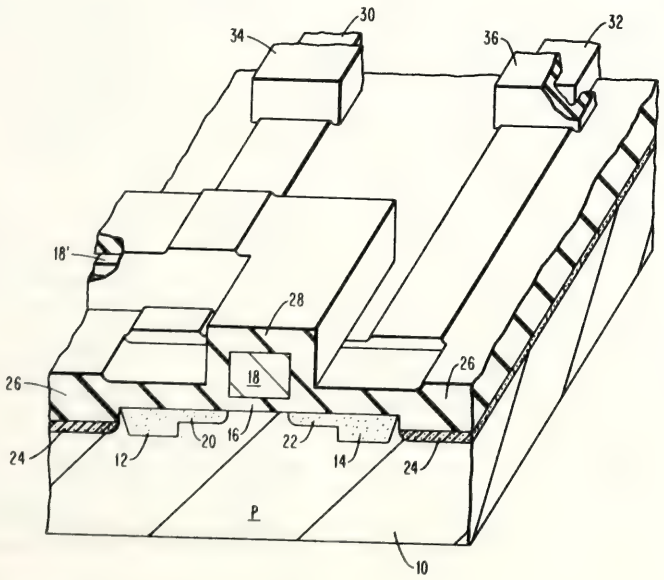
Primary Examiner—W. C. Tupman

Attorney, Agent, or Firm—Stephen J. Limanek

[57] **ABSTRACT**

A three mask method is provided for making a field effect transistor which includes the use of a first mask for defining first and second spaced apart diffusion regions, each having first and second ends, a second mask for defining a contact region at the first end of the first and second diffusion regions and for defining a protected region at the gate region and source and drain electrodes of the transistor, the protected region extending between the second ends of the first and second diffusion regions, and a third mask for forming a gate electrode within the protected region and contact electrodes in the contact region. The source and drain electrodes are formed between the gate electrode and the first and second diffusion regions by ion implantation techniques. The surfaces of the first and second diffusion regions between the contact electrodes and the second end of the first and second diffusions are oxidized to provide a crossover arrangement for gate electrode wiring, when desired, without requiring additional process steps.

11 Claims, 20 Drawing Figures



United States Patent [19]

Esch et al.

[11] **4,219,834**

[45] **Aug. 26, 1980**

[54] **ONE-DEVICE MONOLITHIC RANDOM ACCESS MEMORY AND METHOD OF FABRICATING SAME**

[75] Inventors: **Ronald P. Esch**, San Jose, Calif.; **Robert M. Folsom**, Reston; **Cheng-Yih Liu**, Woodbridge, both of Va.; **Vincent L. Rideout**, Mohegan Lake, N.Y.; **Donald A. Soderman**, Vienna; **G. Thomas Wenning**, Manassas, both of Va.

[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[21] Appl. No.: **850,762**

[22] Filed: **Nov. 11, 1977**

[51] **Int. Cl.**[2] **H01L 27/02**

[52] **U.S. Cl.** **357/41**; 357/46; 357/45; 357/51; 357/53; 357/54; 357/55; 357/59

[58] **Field of Search** 357/41, 45, 46, 51, 357/53, 54, 55, 59

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,811,076 5/1974 Smith 357/41

Primary Examiner—Edward J. Wojciechowicz

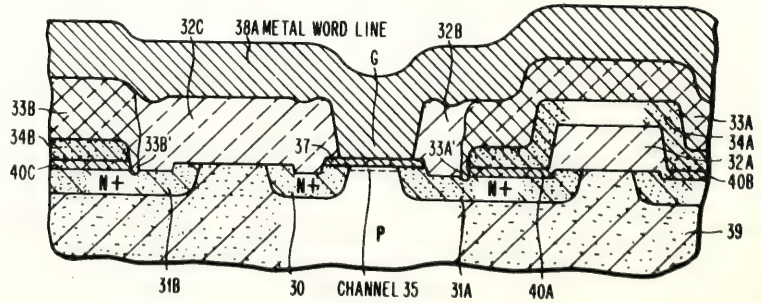
Attorney, Agent, or Firm—Wesley DeBruin

[57] **ABSTRACT**

A dynamic random access memory is fabricated on a monolithic chip of semiconductor material. The memory is formed of an array of memory cells controlled for reading and writing by word and bit lines which are selectively connected to the cells. Each cell is a single field effect transistor structure having improved electrical charge storage capability. The improved charge storage capability of each cell is provided by an electrical capacitance structure uniquely arranged and formed as an integral portion of the field effect transistor structure. The gate electrode of each field effect transistor structure is connected to a predetermined one of said word lines. The drain of each field effect transistor is connected to a predetermined one of said bit lines. The source of each field effect transistor structure is integrally connected to and forms a portion of the uniquely arranged electrical capacitance structure of the field effect transistor structure. The electrical capacitance or storage node structure of each cell has increased electrical charge storage capacity and may be considered as a single capacitor. The single (storage) capacitor of each cell is provided between the source of the field effect transistor, a source of reference potential (reference plane) and the monolithic semiconductor substrate on which the memory is fabricated.

The arrangement of the memory cells, the structure and material of each of the memory cells, and a method of fabricating the entire memory is disclosed. Also disclosed is an improved field effect transistor structure and process for fabricating same. The process of fabrication, cell arrangement and the improved storage node of each memory cell, as structurally fabricated and uniquely arranged, provides a monolithic memory having improved density and operating characteristics.

3 Claims, 28 Drawing Figures



United States Patent [19]
Lever et al.
[11] **4,222,792**
[45] **Sep. 16, 1980**

[54] **PLANAR DEEP OXIDE ISOLATION PROCESS UTILIZING RESIN GLASS AND E-BEAM EXPOSURE**

[75] Inventors: **Reginald F. Lever**, Putnam Valley, N.Y.; **John L. Mauer, IV**, Sherman, Conn.; **Alwin E. Michel**, Ossining, N.Y.; **Laura B. Rothman**, Sherman, Conn.

[73] Assignee: **International Business Machines Corporation**, N.Y.

[21] Appl. No.: **73,593**

[22] Filed: **Sep. 10, 1979**

[51] **Int. Cl.**[2] **H01L 21/26**; H01L 21/316; H01L 21/76

[52] **U.S. Cl.** ..... **148/1.5**; 29/576 W; 29/578; 29/580; 106/287.13; 148/175; 156/643; 156/657; 156/662; 357/49; 357/50; 357/54; 427/93; 427/95; 427/43.1

[58] **Field of Search** ..... 148/1.5, 174, 175; 156/643, 644, 657, 662; 29/576 W, 578, 580; 427/93, 95, 43; 357/49, 50, 54; 106/287.13

[56] **References Cited**

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Roberts, E. D., "Preparation and Properties of Polysiloxane Electron Resist," J. Electrochem. Soc., vol. 120, No. 12, Dec. 1973, pp. 1716–1721.

Primary Examiner—L. Dewayne Rutledge
Assistant Examiner—W. G. Saba
Attorney, Agent, or Firm—Wesley DeBruin

[57] **ABSTRACT**

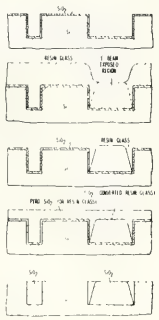
A planar deep oxide isolation process for providing deep wide silicon dioxide filled trenches in the planar surface of a silicon semiconductor substrate, said process comprising the steps:

(a) forming deep wide trenches in the planar surface of the silicon substrate;
(b) forming a thin layer of silicon dioxide on the planar surface of the silicon substrate and the exposed silicon surfaces of said deep wide trenches;
(c) applying resin glass (polysiloxane) to the planar surface of said semiconductor substrate and within said deep wide trenches;
(d) spinning off at least a portion of the resin glass on the planar surface of the substrate;
(e) baking the substrate at a low temperature;
(f) exposing the resin glass contained within the deep wide trenches of substrate to the energy of an E-beam;
(g) developing the resin glass contained on said substrate in a solvent;
(h) heating said substrate in oxygen to convert said resin glass contained within said deep wide trenches to silicon dioxide;
(i) depositing a layer of silicon dioxide to provide a planar silicon dioxide surface on the exposed the surface of said substrate; and
(j) planarize exposed silicon dioxide surface to silicon of substrate.

A planar deep oxide isolation process for providing deep wide silicon dioxide filled trenches in the planar surface of a silicon semiconductor substrate as recited in the preceding paragraph, wherein the following steps are performed in lieu of step i of claim 1, said steps comprising:

(i-1) apply a second thin layer of resin glass; and
(i-2) convert said resin glass to silicon dioxide.

7 Claims, 5 Drawing Figures



United States Patent [19]
Jambotkar
[11] **4,223,329**
[45] **Sep. 16, 1980**

[54] **BIPOLAR DUAL-CHANNEL CHARGE-COUPLED DEVICE**

[75] Inventor: **Chakrapani G. Jambotkar**, Hopewell Junction, N.Y.

[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[21] Appl. No.: **920,935**

[22] Filed: **Jun. 30, 1978**

[51] **Int. Cl.**[3] **H01L 29/78**; G11C 19/28; H01L 27/04

[52] **U.S. Cl.** ..... **357/24**; 357/50; 307/221 D

[58] **Field of Search** ..... 357/24; 307/221 D

[56] **References Cited**

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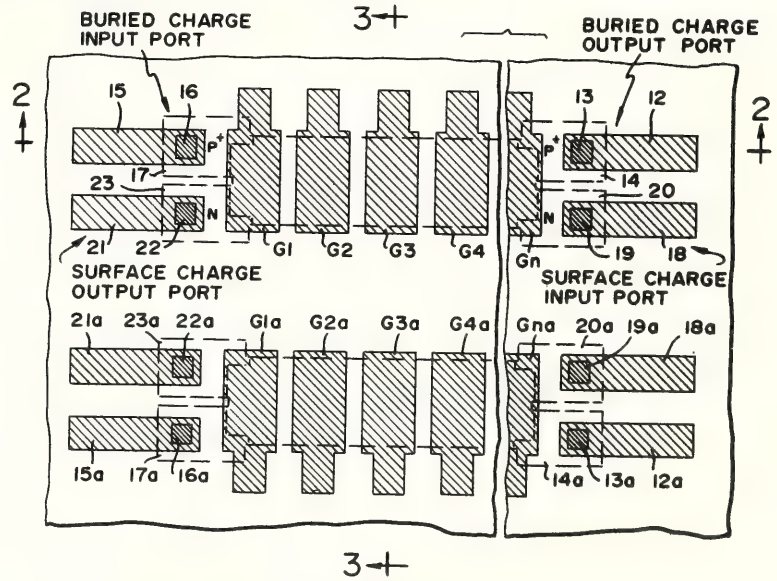
535604	11/1976	U.S.S.R.	357/24

Primary Examiner—Gene M. Munson
Attorney, Agent, or Firm—Robert J. Haase

[57] **ABSTRACT**

A bipolar dual-channel charge-coupled device having a first channel at the surface for storing a first bit stream of minority charge carrier packets and a second channel buried in the bulk for storing a second bit stream of majority charge carrier packets. The two bit streams are transferred along their respective surface and buried channels simultaneously and independently of each other, thereby substantially increasing the bit storage density of the chip.

7 Claims, 4 Drawing Figures



United States Patent [19]

Anantha et al.

[11] **4,228,450**

[45] **Oct. 14, 1980**

[54] **BURIED HIGH SHEET RESISTANCE STRUCTURE FOR HIGH DENSITY INTEGRATED CIRCUITS WITH REACH THROUGH CONTACTS**

[75] Inventors: **Narasipur G. Anantha**, Hopewell Junction; **Augustine W. Chang**, Wappingers Falls, both of N.Y.

[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[21] Appl. No.: **844,768**

[22] Filed: **Oct. 25, 1977**

[51] **Int. Cl.**[2] **H01L 27/02**

[52] **U.S. Cl.** **357/51**; 357/34; 357/49

[58] **Field of Search** 357/34, 49, 51

[56] **References Cited**

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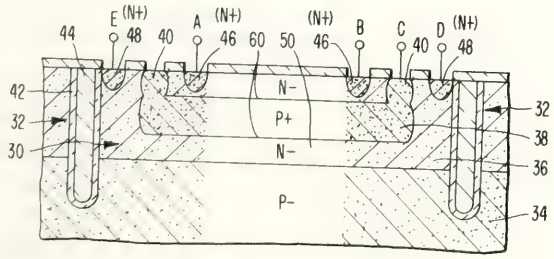
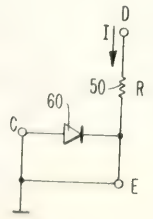
Primary Examiner—Joseph E. Clawson, Jr.
Attorney, Agent, or Firm—George O. Saile

[57] **ABSTRACT**

A high sheet resistance structure for high density integrated circuits and the method for manufacturing such structure is given. The structure includes a silicon region separated from other silicon regions by a dielectric barrier surrounding the region. A resistor of a first conductivity, for example, N type, encompasses substantially the surface of the silicon region. Electrical contacts are made to the resistor. A region highly doped of a second conductivity, for example, P-type, is located below a portion of the resistor region. This region of second conductivity is connected to the surface. Electrical contacts are made to this varied region for biasing purposes. A second region within the same isolated silicon region may be used as a resistor. This region is located below the buried region of second conductivity. Alternatively, the described resistor regions can be connected as transistors. This allows the formation of a standard masterslice which can be personalized at a late stage in the manufacturing to either resistors or transistors in all or a portion of the standard regions.

12 Claims, 10 Drawing Figures





United States Patent [19]

Bergeron et al.

[11] **4,229,753**

[45] **Oct. 21, 1980**

[54] **VOLTAGE COMPENSATION OF TEMPERATURE COEFFICIENT OF RESISTANCE IN AN INTEGRATED CIRCUIT RESISTOR**

[75] Inventors: **David L. Bergeron**, Manassas; **Geoffrey B. Stephens**, Catlett, both of Va.

[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[21] Appl. No.: **825,759**

[22] Filed: **Aug. 18, 1977**

[51] **Int. Cl.**[2] **H01L 23/56**; H01L 29/66; H01L 27/02

[52] **U.S. Cl.** **357/28**; 357/51; 357/91; 338/7; 307/310

[58] **Field of Search** 357/28, 29, 51, 23, 357/91; 307/310; 338/7

[56] **References Cited**

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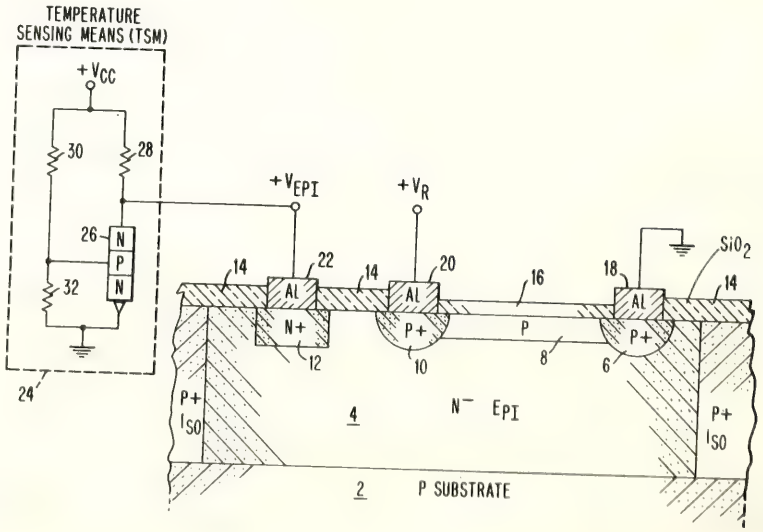
IBM Technical Disclosure Bulletin, vol. 19, No. 5, Oct. 1976, Controlling the Temperature Coefficient of Resistance of Ion Implanted Resistors, pp. 1675–1676.

Primary Examiner—Andrew J. James
Attorney, Agent, or Firm—Maurice H. Klitzman

[57] **ABSTRACT**

A circuit technique is disclosed for compensating for changes in the resistance of an integrated circuit resistor in an epitaxial bed, which is exposed to temperature changes. The resistance of an integrated circuit resistor is a function of the temperature at which is operates. The invention is based on the recognition that the resistance of the resistor is also a function of the potential difference between the body of the resistor and the epitaxial bed itself. Temperature compensation is achieved by connecting a temperature sensing circuit to the epitaxial bed, which has a voltage output which varies inversely with respect to the temperature coefficient of resistance of the resistor. Thus, the net change in the resistance of the resistor as it undergoes a temperature change, approximates zero.

4 Claims, 4 Drawing Figures



United States Patent [19]

Heller

[11] **4,230,954**

[45] **Oct. 28, 1980**

[54] **PERMANENT OR SEMIPERMANENT CHARGE TRANSFER STORAGE SYSTEMS**

[75] Inventor: **Lawrence G. Heller,** Essex Junction, Vt.

[73] Assignee: **International Business Machines Corporation,** Armonk, N.Y.

[21] Appl. No.: **974,409**

[22] Filed: **Dec. 29, 1978**

[51] **Int. Cl.**[3] **H03K 5/00;** H01L 29/78; G11C 11/34; H01L 29/34

[52] **U.S. Cl.** **307/238;** 357/23; 357/24; 357/45; 357/54; 357/89; 365/183

[58] **Field of Search** 357/23, 24, 41, 45; 365/149, 183; 307/238

[56] **References Cited**

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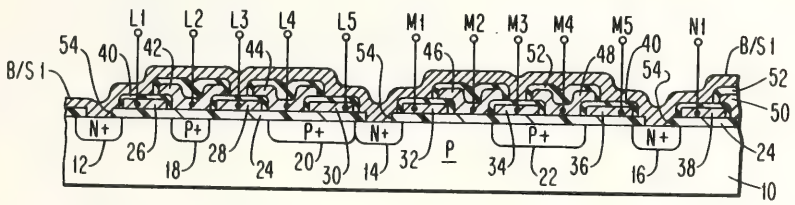
Primary Examiner—Gene M. Munson
Attorney, Agent, or Firm—Stephen J. Limanek

[57] **ABSTRACT**

Storage systems are provided with memory cells made of devices having different voltage thresholds for storing information permanently or semipermanently. The devices are arranged adjacent to each other and communicating with a diffusion region in a semiconductor substrate. Information is sensed by detecting the charge transferred from a selected cell to the diffusion region. In an embodiment of the invention, a P-type substrate has an N+ diffusion region formed therein with a plurality of adjacent and parallelly arranged word lines insulated from the substrate and disposed adjacent to the N+ diffusion region. A P+ region, preferably implanted into the substrate, is disposed under selected segments of the word lines to provide devices having a first or high threshold voltage magnitude. The remaining devices which are not associated with a P-30 region have a second or low threshold voltage magnitude. By applying a voltage of the same magnitude to each of the word lines, potential wells are formed which are filled by charge or carriers from the diffusion region. Since the potential wells associated with the high threshold devices hold less charge than do the low threshold devices, a charge or voltage sensing circuit connected to the N+ diffusion region is used to detect the amount of charge flowing between the wells and the diffusion region to thus identify the high and low threshold devices when the voltage on the selected word line is decreased. By eliminating the P+ regions and storing charge, e.g., electrons, at selected locations under the word lines in dual insulating layers, the cells may be electrically programmable.

18 Claims, 7 Drawing Figures



United States Patent [19]

Goel

[11] **4,183,041**

[45] **Jan. 8, 1980**

[54] **SELF BIASING OF A FIELD EFFECT TRANSISTOR MOUNTED IN A FLIP-CHIP CARRIER**

[75] Inventor: **Jitendra Goel,** Kendall Park, N.J.

[73] Assignee: **RCA Corporation,** New York, N.Y.

[21] Appl. No.: **919,069**

[22] Filed: **Jun. 26, 1978**

[51] **Int. Cl.**[2] **H01L 29/80;** H01L 27/02; H01L 23/02

[52] **U.S. Cl.** **357/81;** 357/80; 357/22; 357/51; 357/74; 333/247

[58] **Field of Search** 357/22, 71, 80, 81, 357/69, 74, 51; 333/246, 247

[56] **References Cited**

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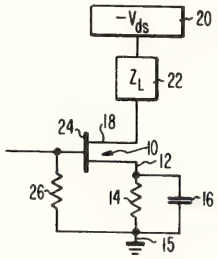
3,825,805	7/1974	Belohoubeck et al.	357/81
3,877,063	4/1975	Abraham et al.	357/69
4,135,168	1/1979	Wade	357/71

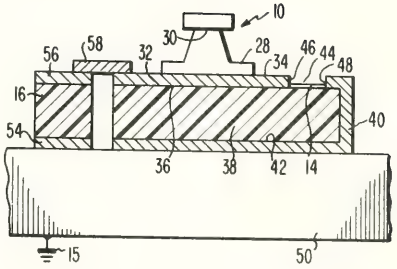
Primary Examiner—Andrew J. James
Attorney, Agent, or Firm—H. Christoffersen; Samuel Cohen; Joseph D. Lazar

[57] **ABSTRACT**

A field effect transistor is mounted in a flip-chip carrier which is in contact with one surface of a metal plate, the other surface of the plate being in contact with one surface of a block of beryllium oxide. A metal sheet, connected to a ground plane, is in contact with the one surface of the block and the surface of the block opposed therefrom. The plate and the sheet have a space therebetween. A film resistor is disposed upon the block in the space.

3 Claims, 3 Drawing Figures





United States Patent [19]

Stewart

[11] **4,185,319**

[45] **Jan. 22, 1980**

[54] NON-VOLATILE MEMORY DEVICE

[75] Inventor: **Roger G. Stewart**, Neshanic Station, N.J.

[73] Assignee: **RCA Corp.**, New York, N.Y.

[21] Appl. No.: **948,507**

[22] Filed: **Oct. 4, 1978**

[51] **Int. Cl.**[2] **G11C 11/40**

[52] **U.S. Cl.** **365/185**; 307/238; 357/53; 365/51

[58] **Field of Search** 307/238, 279, 51; 365/182, 183, 184, 185, 52; 357/53, 68, 86, 89

[56] **References Cited**

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A Distributed Gate Bistable MOS Transistor", Fu et al. *Solid State Electronics* 1971 vol. 14 pp. 799–804.

"Famos-A New Semiconductor Charge Storage Device" Frohman-Bentchkowsky, *Solid State Electronics* 1974 vol. 17 pp. 517–529.

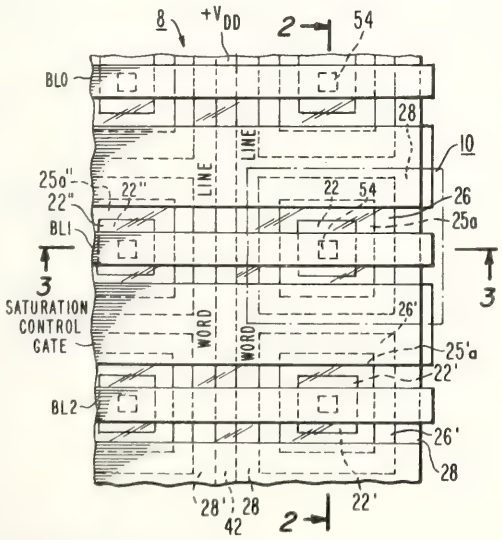
Primary Examiner—Terrell W. Fears

Attorney, Agent, or Firm—H. Christoffersen; H. I. Schanzer; L. P. Benjamin

[57] **ABSTRACT**

A field-effect device with closed floating gate geometry suitable for use as a storage element in a non-volatile memory array.

12 Claims, 5 Drawing Figures



United States Patent [19]

Schade, Jr.

[11] **4,199,733**

[45] **Apr. 22, 1980**

[54] **EXTENDED-DRAIN MOS MIRRORS**

[75] Inventor: **Otto H. Schade, Jr.**, N. Caldwell, N.J.

[73] Assignee: **RCA Corporation**, New York, N.Y.

[21] Appl. No.: **945,601**

[22] Filed: **Sep. 25, 1978**

[30] **Foreign Application Priority Data**

Jan. 19, 1978 [GB] United Kingdom 659/78

Sep. 14, 1978 [GB] United Kingdom 36789/78

[51] **Int. Cl.**[2] **H03F 3/16**

[52] **U.S. Cl.** **330/277**; 330/288; 330/307; 357/23; 357/41

[58] **Field of Search** 330/277, 288, 300, 307; 357/41, 23

[56] **References Cited**

U.S. PATENT DOCUMENTS

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3,953,807	4/1976	Schade, Jr.	330/277
4,015,146	3/1977	Aihara	307/304
4,064,506	12/1977	Cartwright, Jr.	307/304 X

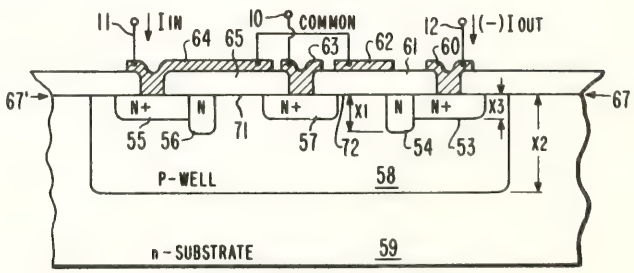
Primary Examiner—James B. Mullins

Attorney, Agent, or Firm—Paul J. Rasmussen; Allen LeRoy Limberg; Eric P. Herrmann

[57] **ABSTRACT**

An improved current amplifier, of the type having input, output and common terminals and which is subject to having widely dissimilar voltages at its input and output terminals has field-effect master and slave transistors formed in a region of semiconductor substrate having an impurity concentration gradient such that the material resistivity increases in a direction into the substrate and provided with relatively deep drain extensions.

6 Claims, 4 Drawing Figures



United States Patent [19]
Goodman et al.
[11] **4,199,773**
[45] **Apr. 22, 1980**

[54] **INSULATED GATE FIELD EFFECT SILICON-ON-SAPPHIRE TRANSISTOR AND METHOD OF MAKING SAME**

[75] Inventors: **Alvin M. Goodman**, Princeton, N.J.; **Charles E. Weitzel**, Scottsdale, Ariz.

[73] Assignee: **RCA Corporation**, New York, N.Y.

[21] Appl. No.: **938,266**

[22] Filed: **Aug. 29, 1978**

[51] **Int. Cl.**[2] **H01L 29/72**
[52] **U.S. Cl.** **357/23**; 357/4; 357/42; 357/49; 357/89; 357/91
[58] **Field of Search** 357/23, 4, 42, 49, 89, 357/91

[56] **References Cited**

U.S. PATENT DOCUMENTS

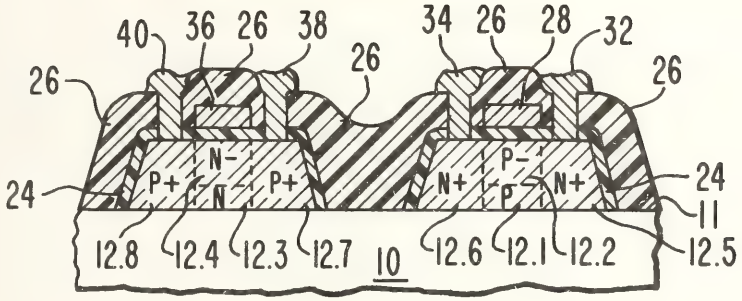
4,106,045 8/1978 Nishi 357/23
4,143,266 3/1979 Borel et al. 357/23

Primary Examiner—Edward J. Wojciechowicz
Attorney, Agent, or Firm—H. Christoffersen; D. S. Cohen; L. P. Benjamin

[57] **ABSTRACT**

A silicon-on-sapphire structure and method for forming the same is described wherein the leakage current attributable to "back channel" leakage is minimized by forming the channel region in such a manner as to have provided therein at least two levels of dopant concentration. The heavier level of dopant concentration is positioned adjacent the silicon/sapphire interface while the lighter level of dopant concentration occupies the remainder of the channel region and is shallower than the heavier level. The classic inversion process takes place in the lightly doped section at the shallow level.

10 Claims, 4 Drawing Figures



United States Patent [19]
Ahmed
[11] **4,199,776**
[45] **Apr. 22, 1980**

[54] **INTEGRATED INJECTION LOGIC WITH FLOATING REINJECTORS**

[75] Inventor: **Adel A. A. Ahmed**, Annandale, N.J.

[73] Assignee: **RCA Corporation**, New York, N.Y.

[21] Appl. No.: **936,409**

[22] Filed: **Aug. 24, 1978**

[51] **Int. Cl.**[2] **H01L 27/04**; H03K 19/08
[52] **U.S. Cl.** **357/46**; 357/44; 357/92; 357/20
[58] **Field of Search** 357/46, 92, 44

[56] **References Cited**

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4,153,909 5/1979 Dobkin 357/92
4,158,783 6/1979 Berger et al. 357/92

FOREIGN PATENT DOCUMENTS

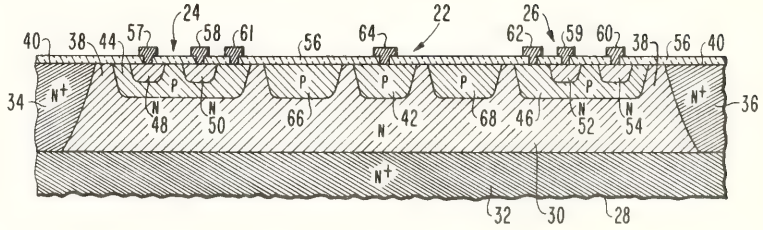
7511516 4/1976 Netherlands 357/92

Primary Examiner—William D. Larkins
Attorney, Agent, or Firm—H. Christoffersen; D. S. Cohen; T. H. Magee

[57] **ABSTRACT**

An integrated injection logic (I^2L) device includes at least two gate structures. Each gate structure includes a first region of one type conductivity with an injector region and a base region of the opposite type conductivity disposed therein adjacent a surface thereof. A second region of the opposite type conductivity is disposed in each gate structure adjacent the surface of the first region between the injector and base region. The second regions are electrically-floating regions free of any contact electrode.

4 Claims, 4 Drawing Figures



United States Patent [19]

Beelitz et al.

[11] **4,199,860**

[45] **Apr. 29, 1980**

[54] **METHOD OF INTEGRATING SEMICONDUCTOR COMPONENTS**

[75] Inventors: **Howard R. Beelitz**, Gillett, Pa.; **Donald R. Preslar**, Somerville, N.J.

[73] Assignee: **RCA Corporation**, New York, N.Y.

[21] Appl. No.: **850,672**

[22] Filed: **Nov. 11, 1977**

[51] **Int. Cl.**[2] **B01J 17/00**

[52] **U.S. Cl.** ..... **29/577 C**; 29/580; 357/15

[58] **Field of Search** ..... 29/576 W, 577, 580; 357/15, 56

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,623,925	11/1971	Jenkins	357/48
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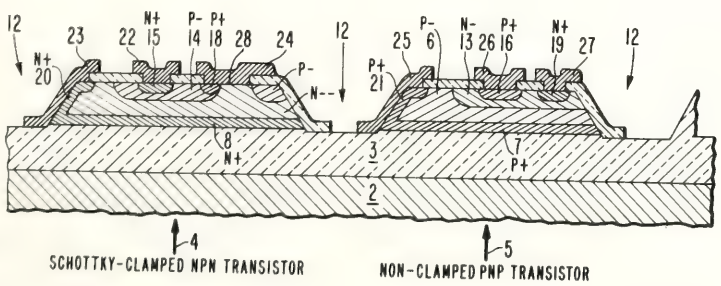
4,063,271	12/1977	Bean	357/56

Primary Examiner—W. C. Tupman
Attorney, Agent, or Firm—Edward J. Norton

[57] **ABSTRACT**

A dielectric-isolated PNP transistor with Schottky protection, either alone or as one of an integrated pair of complementary bipolar transistors has complete dielectric isolation from neighboring devices and from the substrate by means of a topside anisotropic etch. This leaves the devices in mesa form, thinner versions having the facility of lateral terminations, e.g. for the collector. The method is advantageously adapted to provide single type or complementary bipolars with integrated Schottky barrier protection.

9 Claims, 4 Drawing Figures



United States Patent [19]

Ipri

[11] **4,200,878**

[45] **Apr. 29, 1980**

[54] **METHOD OF FABRICATING A NARROW BASE-WIDTH BIPOLAR DEVICE AND THE PRODUCT THEREOF**

[75] Inventor: **Alfred C. Ipri**, Princeton, N.J.

[73] Assignee: **RCA Corporation**, New York, N.Y.

[21] Appl. No.: **914,901**

[22] Filed: **Jun. 12, 1978**

[51] **Int. Cl.**[2] **H01L 21/223**; H01L 21/26; H01L 29/72

[52] **U.S. Cl.** **357/35**; 29/571; 29/578; 148/1.5; 148/187; 357/44; 357/46

[58] **Field of Search** 148/1.5, 187; 357/44, 357/46, 35; 29/578, 571

[56] **References Cited**

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4,124,933	11/1978	Nicholas	29/578

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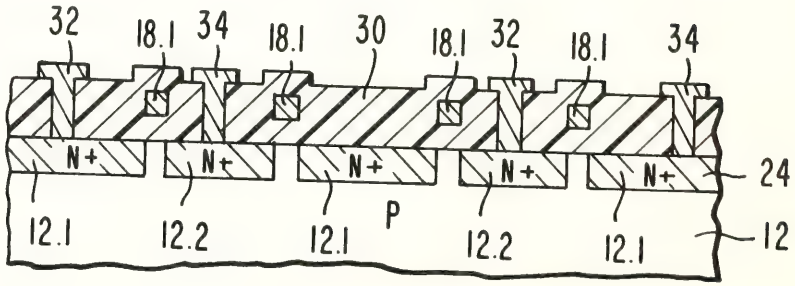
Electronics, Oct. 3, 1974, pp. 111–118.
Solid State Technology, Jun., 1977, pp. 42–48.

Primary Examiner—G. Ozaki
Attorney, Agent, or Firm—H. Christoffersen; D. S. Cohen; L. P. Benjamin

[57] **ABSTRACT**

The basewidth of a lateral, bipolar transistor is markedly reduced by first forming a layer of polycrystalline silicon over an oxide coated substrate. By utilizing a process for doping the exposed edges of the patterned polysilicon layer, a narrower basewidth dimension is achieved than heretofore possible with photolithographic techniques.

2 Claims, 11 Drawing Figures



United States Patent [19]
Scott, Jr. et al.
[11] **4,201,603**
[45] **May 6, 1980**

[54] **METHOD OF FABRICATING IMPROVED SHORT CHANNEL MOS DEVICES UTILIZING SELECTIVE ETCHING AND COUNTERDOPING OF POLYCRYSTALLINE SILICON**

[75] Inventors: **Joseph H. Scott, Jr.**, Plainsboro; **Alfred C. Ipri**, Princeton, both of N.J.

[73] Assignee: **RCA Corporation**, New York, N.Y.

[21] Appl. No.: **966,510**

[22] Filed: **Dec. 4, 1978**

[51] **Int. Cl.**[2] **H01L 21/225**; H01L 21/308

[52] **U.S. Cl.** **148/174**; 29/571; 29/578; 29/580; 148/1.5; 148/175; 148/187; 148/190; 156/628; 156/657; 357/4; 357/23; 357/49; 357/59; 357/91; 427/85

[58] **Field of Search** 148/174, 175, 187, 190, 148/1.5; 156/628, 644, 648, 657; 29/571, 578, 580; 427/85; 357/4, 23, 49, 59, 91

[56] **References Cited**

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4,124,933	11/1978	Nicholas	29/578

FOREIGN PATENT DOCUMENTS

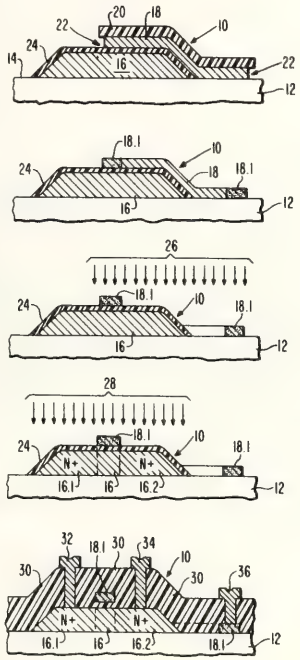
1477512 6/1977 United Kingdom .

Primary Examiner—L. Dewayne Rutledge
Assistant Examiner—W. G. Saba
Attorney, Agent, or Firm—Birgit E. Morris; D. S. Cohen; Lawrence P. Benjamin

[57] **ABSTRACT**

A method for fabricating a short channel MOS device is described wherein the conductivity of the gate member is increased by a factor of about 2.5 by counterdoping a P-type doped polycrystalline line with an N-type dopant.

8 Claims, 5 Drawing Figures



United States Patent [19]
Reichert et al.
[11] **4,202,001**
[45] **May 6, 1980**

[54] **SEMICONDUCTOR DEVICE HAVING GRID FOR PLATING CONTACTS**

[75] Inventors: **Walter F. Reichert**, East Brunswick; **Ho-Chung Huang**, Princeton Junction, both of N.J.

[73] Assignee: **RCA Corporation**, New York, N.Y.

[21] Appl. No.: **903,121**

[22] Filed: **May 5, 1978**

[51] **Int. Cl.**[2] **H01L 29/80**; H01L 27/10; H01L 29/66

[52] **U.S. Cl.** **357/22**; 357/42; 357/55; 357/68

[58] **Field of Search** 357/22, 23, 42, 55, 357/71, 68

[56] **References Cited**

U.S. PATENT DOCUMENTS

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4,069,493	1/1978	Bobenrieth	357/22
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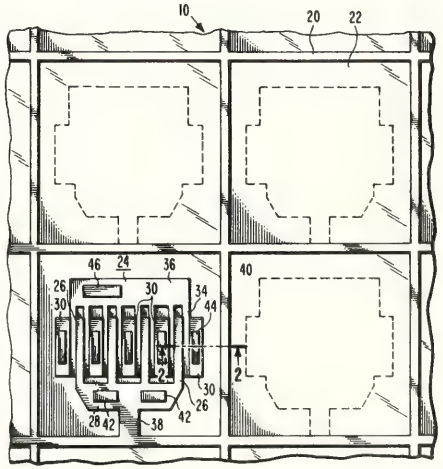
4,104,672	8/1978	Dilorenzo et al.	357/22

Primary Examiner—Andrew J. James
Attorney, Agent, or Firm—H. Christoffersen; D. S. Cohen

[57] **ABSTRACT**

A semiconductor device includes a body of semiconductor material on which are formed a plurality of spaced semiconductor elements. Each of the semiconductor elements includes a plurality of contacts, some of which are separated from each other by recesses in the semiconductor body. A metal grid is on the semiconductor body and surrounds each of the semiconductor elements. At least one of the contacts of each element extends to and is connected to the grid. The grid serves to electrically connect the contacts of all the semiconductor elements to permit the electrical plating of the contacts. Those contacts of each semiconductor element which are not directly connected to the grid are electrically connected thereto through the semiconductor body and an adjacent contact which is directly connected to the grid.

13 Claims, 5 Drawing Figures



United States Patent [19]

Khajezadeh

[11] **4,202,006**

[45] **May 6, 1980**

[54] **SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE**

[75] Inventor: **Heshmat Khajezadeh**, Somerville, N.J.

[73] Assignee: **RCA Corporation**, New York, N.Y.

[21] Appl. No.: **41,086**

[22] Filed: **May 21, 1979**

Related U.S. Application Data

[62] Division of Ser. No. 877,856, Feb. 15, 1978.

[51] **Int. Cl.**[2] **H01L 27/04**

[52] **U.S. Cl.** **357/63**; 357/48; 357/89; 357/90; 357/92

[58] **Field of Search** 357/63, 92, 44, 46, 357/89, 90

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,759,760	9/1973	Encinas	357/35
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3,961,340	6/1976	Encinas	357/34
4,087,900	5/1978	Yiannonlos	357/92

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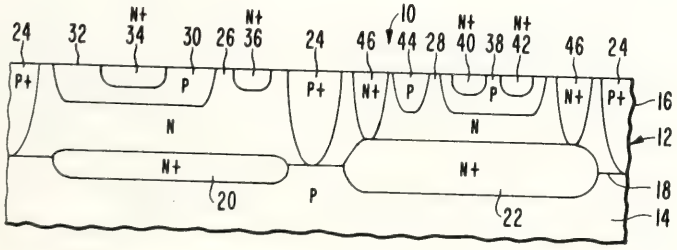
Primary Examiner—William D. Larkins
Attorney, Agent, or Firm—H. Christoffersen; D. S. Cohen; T. H. Magee

[57] **ABSTRACT**

A semiconductor integrated circuit device includes circuit elements having relatively different performance characteristics in which buried regions having different chemical elements are used to autodope an epitaxial layer to different degrees.

4 Claims, 4 Drawing Figures



United States Patent [19]

Schade, Jr.

[11] **4,211,941**

[45] **Jul. 8, 1980**

[54] **INTEGRATED CIRCUITRY INCLUDING LOW-LEAKAGE CAPACITANCE**

[75] Inventor: **Otto H. Schade, Jr.**, North Caldwell, N.J.

[73] Assignee: **RCA Corporation**, New York, N.Y.

[21] Appl. No.: **930,791**

[22] Filed: **Aug. 3, 1978**

[51] **Int. Cl.**[2] **H01L 27/04**; H01L 29/94

[52] **U.S. Cl.** **307/303**; 357/14; 357/23; 357/48; 357/51

[58] **Field of Search** ..... 357/14, 23, 48, 51; 307/303, 296 R

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,654,498	4/1972	Chapron	357/14
3,879,640	4/1975	Schade, Jr.	357/48
4,034,395	7/1977	Abdelrahman	357/51
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4,161,742	7/1979	Kane	357/51
4,164,668	8/1979	Delaporte et al.	357/51

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"Op-Amp IC's", EEE, Nov. 1969, pp. 16, 19-24.

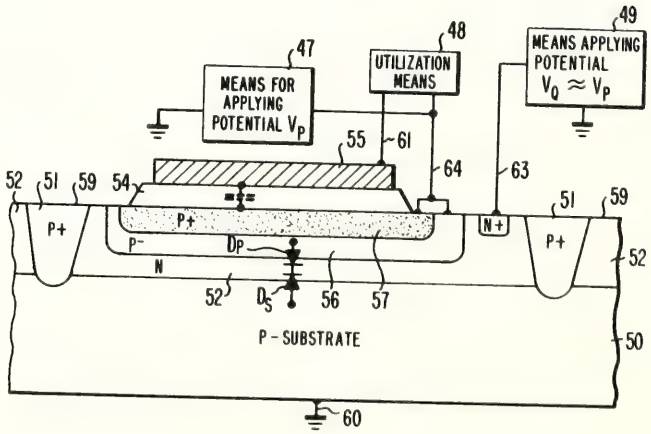
Keonjian, Microelectronics, (McGraw-Hill, N.Y., 1963), pp. 317-319.

Primary Examiner—William D. Larkins
Attorney, Agent, or Firm—Paul J. Rasmussen; Allen LeRoy Limberg; Eric P. Herrmann

[57] **ABSTRACT**

An integrated-circuit MOS capacitor has a first doped semiconductive region forming one of its plates. This first semiconductor region is electrically isolated from the semiconductor substrate by a second doped semiconductor region, which is of opposite conductivity type to and intervenes between the substrate and the first semiconductive region. The present invention resides in the combination of such an MOS capacitor and a circuit for maintaining the potential in the second semiconductor region of the MOS capacitor structure substantially the same as that appearing on the first semiconductor region for minimizing leakage current flow between them. This circuit also provides the leakage current flowing between the second semiconductor region and the substrate, so the leakage current need not flow from the first semiconductor region.

3 Claims, 4 Drawing Figures



United States Patent [19]
Ipri
[11] **4,217,688**
[45] **Aug. 19, 1980**

[54] **FABRICATION OF AN INTEGRATED INJECTION LOGIC DEVICE INCORPORATING AN MOS/BIPOLAR CURRENT INJECTOR**

[75] Inventor: **Alfred C. Ipri**, Princeton, N.J.

[73] Assignee: **RCA Corporation**, New York, N.Y.

[21] Appl. No.: **969,486**

[22] Filed: **Dec. 14, 1978**

Related U.S. Application Data

[62] Division of Ser. No. 914,870, Jun. 12, 1978, abandoned.

[51] **Int. Cl.**[3] **B01J 17/00**
[52] **U.S. Cl.** **29/571**; 29/577R; 29/578; 357/43; 357/46
[58] **Field of Search** 29/571, 577, 578; 357/46, 43

[56] **References Cited**

U.S. PATENT DOCUMENTS

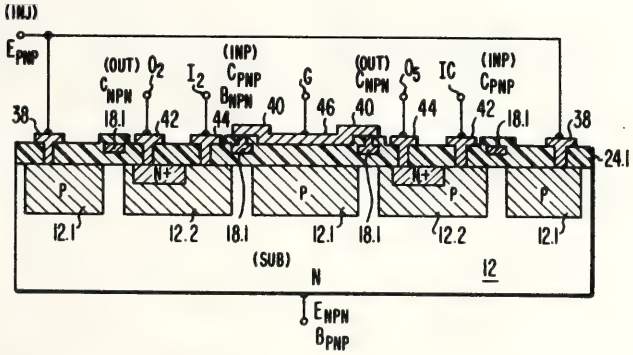
3,608,189	9/1971	Gray	29/571
3,622,812	11/1971	Crawford	357/43
4,063,273	12/1977	Mueller	357/46
4,124,933	11/1978	Nicholas	29/578

Primary Examiner—W. C. Tupman
Attorney, Agent, or Firm—Birgit E. Morris; D. S. Cohen; Lawrence P. Benjamin

[57] **ABSTRACT**

A novel semiconductor configuration is presented utilizing a narrow, gate-like (base) structure formed of, for example, a floating polycrystalline silicon line, that is capable of modulating both the number and type of carriers (electrons or holes) flowing thereunder, between a pair of similarly doped, separated regions. One particular structure described is a four terminal I^2L configuration where the inverter transistor can function in either the mode of an MOS device or the mode of a bipolar device.

1 Claim, 12 Drawing Figures



United States Patent [19]
McElroy
[11] **4,198,695**
[45] **Apr. 15, 1980**

[54] **STATIC SEMICONDUCTOR MEMORY CELL USING DATA LINES FOR VOLTAGE SUPPLY**

[75] Inventor: **David J. McElroy**, Houston, Tex.

[73] Assignee: **Texas Instruments Incorporated**, Dallas, Tex.

[21] Appl. No.: **925,892**

[22] Filed: **Jul. 19, 1978**

[51] **Int. Cl.**[2] **G11C 11/40**
[52] **U.S. Cl.** **365/154**; 307/279; 357/41; 357/45
[58] **Field of Search** 365/154, 190, 205; 307/279, 291, 238; 357/41, 45

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,292,008	12/1966	Rapp	365/154
3,530,443	9/1970	Crafts et al.	365/154
3,949,383	4/1976	Askin et al.	365/154

OTHER PUBLICATIONS

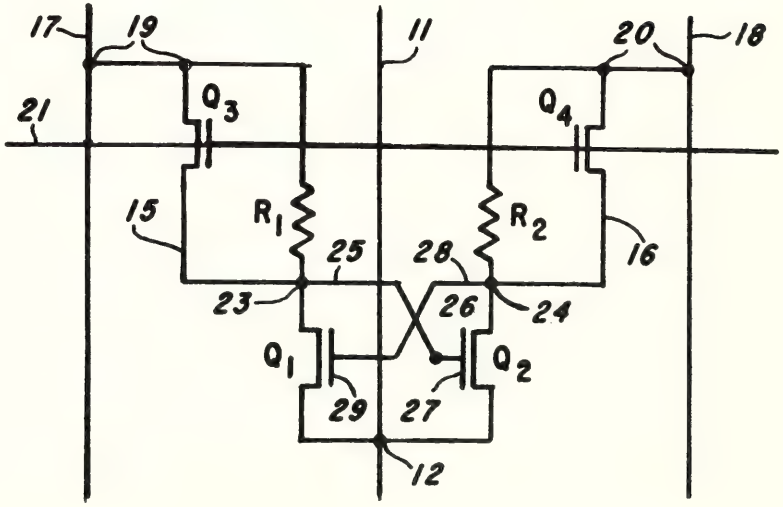
Gaensslen et al., FET Memory Cell, IBM Technical Disclosure Bulletin, vol. 13, No. 7, p. 1751, 12/70.

Primary Examiner—Stuart N. Hecker
Attorney, Agent, or Firm—John G. Graham

[57] **ABSTRACT**

A semiconductor memory circuit includes two cross coupled driver transistors with storage nodes connected to data lines by coupling transistors, providing a static RAM cell. Load resistors are connected from the storage nodes to the data lines rather than to a voltage supply, and the data lines are maintained at an intermediate voltage level in standby operation. The intermediate voltage is sufficient to hold the driver transistors in a stable state, one conducting and one off.

3 Claims, 9 Drawing Figures



United States Patent [19]
Darley et al.
[11] **4,201,997**
[45] **May 6, 1980**

[54] **MESFET SEMICONDUCTOR DEVICE AND METHOD OF MAKING**

[75] Inventors: **Henry M. Darley**, Plano; **Theodore W. Houston**, Richardson, both of Tex.; **James B. Kruger**, Thousand Oaks, Calif.

[73] Assignee: **Texas Instruments Incorporated**, Dallas, Tex.

[21] Appl. No.: **898,582**

[22] Filed: **Apr. 21, 1978**

[51] **Int. Cl.**[2] **H01L 29/48**
[52] **U.S. Cl.** **357/15**; 357/22; 357/41; 357/49; 357/50
[58] **Field of Search** 357/15, 41, 49, 50, 357/23, 22

[56] **References Cited**

U.S. PATENT DOCUMENTS

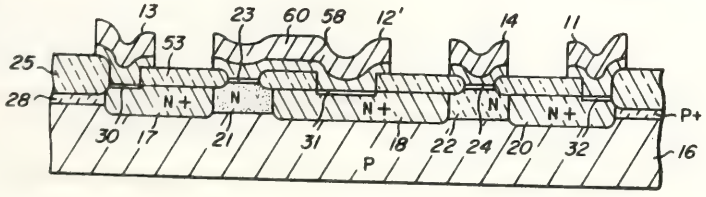
4,104,672 8/1978 DiLorenzo et al. 357/15
4,139,786 2/1979 Raymond et al. 357/41

Primary Examiner—Edward J. Wojciechowicz
Attorney, Agent, or Firm—Ronald A. Williamson; William E. Hiller; Richard L. Donaldson

[57] **ABSTRACT**

An improved MESFET integrated circuit device with a metal-semiconductor diode as the control element and a source and drain as other device elements is fabricated using a self-aligned gate process which consists of an implanted channel stopper underneath a thick field oxide, depletion and enhancement mode device channel implants, implanted source and drain regions, selective oxidation to form self-aligned gates, metal-semiconductor junctions as control elements, barrier metal and a thin film metallization system. The process and device structure are suited for high packing density, very low speed power product and ease of fabrication making it attractive for digital applications.

6 Claims, 18 Drawing Figures



United States Patent [19]
Darley et al.
[11] **4,202,003**
[45] **May 6, 1980**

[54] **MESFET SEMICONDUCTOR DEVICE AND METHOD OF MAKING**

[75] Inventors: **Henry M. Darley**, Plano; **Theodore W. Houston**, Richardson; **Han T. Yuan**, Dallas, all of Tex.

[73] Assignee: **Texas Instruments Incorporated**, Dallas, Tex.

[21] Appl. No.: **898,581**

[22] Filed: **Apr. 21, 1978**

[51] **Int. Cl.**[2] **H01L 29/48**
[52] **U.S. Cl.** **357/15**; 357/41; 357/49; 357/50; 357/22
[58] **Field of Search** 357/15, 41, 49, 50, 357/22

[56] **References Cited**

U.S. PATENT DOCUMENTS

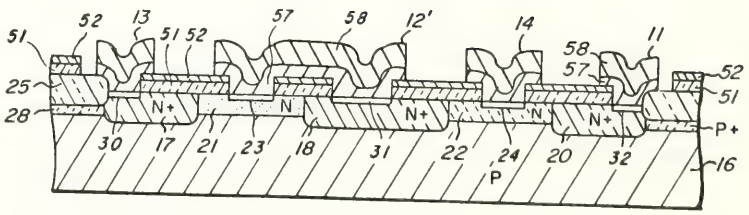
4,104,672 8/1978 DiLorenzo et al. 357/15
4,139,786 2/1979 Raymond et al. 357/41

Primary Examiner—Edward J. Wojciechowicz
Attorney, Agent, or Firm—Ronald A. Williamson; William E. Hiller; Richard L. Donaldson

[57] **ABSTRACT**

A MESFET integrated circuit device with a metal-semiconductor diode as the control element and a source and drain as other device elements is fabricated using a method which consists of an implanted channel stopper underneath a thick field oxide, implanted source and drain regions, depletion and enhancement mode device channel implants, metal-semiconductor junctions as control elements, barrier metal and a thin film metallization system. The process and device structure are suited for high packing density, very low speed power product and ease of fabrication making it attractive for digital applications.

7 Claims, 16 Drawing Figures



United States Patent [19]
Chatterjee et al.

[11] **4,203,125**
[45] **May 13, 1980**

[54] **BURIED STORAGE PUNCH THROUGH DYNAMIC RAM CELL**

[75] Inventors: **Pallab K. Chatterjee; Geoff W. Taylor,** both of Dallas; **Al F. Tasch, Jr.,** Richardson; **Horng-Sen Fu,** Dallas, all of Tex.

[73] Assignee: **Texas Instruments Incorporated,** Dallas, Tex.

[21] Appl. No.: **921,933**

[22] Filed: **Jul. 3, 1978**

[51] **Int. Cl.**[2] **H01L 29/78**
[52] **U.S. Cl.** **357/41;** 357/23; 357/20

[58] **Field of Search** 357/41, 23, 20

[56] **References Cited**

U.S. PATENT DOCUMENTS

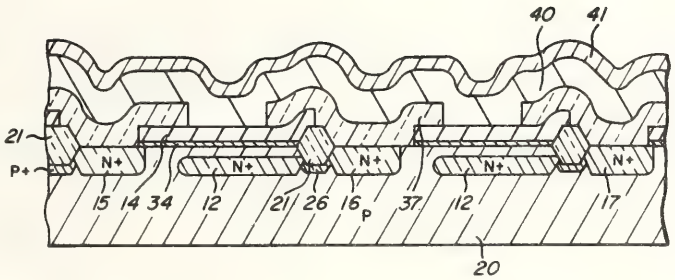
3,748,187	7/1973	Aubuchon	148/1.5
4,065,783	12/1977	Ouyang	357/41

Primary Examiner—Martin H. Edlow
Attorney, Agent, or Firm—Ronald A. Williamson; Richard L. Donaldson; William E. Hiller

[57] **ABSTRACT**

An MOS random access memory cell using the capacitance of a buried P-N junction as the storage element is formed by a process compatable with standard N-channel silicon gate manufacturing methods. The cell is fabricated using a method which consists of an implanted channel stopper underneath a thick field oxide, a buried, fully implanted charge storage element which also is the source of the cell transistor, self-aligned polysilicon gates, multilayer oxide and a thin film of metallization for interconnections. The vertical stacking of the charge storage and transfer elements and the increase in storage area to cell area ratio with the buried storage area provide a cell with very high packing density.

8 Claims, 14 Drawing Figures



United States Patent [19]
Reed

[11] **4,205,227**
[45] **May 27, 1980**

[54] **SINGLE JUNCTION EMITTER ARRAY**

[75] Inventor: **Bruce S. Reed,** Dallas, Tex.

[73] Assignee: **Texas Instruments Incorporated,** Dallas, Tex.

[21] Appl. No.: **871,657**

[22] Filed: **Jan. 23, 1978**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 745,153, Nov. 26, 1976, abandoned.

[51] **Int. Cl.**[2] **H01J 31/50**
[52] **U.S. Cl.** **250/330;** 250/338; 357/30

[58] **Field of Search** 250/370, 332, 334, 338, 250/330; 357/17, 19, 55, 30, 20

[56] **References Cited**

U.S. PATENT DOCUMENTS

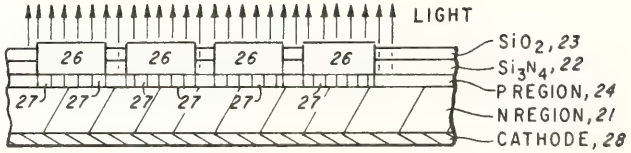
3,293,513	12/1966	Biard et al.	357/17
3,388,255	6/1968	May	357/19
3,636,618	1/1972	Herzog et al.	357/17
3,846,193	11/1974	Jacobus et al.	357/17

Primary Examiner—Alfred E. Smith
Assistant Examiner—Carolyn E. Fields
Attorney, Agent, or Firm—Rene' Grossman; James T. Comfort; Alva H. Bandy

[57] **ABSTRACT**

An apparatus for translating information in one form to electrical signals for driving a single junction emitter light source is disclosed. For example, a device for scanning radiant energy includes a detector array for converting detected invisible electromagnetic energy emanating from a body into electrical signals representative thereof, an electrical signal processing means coupled to the detector array for processing the electrical signals thereof for display, and a single junction emitter array for producing visible light indicative of the invisible electromagnetic energy emanating from the detected body. The single junction emitter array comprises a substrate of light emitting semiconductor material forming a region of n-type conductivity, a region of p-type conductivity formed in the substrate to form with the n-type conductivity region a continuous p-n junction, a plurality of spaced contacts in contact with the p-type conductivity region, and a corresponding plurality of biasing circuits connected to the contacts. The biased contacts coact with the continuous p-n junction to form a plurality of light emitter elements for producing, without scan lines, visible light indicative of the visible electromagnetic energy emanating from the body.

3 Claims, 14 Drawing Figures



United States Patent [19]

Rao

[11] **4,207,585**

[45] **Jun. 10, 1980**

[54] **SILICON GATE MOS ROM**

[75] Inventor: **G. R. Mohan Rao**, Houston, Tex.

[73] Assignee: **Texas Instruments Incorporated**, Dallas, Tex.

[21] Appl. No.: **841,502**

[22] Filed: **Oct. 11, 1977**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 701,932, Jul. 1, 1976, abandoned.

[51] **Int. Cl.**[2] **H01L 27/04**

[52] **U.S. Cl.** **357/41**; 29/571; 29/580; 29/578; 357/23; 357/45; 357/59; 365/104

[58] **Field of Search** 357/23, 41, 45, 91, 357/59; 29/571, 578, 580; 365/104

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,676,921	7/1972	Kooi	357/23
3,711,753	1/1973	Brand et al.	357/59
3,914,855	10/1975	Cheney et al.	357/91

OTHER PUBLICATIONS

Antipov, IBM Tech. Discl. Bull., vol. 17, No. 1, pp. 102-103, Jun. 1974.

Richman, MOS Field Effect Transistors and Integrated Circuits, (Wiley, N.Y., 1973), pp. 200-212.

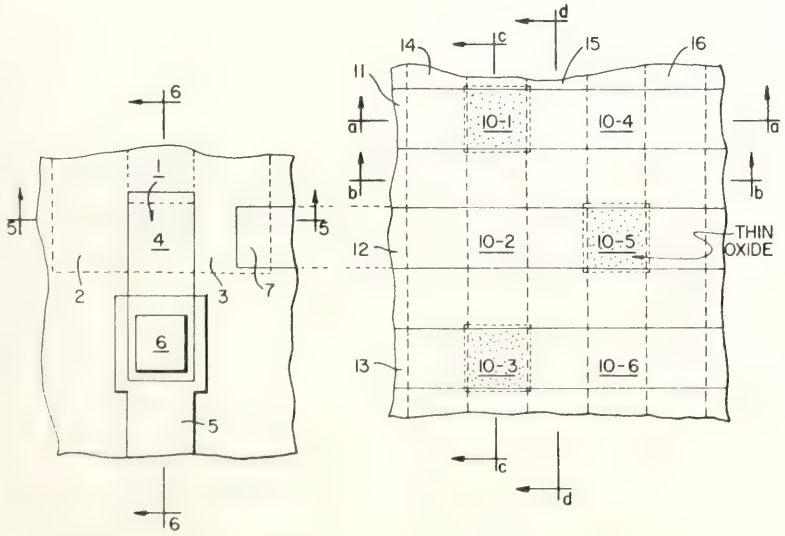
Primary Examiner—William D. Larkins

Attorney, Agent, or Firm—John G. Graham

[57] **ABSTRACT**

An N-channel silicon gate MOS read only memory or ROM formed by a process compatible with standard N-channel manufacturing methods but which allows the elimination of contacts between overlying metal or polysilicon lines and the semiconductor surface. Address lines are polysilicon, and output and ground lines are defined by N+ regions buried beneath field oxide. In the array, for each potential MOS transistor, a logic "1" or "0" is programmed by providing a thin oxide gate region beneath a polysilicon address line for one and providing thick field oxide for the other.

7 Claims, 9 Drawing Figures



United States Patent [19]

Redwine et al.

[11] **4,208,727**

[45] **Jun. 17, 1980**

[54] **SEMICONDUCTOR READ ONLY MEMORY USING MOS DIODES**

[75] Inventors: **Donald J. Redwine; G. R. Mohan Rao**, both of Houston, Tex.

[73] Assignee: **Texas Instruments Incorporated**, Dallas, Tex.

[21] Appl. No.: **915,633**

[22] Filed: **Jun. 15, 1978**

[51] **Int. Cl.**[2] **G11C 17/06**

[52] **U.S. Cl.** **365/105**; 357/41; 357/45; 365/104

[58] **Field of Search** 365/103, 104, 105; 357/41, 45

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,865,651	2/1975	Arita	365/104
3,914,855	10/1975	Cheney et al.	365/104
4,059,826	11/1977	Rogers	365/104

OTHER PUBLICATIONS

Cook et al., Read-Only Memory Fabrication by Laser Formed Connections, IBM Technical Disclosure Bulletin, vol. 15, No. 8, Jan. 1973, pp. 2371-2372.

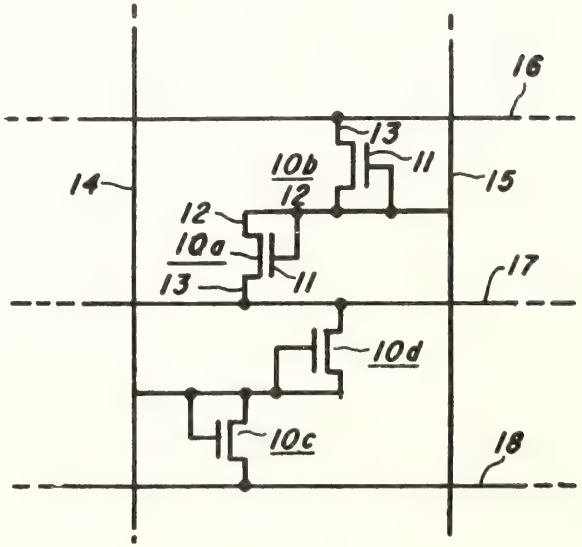
Primary Examiner—Stuart N. Hecker

Attorney, Agent, or Firm—John G. Graham

[57] **ABSTRACT**

A semiconductor integrated circuit functioning as a read only memory or ROM employs MOS diodes as the memory cells and is formed by a process compatible with standard N-channel silicon gate manufacturing methods. Row address lines are metal strips and gates are polysilicon segments, while output or column lines are defined by elongated N+ regions. The gates are shorted to N+ drain regions to provide diode-like cells. Each MOS transistor in the array is programmed to be a logic "1" or "0", such as by ion implanting through the polysilicon gates and thin gate oxide, rendering some cells of such high threshold that they will not turn on. Alternatively, the array may be contact programmable.

4 Claims, 10 Drawing Figures



United States Patent [19]
Rao
[11] **4,213,139**
[45] **Jul. 15, 1980**

[54] **DOUBLE LEVEL POLYSILICON SERIES TRANSISTOR CELL**

[75] Inventor: **G. R. Mohan Rao**, Houston, Tex.

[73] Assignee: **Texas Instruments Incorporated**, Dallas, Tex.

[21] Appl. No.: **907,234**

[22] Filed: **May 18, 1978**

[51] **Int. Cl.**[2] **H01L 27/02**
[52] **U.S. Cl.** **357/41**; 357/23; 357/45; 357/41; 357/59
[58] **Field of Search** 357/23, 41, 45, 46, 357/59

[56] **References Cited**

U.S. PATENT DOCUMENTS

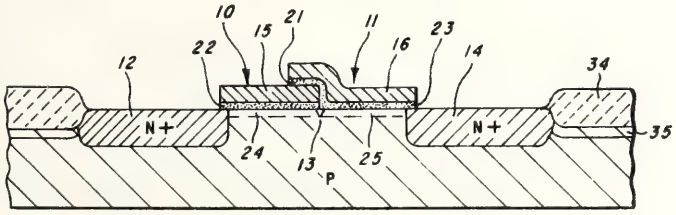
4,084,108	4/1978	Fujimoto	357/59
4,099,196	4/1978	Simko	357/59

Primary Examiner—Edward J. Wojciechowicz
Attorney, Agent, or Firm—John G. Graham

[57] **ABSTRACT**

A pair of MOS transistors are formed as an integrated semiconductor device, sharing a common source/drain region which is created by the edges of inverted regions beneath the gates of the transistors. These gates are first and second level polysilicon, with the second partly overlapping the first. On the opposite ends, the source and drain regions are formed by diffusion using the oxide under the first and second level poly as the diffusion mask.

6 Claims, 7 Drawing Figures



United States Patent [19]
McElroy
[11] **4,213,142**
[45] **Jul. 15, 1980**

[54] **SEMICONDUCTOR DEVICE AND METHOD**

[75] Inventor: **David J. McElroy**, Houston, Tex.

[73] Assignee: **Texas Instruments Incorporated**, Dallas, Tex.

[21] Appl. No.: **32,597**

[22] Filed: **Apr. 23, 1979**

Related U.S. Application Data

[60] Continuation of Ser. No. 797,273, May 16, 1977, which is a division of Ser. No. 573,676, May 1, 1975.

[51] **Int. Cl.**[2] **H01L 29/72**
[52] **U.S. Cl.** **357/91**; 357/23; 357/41; 357/55; 357/88; 357/89; 357/90
[58] **Field of Search** 357/23, 41, 55, 88, 357/89, 90, 91

[56] **References Cited**

U.S. PATENT DOCUMENTS

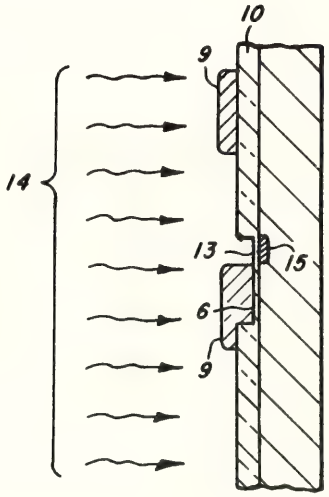
3,936,861	2/1976	Borel et al.	357/91
3,967,365	7/1976	Friedrich	357/91

Primary Examiner—Edward J. Wojciechowicz
Attorney, Agent, or Firm—John G. Graham

[57] **ABSTRACT**

A semiconductive device and a method for producing the semiconductive device, wherein random defects or inaccuracies in precise registrations of certain patterns are compensated by the introduction of selected impurities. The selected impurities bring about changes in the electrical characteristics of those portions of the semiconductor affected by the random defects or registration inaccuracies so as to prevent them from causing malfunctions in the completed devices.

8 Claims, 4 Drawing Figures



United States Patent [19]

McElroy

[11] 4,219,836

[45] Aug. 26, 1980

[54] CONTACT PROGRAMMABLE DOUBLE LEVEL POLYSILICON MOS READ ONLY MEMORY

[75] Inventor: David J. McElroy, Houston, Tex.

[73] Assignee: Texas Instruments Incorporated, Dallas, Tex.

[21] Appl. No.: 907,235

[22] Filed: May 18, 1978

[51] Int. Cl.[2] H01L 29/02

[52] U.S. Cl. 357/55; 357/45; 357/41

[58] Field of Search 357/45, 41, 55

[56] References Cited

U.S. PATENT DOCUMENTS

3,914,855	10/1975	Cheney et al.	357/45
3,985,591	10/1976	Arita	357/45

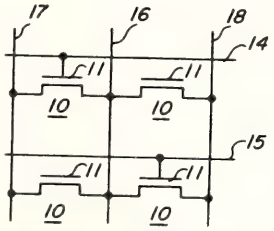
Primary Examiner—Edward J. Wojciechowicz

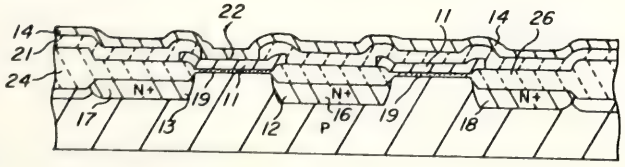
Attorney, Agent, or Firm—John G. Graham

[57] ABSTRACT

A contact programmable, small cell area MOS read only memory or ROM is formed by a process compatible with standard N-channel silicon gate manufacturing methods. Address lines are metal, gates are second level polysilicon, and output and ground lines are defined by elongated N+ regions. Each potential MOS transistor in the array is programmed to be a logic "1" or "0", by presence or absence of a contact engaging the polysilicon gate over the thin gate oxide.

10 Claims, 11 Drawing Figures





United States Patent [19]

Kuo

[11] 4,230,504

[45] Oct. 28, 1980

[54] METHOD OF MAKING IMPLANT PROGRAMMABLE N-CHANNEL ROM

[75] Inventor: Chang-Kiang Kuo, Houston, Tex.

[73] Assignee: Texas Instruments Incorporated, Dallas, Tex.

[21] Appl. No.: 900,549

[22] Filed: Apr. 27, 1978

[51] Int. Cl.[2] G11C 11/40; G11C 17/00

[52] U.S. Cl. 148/1.5; 29/571; 148/187; 357/45; 357/91

[58] Field of Search 365/104; 148/1.5, 187; 357/45, 91; 29/571

[56] References Cited

U.S. PATENT DOCUMENTS

3,852,120	12/1974	Johnson et al.	148/1.5
3,865,651	2/1975	Arita	148/187
3,887,994	6/1975	Ku et al.	29/571
3,914,855	10/1975	Cheney et al.	29/571
4,055,444	10/1977	Rao	48/1.5
4,059,826	11/1977	Rogers	365/104
4,096,522	6/1978	Suzuki et al.	356/45
4,151,020	4/1979	McElroy	148/187
4,151,021	4/1979	McElroy	148/187

Primary Examiner—L. Dewayne Rutledge

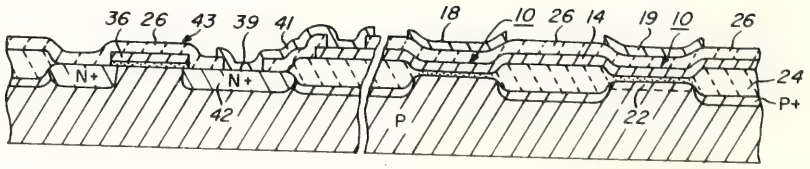
Assistant Examiner—Upendra Roy

Attorney, Agent, or Firm—John G. Graham

[57] ABSTRACT

An MOS read only memory or ROM is formed by a process compatible with standard N-channel silicon gate ROM manufacturing methods. Instead of moat programming or contact programming as is used in almost all standard processes, however, the ROM is programmed by implant after the polysilicon level of gates and interconnection has been deposited and patterned and prior to metal deposition. Address lines and gates are polysilicon, ground lines are defined by elongated N+ regions, and output lines are metal strips contacting the N+ diffused drains. Each potential MOS transistor in the array is programmed to be a logic "1" or "0" by ion implanting through the polysilicon gates and thin gate oxide, using patterned photoresist as a mask prior to application of the polycrystalline silicon.

8 Claims, 10 Drawing Figures



United States Patent [19]
Sawazaki
[11] **4,189,738**
[45] **Feb. 19, 1980**

[54] **SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE**

[75] Inventor: **Hajime Sawazaki**, Tokyo, Japan
[73] Assignee: **Tokyo Shibaura Electric Co., Ltd.**, Japan

[21] Appl. No.: **946,632**
[22] Filed: **Sep. 28, 1978**

Related U.S. Application Data

[63] Continuation of Ser. No. 778,598, Mar. 17, 1977, abandoned.

[30] **Foreign Application Priority Data**

Mar. 18, 1976 [JP] Japan 51-29662

[51] **Int. Cl.**[2] **H01L 27/02**
[52] **U.S. Cl.** **357/40**; 357/34; 357/44; 357/51; 330/268; 330/272
[58] **Field of Search** 357/34, 40, 44, 51; 330/268, 272

[56] **References Cited**

U.S. PATENT DOCUMENTS

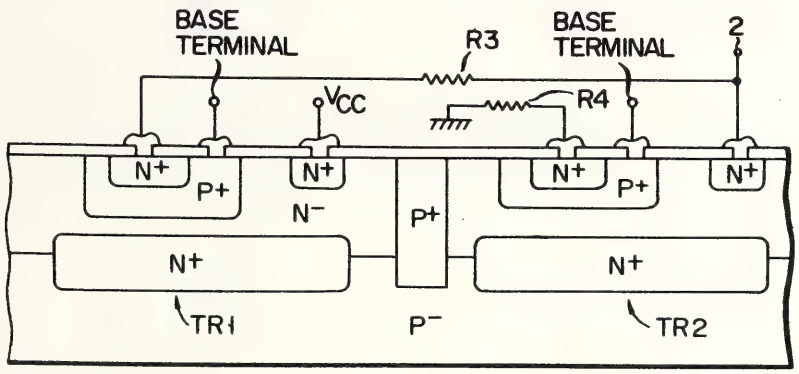
3,961,340 6/1976 Encinas 357/44
3,986,199 10/1976 Williams 357/44

Primary Examiner—Edward J. Wojciechowicz
Attorney, Agent, or Firm—Finnegan, Henderson, Farabow & Garrett

[57] **ABSTRACT**

There is provided a semiconductor integrated circuit device having a Class B push-pull circuit including a first transistor of which the base is connected with a signal source and the collector to a positive power source, and a second transistor of which the collector is connected with the emitter of the first transistor, the base to the signal source, and the emitter to ground. The first transistor has a large area of safe operation compared with the second transistor.

3 Claims, 8 Drawing Figures



United States Patent [19]
Natori et al.
[11] **4,199,772**
[45] **Apr. 22, 1980**

[54] **SEMICONDUCTOR MEMORY DEVICE**

[75] Inventors: **Kenji Natori**, Kamakura; **Fujio Masuoka**, Yokohama, both of Japan
[73] Assignee: **Tokyo Shibaura Electric Co., Ltd.**, Japan

[21] Appl. No.: **847,542**
[22] Filed: **Nov. 1, 1977**

[30] **Foreign Application Priority Data**

Nov. 17, 1976 [JP] Japan 51-138180

[51] **Int. Cl.**[2] **H01L 29/78**
[52] **U.S. Cl.** **357/23**; 357/41; 357/55; 357/14
[58] **Field of Search** 357/23, 41, 55, 14

[56] **References Cited**

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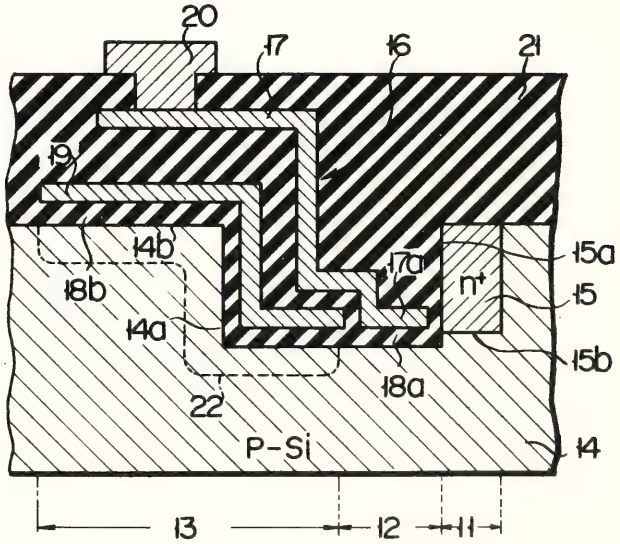
4,012,757 3/1977 Koo 357/24
4,017,883 4/1977 Ho 357/24
4,084,175 4/1978 Ouyang 357/55

Primary Examiner—Martin H. Edlow
Attorney, Agent, or Firm—Finnegan, Henderson, Farabow, Garrett & Dunner

[57] **ABSTRACT**

A semiconductor memory device in which a plurality of unit memory cells are formed on a semiconductor substrate; each memory cell comprises a main electrode region provided with either of the source and drain sections of an MOS transistor, a gate region and an MOS capacitor region, the main electrode region, gate region and capacitor region being arranged in the order mentioned; a recess is formed in a semiconductor region including the gate region and part of the MOS capacitor region; the gate region is formed in one selected portion of the recess-defining wall body; and part of the capacitor electrode of the capacitor region extends over another selected portion of the recess-defining wall body.

11 Claims, 27 Drawing Figures



United States Patent [19]

Satou et al.

[11] **4,209,713**

[45] **Jun. 24, 1980**

[54] **SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE IN WHICH DIFFICULTIES CAUSED BY PARASITIC TRANSISTORS ARE ELIMINATED**

[75] Inventors: **Kazuo Satou**, Yokohama; **Mitsuhiko Ueno**, Fujisawa; **Yasoji Suzuki**, Ayase, all of Japan

[73] Assignee: **Tokyo Shibaura Electric Company, Limited**, Kawasaki, Japan

[21] Appl. No.: **911,164**

[22] Filed: **May 31, 1978**

Related U.S. Application Data

[63] Continuation of Ser. No. 705,960, Jul. 16, 1976, abandoned.

[30] **Foreign Application Priority Data**

Jul. 18, 1975 [JP] Japan 50-87917
Jan. 8, 1976 [JP] Japan 51-1132

[51] **Int. Cl.**[2] **H03K 17/16**; H03K 17/72; H03K 19/40; H01L 27/02

[52] **U.S. Cl.** ..... **307/200 B**; 307/205; 307/213; 307/251; 307/304; 357/42

[58] **Field of Search** ..... 307/200 B, 213, 214, 307/251, 304, 205; 330/207 P; 357/42

[56] **References Cited**

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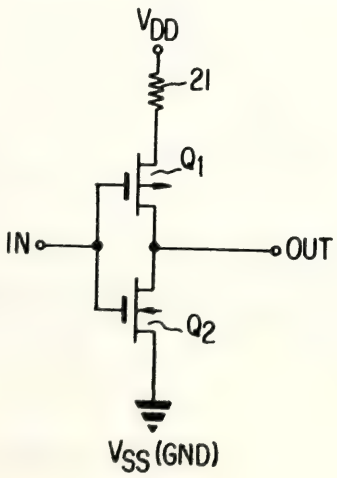
Primary Examiner—Larry N. Anagnos
Attorney, Agent, or Firm—Oblon, Fisher, Spivak, McClelland & Maier

[57] **ABSTRACT**

A semiconductor integrated circuit device comprising a CMOS circuit in which parasitic transistors form a parasitic thyristor circuit. In this device, noise absorption resistances are provided at the noise inputs to absorb noise which otherwise might become trigger pulses for the thyristors.

4 Claims, 9 Drawing Figures



United States Patent [19]

Egawa et al.

[11] **4,209,797**

[45] **Jun. 24, 1980**

[54] **COMPLEMENTARY SEMICONDUCTOR DEVICE**

[75] Inventors: **Hideharu Egawa**, Tokyo; **Koji Matsuki**, Yokohama; **Yasoji Suzuki**, Ayase, all of Japan

[73] Assignee: **Tokyo Shibaura Denki Kabushiki Kaisha**, Japan

[21] Appl. No.: **922,192**

[22] Filed: **Jul. 5, 1978**

[30] **Foreign Application Priority Data**

Jul. 4, 1977 [JP] Japan 52-79045

[51] **Int. Cl.**[2] **H01L 27/02**; H01L 27/12; H01L 29/04

[52] **U.S. Cl.** **357/42**; 357/49; 357/59; 357/91

[58] **Field of Search** 357/42, 59, 91

[56] **References Cited**

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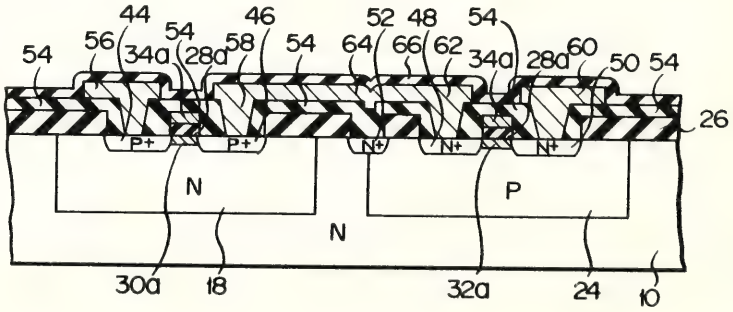
Lin et al., "Shielded silicon gate complementary MOS integrated circuit", IEEE Trans. Electron Devices, vol. ED-19, (11/72), pp. 1199-1207.

Primary Examiner—Gene M. Munson
Attorney, Agent, or Firm—Finnegan, Henderson, Farabow, Garrett & Dunner

[57] **ABSTRACT**

A complementary semiconductor device includes P- and N-type semiconductor regions separately formed in a semiconductor substrate and having substantially the same concentration of impurities. The N- and P-channel type silicon gate field effect transistors are formed in the P- and N-channel type regions, respectively. Gate electrodes of the P-and N-channel type silicon gate field effect transistors are formed by polycrystalline silicons of the same conductivity type. An impurity of the same conductivity type is doped into both the semiconductor regions to provide channel doped regions.

11 Claims, 15 Drawing Figures



United States Patent [19]
Hirasawa et al.
[11] **4,212,025**
[45] **Jul. 8, 1980**

[54] **VOLTAGE DIVIDING INTEGRATED CIRCUIT DEVICE**

[75] Inventors: **Masataka Hirasawa**, Ayase; **Akira Hashimoto; Haruji Yamazaki**, both of Yokohama, allof, Japan

[73] Assignee: **Tokyo Shibaura Electric Co., Ltd.**, Japan

[21] Appl. No.: **873,881**

[22] Filed: **Jan. 31, 1978**

[30] **Foreign Application Priority Data**

Jan. 31, 1977 [JP] Japan 52-9397

[51] **Int. Cl.**[2] **H01L 27/04**
[52] **U.S. Cl.** **357/51**; 357/42; 357/48; 357/86; 357/89
[58] **Field of Search** 357/41, 51, 91, 42, 357/89, 86, 22

[56] **References Cited**

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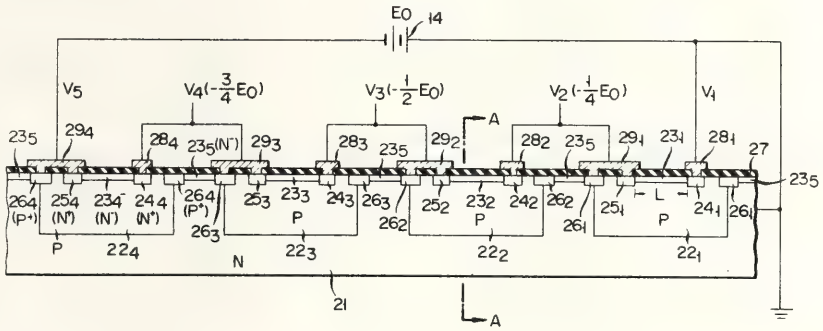
Primary Examiner—William D. Larkins
Attorney, Agent, or Firm—Finnegan, Henderson, Farabow, Garrett & Dunner

[57] **ABSTRACT**

In a first conductivity type semiconductor substrate a plurality of second conductivity type regions are formed. First conductivity type resistivity regions are formed in the second conductivity type regions, respectively. The first conductivity type resistive regions are connected in series between power source terminals, through at least one divided potential taking-out electrode.

3 Claims, 3 Drawing Figures



United States Patent [19]
Matsuda et al.
[11] **4,216,491**
[45] **Aug. 5, 1980**

[54] **SEMICONDUCTOR INTEGRATED CIRCUIT ISOLATED THROUGH DIELECTRIC MATERIAL**

[75] Inventors: **Takashi Matsuda; Kazuo Niwa; Yasusuke Sumitomo**, all of Yokohama, Japan

[73] Assignee: **Tokyo Shibaura Electric Co., Ltd.**, Kawasaki, Japan

[21] Appl. No.: **938,511**

[22] Filed: **Aug. 31, 1978**

Related U.S. Application Data

[63] Continuation of Ser. No. 732,544, Oct. 14, 1976, abandoned.

[30] **Foreign Application Priority Data**

Oct. 15, 1975 [JP] Japan 50-124030

[51] **Int. Cl.**[2] **H01L 27/12**; H01L 29/72; H01L 29/46
[52] **U.S. Cl.** **357/49**; 357/34; 357/67; 357/71
[58] **Field of Search** 357/49, 59, 34

[56] **References Cited**

U.S. PATENT DOCUMENTS

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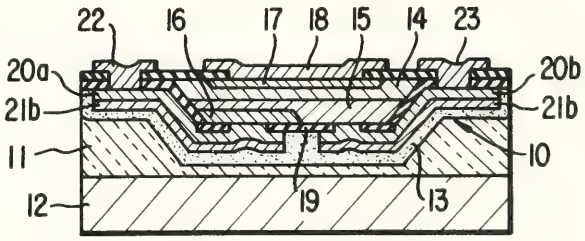
3,942,187	3/1976	Gelsing et al.	357/67
4,131,909	12/1978	Matsuda et al.	357/49

Primary Examiner—Gene M. Munson
Attorney, Agent, or Firm—Oblon, Fisher, Spivak, McClelland & Maier

[57] **ABSTRACT**

A semiconductor integrated circuit which includes a plurality of island regions surrounded by a bottom dish-like dielectric layer formed on one side of a support body. A transistor element is formed in the island region, and the collector region of the transistor element is formed more adjacent to one surface of the island region than the other regions. The emitter and base electrodes of the transistor element are respectively led out from the bottom side of the island region to the surface of the support body using interior leads. The method for manufacturing the above-described device is also disclosed.

5 Claims, 15 Drawing Figures



United States Patent [19]

Masuoka

[11] **4,223,333**

[45] **Sep. 16, 1980**

[54] **CHARGE PUMPING SEMICONDUCTOR MEMORY**

[75] Inventor: **Fujio Masuoka**, Yokohama, Japan

[73] Assignee: **Tokyo Shibaura Denki Kabushiki Kaisha**, Kawasaki, Japan

[21] Appl. No.: **945,347**

[22] Filed: **Sep. 25, 1978**

[30] **Foreign Application Priority Data**

Sep. 30, 1977 [JP] Japan 52-117524

[51] **Int. Cl.**[3] **H01L 27/02**; H01L 29/04; H03K 5/00; G11C 11/34

[52] **U.S. Cl.** **357/41**; 357/54; 357/59; 307/238; 365/154

[58] **Field of Search** 357/41; 307/238; 365/154

[56] **References Cited**

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Iizuka et al., "Electrically Alterable Avalanche-Injection-Type MOS Read-Only Memory With Stacked Gate Structure", IEEE Trans. Electron Devices vol. ED-23 (4/76), pp. 379-387.

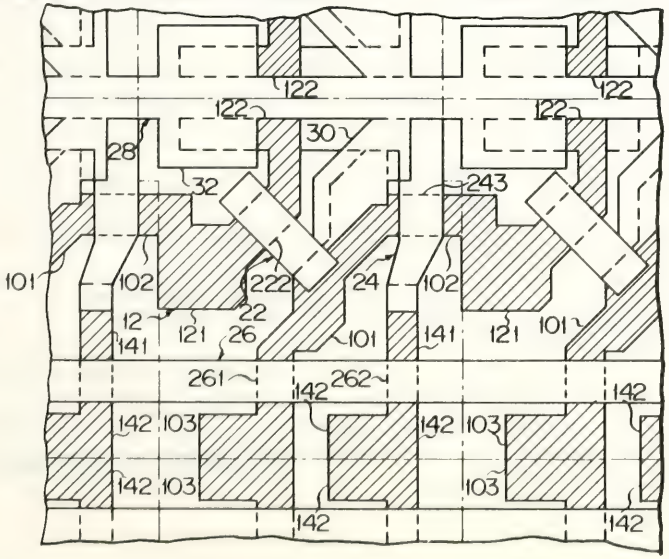
Primary Examiner—Gene M. Munson

Attorney, Agent, or Firm—Oblon, Fisher, Spivak, McClelland & Maier

[57] **ABSTRACT**

There is provided a semiconductor memory apparatus comprising a plurality of memory cells collectively integrated on the same chip in a matrix array and each formed of a flip-flop circuit including a pair of driver MOS transistors, a pair of load MOS capacitors connected to the respective paired driver MOS transistors and address-selection MOS transistors connected to both output terminals of the flip-flop circuit. The memory cells arranged in a row direction are of the same pattern, the adjacent memory cells arranged in a column direction are made symmetrical with each other, the source of one of the paired driver MOS transistors of a given memory cell is connected to the source of the corresponding one of the paired driver MOS transistors of another memory cell disposed adjacent to the first-mentioned memory cell in a row direction, the gates of the driver MOS transistors and address-selection MOS transistors are formed by selectively etching a first polycrystalline silicon layer, and the paired MOS capacitors are constituted by a second polycrystalline layer mounted through an insulation layer over the respective drain regions of the paired driver MOS transistor.

12 Claims, 11 Drawing Figures



United States Patent [19]

Yonezawa et al.

[11] **4,224,636**

[45] **Sep. 23, 1980**

[54] **SEMICONDUCTOR DEVICE WITH THERMALLY COMPENSATING SiO_2-SILICATE GLASS-SIC PASSIVATION LAYER**

[75] Inventors: **Toshio Yonezawa**, Yokosuka; **Takashi Ajima**, Tokyo; **Masato Uchida**, Yokohama, all of Japan

[73] Assignee: **Tokyo Shibaura Electric Co., Ltd.**, Japan

[21] Appl. No.: **915,542**

[22] Filed: **Jun. 14, 1978**

Related U.S. Application Data

[63] Continuation of Ser. No. 753,444, Dec. 22, 1976, abandoned.

[30] **Foreign Application Priority Data**

Dec. 24, 1975 [JP] Japan 50-153379

Mar. 16, 1976 [JP] Japan 51-27650

Mar. 16, 1976 [JP] Japan 51-27651

[51] **Int. Cl.**[2] **H01L 29/34**

[52] **U.S. Cl.** **357/54**; 357/16; 357/49; 357/52; 357/60; 357/71

[58] **Field of Search** 357/16, 54, 52, 71, 357/49, 60; 427/85, 93, 95, 228, 249

[56] **References Cited**

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1143864	2/1969	United Kingdom	357/54
1162565	8/1969	United Kingdom	357/49
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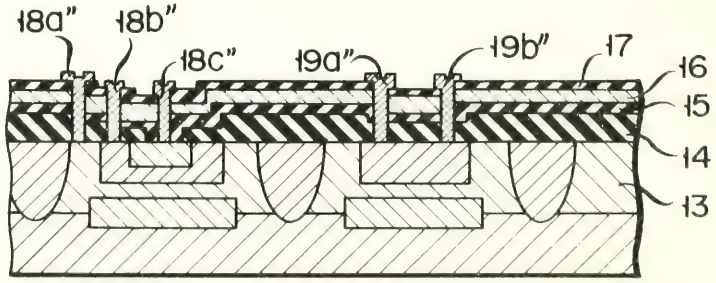
Primary Examiner—Stanley D. Miller, Jr.

Attorney, Agent, or Firm—Finnegan, Henderson, Farabow, Garrett & Dunner

[57] **ABSTRACT**

A semiconductor device comprising a semiconductor substrate and protective films formed thereon. The protective films comprise at least one silicon carbide film which may be pure or may contain particular impurities.

8 Claims, 22 Drawing Figures



United States Patent [19]
Iizuka
[11] **4,231,055**
[45] **Oct. 28, 1980**

[54] **COMPLEMENTARY MOS TRANSISTORS WITHOUT AN ISOLATION REGION**

[75] Inventor: **Tetsuya Iizuka**, Kawasaki, Japan

[73] Assignee: **Tokyo Shibaura Denki Kabushiki Kaisha**, Kawasaki, Japan

[21] Appl. No.: **957,443**

[22] Filed: **Nov. 3, 1978**

[30] **Foreign Application Priority Data**

Nov. 16, 1977 [JP] Japan 52/137649
Nov. 16, 1977 [JP] Japan 52/137650
Nov. 22, 1977 [JP] Japan 52/140204

[51] **Int. Cl.**[2] **H01L 27/02**; H01L 29/78
[52] **U.S. Cl.** **357/42**; 357/23; 357/89
[58] **Field of Search** 357/23, 41, 42

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,840,888	10/1974	Gaensslen et al.	357/42
3,893,155	7/1975	Ogiue	357/42
4,131,907	12/1978	Ouyang	357/42
4,152,717	5/1979	Satou et al.	357/42

OTHER PUBLICATIONS

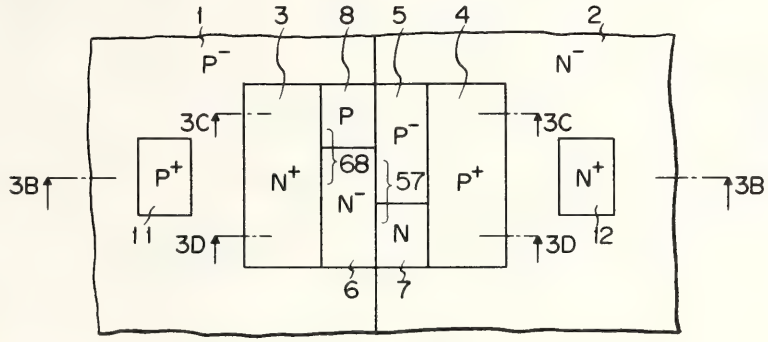
IPRI "Lambda Diodes Utilizing an Enhancement-Depletion C MOS/SOS Process" IEEE Trans. Electron Devices vol. ED-24 pp. 7-12.

Primary Examiner—Gene M. Munson
Attorney, Agent, or Firm—Oblon, Fisher, Spivak, McClelland & Maier

[57] **ABSTRACT**

A first semiconductor region of P− type is formed in a semiconductor substrate of N− types. The N− region adjacent to the first semiconductor region is a second semiconductor region. A third semiconductor region of N+ type and a fourth semiconductor region of P+ type are formed on the first and second semiconductor regions, respectively. Between the first semiconductor region and fourth semiconductor region is formed a first channel region which includes a subregion of P− type and a fifth semiconductor region of N types. Between the second semiconductor region and third semiconductor region is formed a second channel region which includes a subregion of N− type and a sixth semiconductor region of P type. The fourth semiconductor region, the subregion of the first channel region and the sixth semiconductor region are used for a P-channel MOS transistor. The third semiconductor region, the subregion of the second channel region and the fifth semiconductor region are used for an N-channel MOS transistor.

10 Claims, 17 Drawing Figures



United States Patent [19]
Müller
[11] **4,183,036**
[45] **Jan. 8, 1980**

[54] **SCHOTTKY-TRANSISTOR-LOGIC**

[75] Inventor: **Rüdiger Müller**, Munich, Fed. Rep. of Germany

[73] Assignee: **Siemens Aktiengesellschaft**, Berlin & Munich, Fed. Rep. of Germany

[21] Appl. No.: **798,798**

[22] Filed: **May 20, 1977**

[30] **Foreign Application Priority Data**

May 31, 1976 [DE] Fed. Rep. of Germany 2624339
May 31, 1976 [DE] Fed. Rep. of Germany 2624409

[51] **Int. Cl.**[2] **H01L 27/04**; H03K 19/08
[52] **U.S. Cl.** **357/44**; 357/15; 357/46; 357/50; 357/91; 357/92; 148/1.5
[58] **Field of Search** 357/15, 44, 46, 92; 307/213

[56] **References Cited**

U.S. PATENT DOCUMENTS

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4,035,664	7/1977	Berger et al.	357/92
4,053,925	10/1977	Burr et al.	357/91

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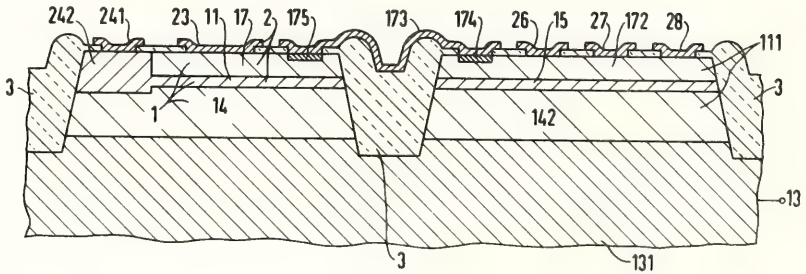
Blatt et al., IEEE IEDM, Technical Digest, (Dec. 1974), pp. 511-514.

Primary Examiner—William D. Larkins
Attorney, Agent, or Firm—Hill, Van Santen, Steadman, Chiara & Simpson

[57] **ABSTRACT**

A Schottky-transistor-logic arrangement is disclosed which comprises a highly doped semiconductor substrate of one conductivity type. An epitaxial layer of the same conductivity type is formed on the substrate. A deep-implanted doped zone of the other conductivity type is located in the epitaxial layer in a plane spaced below the outer surface of said epitaxial layer and lying substantially parallel thereto. A load transistor and an output transistor are formed by constructing the arrangement so that the buried layer provides the base of the load transistor and the emitter of the output transistor. The emitter of the load transistor is provided by a portion of the epitaxial layer which lies below the deep-implanted doped zone. The collector of the load transistor and the base of the output transistor are provided by the portion of the epitaxial layer which lies above the deep-implanted zone. A Schottky electrode on the outer surface of the epitaxial layer provides the collector of the output transistor. A plurality of Schottky diodes are also formed in a portion of the epitaxial layer which possess a lower Schottky barrier than the Schottky electrode of the output transistor.

3 Claims, 6 Drawing Figures



United States Patent [19]

Krause

[11] **4,190,778**

[45] **Feb. 26, 1980**

[54] **A.C. SUPPLIED INTEGRATED SEMI-CONDUCTOR LOGIC CIRCUIT**

[75] Inventor: **Gerhard Krause**, Rosenheim, Fed. Rep. of Germany

[73] Assignee: **Siemens Aktiengesellschaft**, Berlin & Munich, Fed. Rep. of Germany

[21] Appl. No.: **914,842**

[22] Filed: **Jun. 12, 1978**

Related U.S. Application Data

[62] Division of Ser. No. 647,856, Jan. 9, 1976.

[51] **Int. Cl.**[2] **H03K 17/00**

[52] **U.S. Cl.** ..... **307/254**; 307/210; 307/296 A; 307/315; 357/15; 357/36; 357/51; 357/58

[58] **Field of Search** ..... 307/254, 210, 296 A, 307/215, 106, 108; 357/15

[56] **References Cited**

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3,911,466	10/1975	Lattin	357/23
3,953,875	4/1975	Cave et al.	357/51
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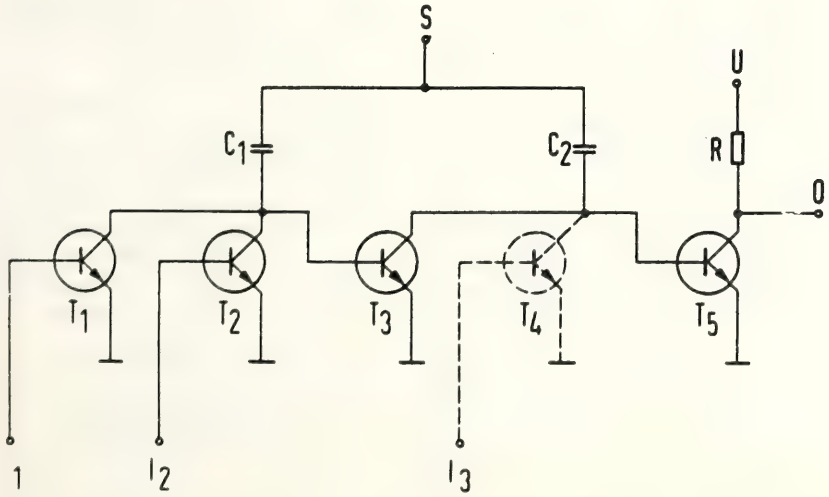
Primary Examiner—Stanley D. Miller, Jr.
Assistant Examiner—B. P. Davis
Attorney, Agent, or Firm—Hill, Van Santen, Steadman, Chiara & Simpson

[57] **ABSTRACT**

An integrated semiconductor circuit arrangement includes active and passive function elements in a semiconductor body and a high frequency a.c. voltage is used as a supply voltage for the function elements. A highly doped semiconductor substrate of one conductivity type carries a weakly doped layer, for example, of the same conductivity which has zones of the opposite conductivity therein. The substrate functions as an emitter for a plurality of transistors of which the doped zones serve as bases. Spaced co-planar layer sections bridge the base zones and serve as collectors. The collectors are either metal layers or semiconductor layers and in either case are covered with an insulating layer which carries a conductive layer for connection to a high frequency supply.

1 Claim, 4 Drawing Figures



United States Patent [19]

Meusburger et al.

[11] **4,197,554**

[45] **Apr. 8, 1980**

[54] **MONOLITHICALLY INTEGRATED CIRCUIT ARRANGEMENT COMPRISING ONE-TRANSISTOR STORAGE ELEMENTS**

[75] Inventors: **Guenther Meusburger**, Munich; **Karlheinrich Horninger**, Eglharting, both of Fed. Rep. of Germany

[73] Assignee: **Siemens Aktiengesellschaft**, Berlin & Munich, Fed. Rep. of Germany

[21] Appl. No.: **898,489**

[22] Filed: **Apr. 20, 1978**

[30] **Foreign Application Priority Data**

May 6, 1977 [DE] Fed. Rep. of Germany 2720533

[51] **Int. Cl.**[2] **H01L 27/02**

[52] **U.S. Cl.** **357/51**; 357/23; 357/41; 357/55; 357/45

[58] **Field of Search** 357/23, 41, 45, 51, 357/55

[56] **References Cited**

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4,115,795	9/1978	Masuoka et al.	357/41

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Electronic Letters—Mar. 18, 1976, pp. 140–141.

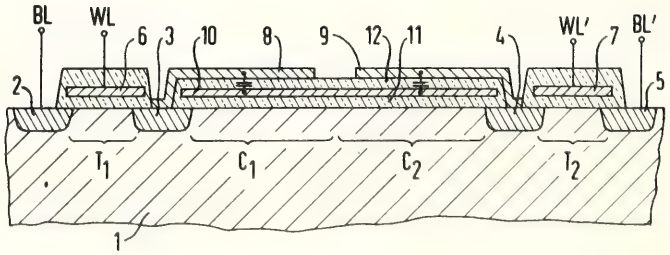
Primary Examiner—Edward J. Wojciechowicz

Attorney, Agent, or Firm—Hill, Van Santen, Steadman, Chiara & Simpson

[57] **ABSTRACT**

A monolithic integrated circuit arrangement is disclosed which is formed of a group of one-transistor storage elements arranged on a semiconductor layer. Each storage element has a selection field effect transistor and a storage capacitor. The storage elements are arranged in pairs. First and second storage capacitors of each pair are combined to save storage area. In one embodiment, a first conductive coating overlying a surface of the semiconductor layer is employed as a common second electrode for all the storage capacitors. Additional second conductive coatings insulated from the first conductive coating and arranged thereover form the first electrodes for the storage capacitors. In another embodiment a first conductive coating is employed as a common second electrode for the storage capacitors. A second conductive coating is utilized as a first electrode for some of the storage electrodes while an inversion or diffusion layer is utilized as a first electrode for the other storage capacitors. In a final embodiment a first conductive coating over the semiconductor layer is utilized as a common second electrode for all of the storage capacitors. A second conductive coating over the first conductive coating and insulated therefrom is utilized as a first electrode for some of the storage capacitors whereas other storage capacitors have their first electrode formed as an inversion layer adjacent to a shift electrode.

11 Claims, 4 Drawing Figures



United States Patent [19]
Hoffmann et al.
[11] **4,206,471**
[45] **Jun. 3, 1980**

[54] **SEMICONDUCTOR STORAGE ELEMENT AND A PROCESS FOR THE PRODUCTION THEREOF**

[75] Inventors: **Kurt Hoffmann**, Taufkirchen; **Reiner Sigusch**, Munich, both of Fed. Rep. of Germany

[73] Assignee: **Siemens Aktiengesellschaft**, Berlin & Munich, Fed. Rep. of Germany

[21] Appl. No.: **943,065**

[22] Filed: **Sep. 18, 1978**

[30] **Foreign Application Priority Data**

Sep. 28, 1977 [DE] Fed. Rep. of Germany 2743619

[51] **Int. Cl.**[2] **H01L 27/10**
[52] **U.S. Cl.** **357/45**; 357/41; 307/238; 29/571
[58] **Field of Search** 357/41, 45, 23; 307/238; 29/571

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,997,799	12/1976	Baker	307/238
4,139,786	2/1979	Raymond et al.	307/238
4,150,389	4/1979	Roessler	357/23

OTHER PUBLICATIONS

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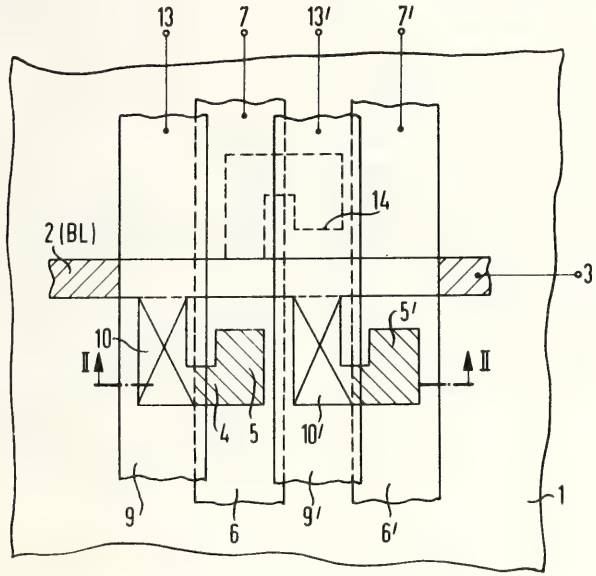
Primary Examiner—Martin H. Edlow
Attorney, Agent, or Firm—Hill, Van Santen, Steadman, Chiara & Simpson

[57] **ABSTRACT**

A semiconductor storage element is disclosed having a storage capacitor whose storage electrode is arranged above a doped semiconductor layer. The storage electrode is formed of a portion of a strip-like reference potential line which is separated from the semiconductor layer by a thin insulating layer. A transfer gate is also provided adjacent to the storage electrode which is formed from a portion of a strip-like word line likewise separated from the semiconductor layer by a thinner insulating layer. An oppositely doped zone is arranged at a surface of the semiconductor layer and serves as a bit line. The word line and the reference potential line run parallel to one another and are arranged directly adjacent to one another. When a potential is connected to the transfer gate, the bit line doped zone may be selectively conductively connected to the storage zone. The reference potential line for one group of the storage elements can be also used as a word line for another group of the storage elements.

11 Claims, 6 Drawing Figures



United States Patent [19]
Hoffmann et al.
[11] **4,208,670**
[45] **Jun. 17, 1980**

[54] **ONE-TRANSISTOR STORAGE ELEMENT AND A PROCESS FOR THE PRODUCTION THEREOF**

[75] Inventors: **Kurt Hoffmann**, Taufkirchen; **Reiner Sigusch**, Munich, both of Fed. Rep. of Germany

[73] Assignee: **Siemens Aktiengesellschaft**, Berlin & Munich, Fed. Rep. of Germany

[21] Appl. No.: **943,066**

[22] Filed: **Sep. 18, 1978**

[30] **Foreign Application Priority Data**

Sep. 28, 1977 [DE] Fed. Rep. of Germany 2743662

[51] **Int. Cl.**[2] **H01L 27/10**
[52] **U.S. Cl.** **357/45**; 357/41; 307/238; 29/571
[58] **Field of Search** 357/45, 41, 23; 307/238; 29/571

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,997,799	12/1976	Boher	307/238
4,139,786	2/1979	Raymond	307/238
4,150,389	4/1979	Roessler	397/23

OTHER PUBLICATIONS

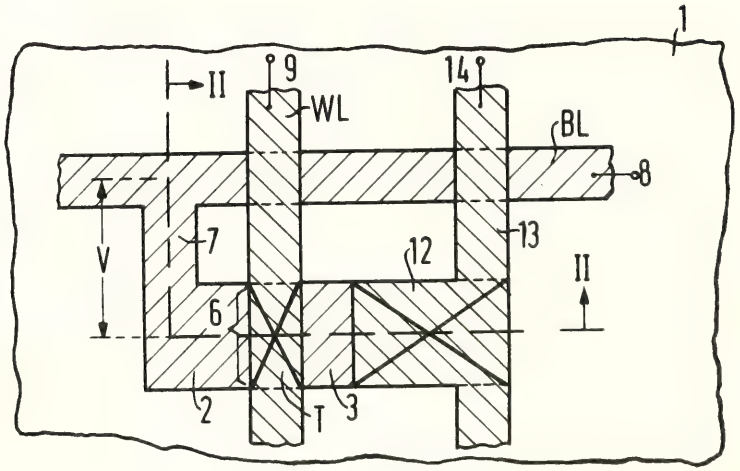
Stein, *IEEE Journ. of Solid State Circuits*, vol. SC-8, No. 5, Oct. 1973.

Primary Examiner—Martin H. Edlow
Attorney, Agent, or Firm—Hill, Van Santen, Steadman, Chiara & Simpson

[57] **ABSTRACT**

A one-transistor storage element system and a method for producing the same is disclosed wherein each storage element has a sselector field effect transistor and a storage capacitor. A doped semiconductor layer is provided having an oppositely doped bit line provided at a surface thereof, an oppositely doped source zone connecting to the bit line by an oppositely doped connecting zone, and an oppositely doped drain zone also provided at a surface of the semiconductor layer. An insulating layer is provided over the surface of the semiconductor layer and an electrically conductive coating is provided thereon. A first separate part of the conductive coating forms a word line which is positioned over a gap between the source and drain zones. Portions of the word line form a gate beneath which a channel of the transistor is formed. A second separate part of the electrically conductive coating is formed over a portion of the semiconductor layer adjacent the drain zone and forms one of the electrodes of the storage capacitor. The other electrode of the storage capacitor is either provided as a diffusion zone in the semiconductor layer or may be an induced zone. A reference potential line formed by a connecting third part of the electrical conductive layer is also provided.

10 Claims, 8 Drawing Figures



United States Patent [19]

Werner

[11] **4,220,961**

[45] **Sep. 2, 1980**

[54] **MONOLITHIC COMBINATION OF TWO COMPLEMENTARY BIPOLAR TRANSISTORS**

[75] Inventor: **Wolfgang Werner**, Munich, Fed. Rep. of Germany

[73] Assignee: **Siemens Aktiengesellschaft**, Berlin & Munich, Fed. Rep. of Germany

[21] Appl. No.: **971,007**

[22] Filed: **Dec. 19, 1978**

[30] **Foreign Application Priority Data**

Dec. 23, 1977 [DE] Fed. Rep. of Germany 2757762

[51] **Int. Cl.**[2] **H01L 27/02**

[52] **U.S. Cl.** **357/46**; 357/59; 357/92

[58] **Field of Search** 357/46, 59, 92

[56] **References Cited**

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IEEE Inter. Solid State Circuits Conf.—Feb. 1975, pp. 172-173.

Primary Examiner—Edward J. Wojciechowicz

Attorney, Agent, or Firm—Hill, Van Santen, Steadman, Chiara & Simpson

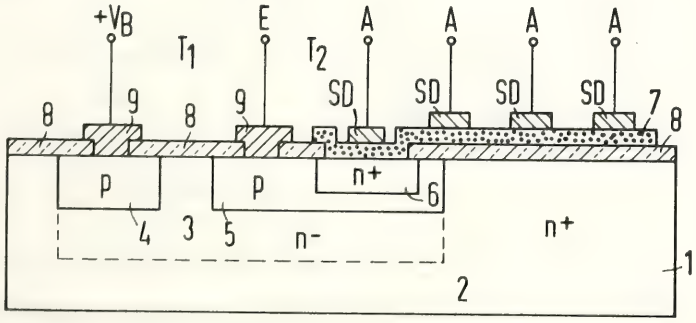
[57] **ABSTRACT**

In the production of integrated I²L-circuits, a lateral transistor and a vertical transistor are generated next to one another on the surface of a monocrystalline semiconductor body. Thereby, it is seen to that the base zone of the vertical transistor coincides with the collector zone of the lateral transistor and the base zone of the lateral transistor coincides with the emitter zone of the vertical transistor. Further, it is known to provide at least one collector zone of monocrystalline semiconductor material belonging to the vertical transistor and marked off from the base zone of this transistor by a pn-junction and to provide a Schottky contact as collector electrode.

The invention makes provisions for applying a polycrystalline layer of the same semiconductor material and the doping of the collector zone on the surface of the monocrystalline collector zone and then making this the carrier of the collector electrode or collector electrodes, respectively.

In addition to reducing the effort otherwise required, an increase of the component density as well as a series of structural improvements can be attained.

13 Claims, 7 Drawing Figures



United States Patent [19]

Mauthe

[11] **4,224,635**

[45] **Sep. 23, 1980**

[54] **DYNAMIC STORAGE ELEMENT HAVING STATIC STORAGE ELEMENT BEHAVIOR**

[75] Inventor: **Manfred Mauthe**, Munich, Fed. Rep. of Germany

[73] Assignee: **Siemens Aktiengesellschaft**, Berlin & Munich, Fed. Rep. of Germany

[21] Appl. No.: **922,747**

[22] Filed: **Jul. 7, 1978**

[30] **Foreign Application Priority Data**

Jul. 29, 1977 [DE] Fed. Rep. of Germany 2734354

[51] **Int. Cl.**[2] **H01L 27/02**; H01L 29/78; H01L 29/34; H03K 5/00

[52] **U.S. Cl.** **357/41**; 357/23; 357/24; 357/54; 357/91; 307/238; 365/149

[58] **Field of Search** ..... 357/23, 24, 41, 54; 307/221 D, 238; 365/149, 182

[56] **References Cited**

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Tasch et al., "The Charge-Coupled Ram Cell Concept" IEEE J. Solid-State Circuits, vol. SC-11 (2/76) pp. 58-63.

Spampinato et al., "Single Electrode One-Device Cell" IBM Technical Disclosure Bulletin vol. 15, (11/72) pp. 2019-2020.

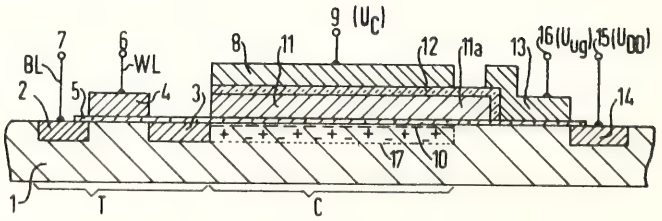
Primary Examiner—Gene M. Munson

Attorney, Agent, or Firm—Hill, Van Santen, Steadman, Chiara & Simpson

[57] **ABSTRACT**

A storage element comprises a storage capacitor which has a storage electrode, arranged insulated over a doped semiconductor layer, connected to a constant voltage, and a selection element which manifest a gate connected to a word line, arranged in an insulated manner above the semiconductor layer. A source zone connected to a bit line is oppositely doped and arranged at the surface of the semiconductor layer. The selection element selectively connects the source zone to a surface storage region of the semiconductor layer which is disposed beneath the storage electrode. Between the storage electrode and the semiconductor layer an insulated electrode is provided and the semiconductor layer is additionally p-doped and n-doped in a zone beneath a portion, adjacent the selection element, of the electrode and an overflow electrode and an oppositely doped drain zone are provided on the side of the electrode opposite the selection element.

6 Claims, 4 Drawing Figures



United States Patent [19]

Horninger

[11] **4,225,876**

[45] **Sep. 30, 1980**

[54] **MONOLITHICALLY INTEGRATED SEMICONDUCTOR ARRANGEMENT**

[75] Inventor: **Karlheinrich Horninger**, Eglharting, Fed. Rep. of Germany

[73] Assignee: **Siemens Aktiengesellschaft**, Berlin & Munich, Fed. Rep. of Germany

[21] Appl. No.: **939,485**

[22] Filed: **Sep. 5, 1978**

[30] **Foreign Application Priority Data**

Sep. 6, 1977 [DE] Fed. Rep. of Germany 2740154

[51] **Int. Cl.**[2] **H01L 27/14**

[52] **U.S. Cl.** **357/23**; 357/41; 307/238; 357/45

[58] **Field of Search** 357/23, 41, 45; 365/103; 307/238

[56] **References Cited**

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4,075,045	2/1978	Rideout	148/187
4,125,854	11/1978	McKenny	357/41
4,131,906	12/1978	Kinoshita	357/41
4,150,389	4/1979	Roessler	357/23

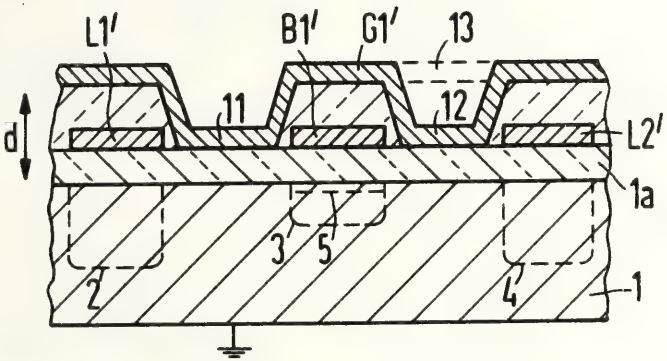
Primary Examiner—Martin H. Edlow

Attorney, Agent, or Firm—Hill, Van Santen, Steadman, Chiara & Simpson

[57] **ABSTRACT**

A monolithically integrated semiconductor arrangement is disclosed wherein a plurality of first lines are provided which run parallel to one another and which are provided with first terminals at one end. A plurality of second lines which run parallel to one another are also provided which cross beneath the first lines and are connected via load elements at one end to a supply voltage terminal. Reference potential lines are also provided adjacent each of the second lines. At a series of selected crossing points of the first and second lines coupling elements are formed which can be operated by the first line and by which the second line is connected to an adjacent reference potential line. The semiconductor arrangement is formed on a semiconductor layer having a thin insulating layer thereon with the second lines and reference potential lines arranged on the thin insulating layer. The first lines are then arranged over the second line and reference potential lines and are separated therefrom by an additional insulating layer. At crossing points selected for coupling, a portion of the first line approaches the semiconductor layer surface more closely and is separated therefrom by the thin insulating line. Diffusion zones are provided at one end of each of the reference potential lines and second lines. With the system disclosed, diffusions are not required for the formation of the first and second lines and coupling elements.

9 Claims, 4 Drawing Figures



United States Patent [19]

Le Can et al.

[11] **4,183,037**

[45] **Jan. 8, 1980**

[54] **SEMICONDUCTOR DEVICE**

[75] Inventors: **Claude J. P. F. Le Can**, Nijmegen; **Cornelis M. Hart**; **Hendricus E. J. Wulms**, both of Eindhoven, all of Netherlands

[73] Assignee: **U.S. Philips Corporation**, New York, N.Y.

[21] Appl. No.: **847,723**

[22] Filed: **Nov. 2, 1977**

[30] **Foreign Application Priority Data**

Jan. 17, 1977 [NL] Netherlands 7700420

[51] **Int. Cl.**[2] **H01L 27/04**

[52] **U.S. Cl.** **357/44**; 357/59; 357/71; 357/92

[58] **Field of Search** 354/40, 35, 92, 59, 354/71, 44

[56] **References Cited**

U.S. PATENT DOCUMENTS

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4,056,810	11/1977	Hart et al.	357/35 X
4,078,208	3/1978	Hart et al.	357/92 X
4,109,275	8/1978	Sarkary	357/71 X

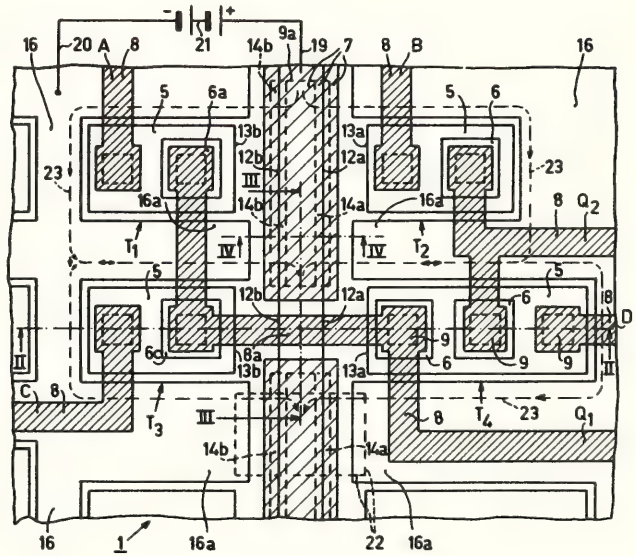
Primary Examiner—James W. Davie

Attorney, Agent, or Firm—Thomas A. Briody; Edward J. Connors, Jr.; James J. Cannon, Jr.

[57] **ABSTRACT**

The invention relates to a semiconductor device in which a crossing connection is realized by using parts of a layer of refractory conductive material already present for masking as a part of a current conductor separated from a crossing conductor by an insulation layer. The mask of refractory material may also define the regions in which switching transistors are realized. The invention results in important advantages, in connection with density and crossing connections, in particular in I^2L-circuits.

9 Claims, 15 Drawing Figures



United States Patent [19]

Gaffre

[11] **4,198,251**

[45] **Apr. 15, 1980**

[54] **METHOD OF MAKING POLYCHROMATIC MONOLITHIC ELECTROLUMINESCENT ASSEMBLY UTILIZING EPITAXIAL DEPOSITION OF GRADED LAYERS**

[75] Inventor: **Michel Gaffre**, Caen, France

[73] Assignee: **U.S. Philips Corporation**, New York, N.Y.

[21] Appl. No.: **863,456**

[22] Filed: **Dec. 22, 1977**

Related U.S. Application Data

[60] Continuation of Ser. No. 836,607, Sep. 26, 1977, abandoned, which is a division of Ser. No. 721,289, Sep. 8, 1976, abandoned.

[30] **Foreign Application Priority Data**

Sep. 18, 1975 [FR] France 75 28632

[51] **Int. Cl.**[2] **H01L 21/20**; H01L 21/82

[52] **U.S. Cl.** ..... **148/175**; 29/569 L; 148/187; 307/311; 313/500; 357/16; 357/17; 357/45; 357/88; 357/90

[58] **Field of Search** ..... 148/175, 187; 29/569 L, 29/576 E, 578; 313/500; 357/16, 17, 45, 90, 88; 250/211 J; 307/311

[56] **References Cited**

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3,566,218	2/1971	Widlar et al.	148/187 X
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3,890,170	6/1975	Russ	148/175
3,947,840	3/1976	Craford et al.	313/500 X
3,964,940	6/1976	Hart et al.	148/175
4,001,056	1/1977	Groves et al.	148/175
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Murray et al., "Lighting up in a Group", Electronics, Mar. 4, 1968, pp. 104-110.

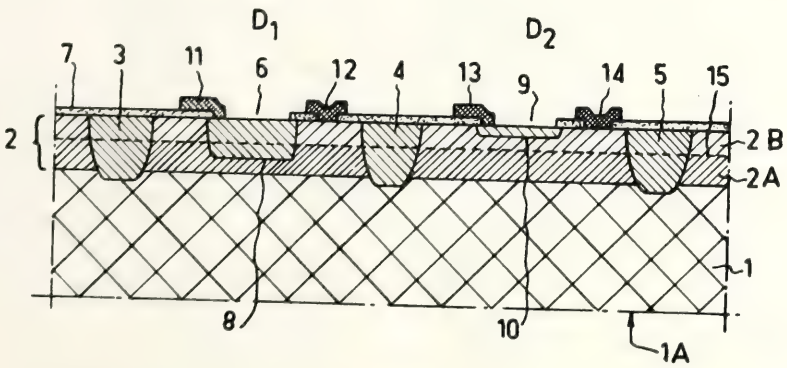
Craford et al., "L.E.D. Technology", Solid State Technology, Jan. 1974, pp. 39-58.

Primary Examiner—L. Dewayne Rutledge
Assistant Examiner—W. G. Saba
Attorney, Agent, or Firm—Thomas A. Briody; Paul R. Miller

[57] **ABSTRACT**

A monolithic assembly comprising electroluminescent diodes emitting radiations of different wavelengths. The junctions of the said diodes are established in different sectors of a layer of a semiconductor compound where the concentration of a given impurity is variable. Also, the manufacture of polychromatic integrated emission devices.

3 Claims, 2 Drawing Figures



United States Patent [19]

van Gils

[11] **4,199,378**

[45] **Apr. 22, 1980**

[54] **METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE MANUFACTURED WHILE USING SUCH A METHOD**

[75] Inventor: **Johannes A. A. van Gils**, Eindhoven, Netherlands

[73] Assignee: **U.S. Philips Corporation**, New York, N.Y.

[21] Appl. No.: **935,025**

[22] Filed: **Aug. 18, 1978**

[30] **Foreign Application Priority Data**

Aug. 25, 1977 [NL] Netherlands 7709363

[51] **Int. Cl.**[2] **H01L 21/225**; H01L 21/26; H01L 27/04

[52] **U.S. Cl.** **148/1.5**; 148/187; 357/44; 357/50; 357/91

[58] **Field of Search** 148/1.5, 187, 175; 357/91, 44, 50

[56] **References Cited**

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4,029,527	6/1977	Glasl et al.	148/187
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Graul et al., ". . . Double Implanted Transistors," IEEE J. Solid St. Circuit, vol. SC-10, (1971), 201.

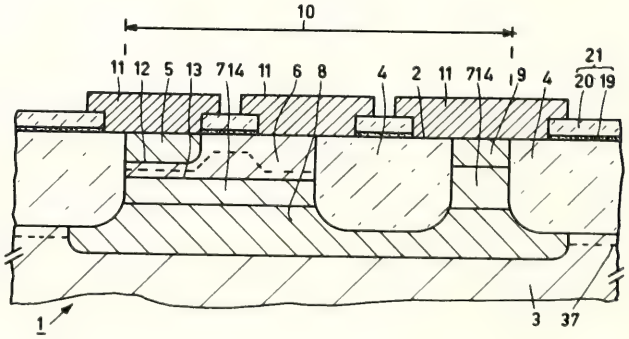
Jambotkar, ". . . Bipolar Transistors," IBM-TDB, 19, (1977), 4601.

Primary Examiner—L. Dewayne Rutledge
Assistant Examiner—Upendra Roy
Attorney, Agent, or Firm—Thomas A. Briody; Jack Oisher; Steven R. Biren

[57] **ABSTRACT**

A method of manufacturing LOCOS transistors in which base doping, emitter doping and emitter metallization are provided via the same aperture. Problems at the edge of the sunken oxide are eliminated by a two-stage doping technique so that the channel stopper diffusion in the epitaxial layer may be omitted, which presents particular advantages in the manufacture of I^2L devices.

15 Claims, 17 Drawing Figures



United States Patent [19]
Gee et al.
[11] **4,218,693**
[45] **Aug. 19, 1980**

[54] **INTEGRATED LOGIC CIRCUIT HAVING INTERCONNECTIONS OF VARIOUS LENGTHS BETWEEN FIELD EFFECT TRANSISTORS OF ENHANCEMENT AND DEPLETION MODES**

[75] Inventors: **Lawrence F. Gee; Denis B. Jarvis,** both of Chandlers Ford; **Christopher J. Aldhous,** Southampton, all of England

[73] Assignee: **U.S. Philips Corporation,** New York, N.Y.

[21] Appl. No.: **868,052**

[22] Filed: **Jan. 9, 1978**

[30] **Foreign Application Priority Data**

Jan. 17, 1977 [GB] United Kingdom 1788/77

[51] **Int. Cl.**[2] **H01L 27/02;** H01L 29/78; H01L 27/10; H03K 3/353

[52] **U.S. Cl.** **357/41;** 357/23; 357/45; 357/59; 357/91; 307/304

[58] **Field of Search** 357/23, 41, 45; 307/304

[56] **References Cited**

U.S. PATENT DOCUMENTS

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4,110,776	8/1978	Rao et al.	357/23
4,125,854	11/1978	McKenny et al.	357/41

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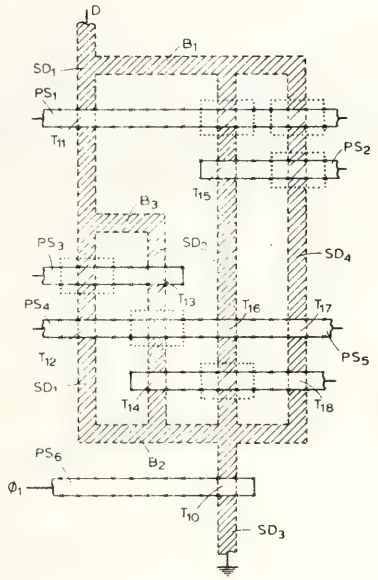
Kawagoe et al "Minimum Size ROM Structure Compatible with Silicon-Gate E/D MOS LSI" IEEE J. Solid-State Circuits vol. SC-11 (6/76) pp. 360-364.

Primary Examiner—Gene M. Munson
Attorney, Agent, or Firm—Thomas A. Briody; Jack Oisher; Steven R. Biren

[57] **ABSTRACT**

An integrated logic circuit includes an array of insulated gate field effect transistors formed at the crossings of a plurality of substantially parallel first conductor tracks which form the transistor gate electrodes and a plurality of substantially parallel strip-shaped surface regions which form the source and drain electrode regions of the transistors. The field effect transistors of the device include a first group of transistors having a first threshold voltage and a second group of transistors having a second threshold voltage different from the first. In order to make a more compact, easily-designed and easily-manufactured circuit, the conductor tracks and the strip-shaped surface regions form a nonuniform array in which the track and surface regions need not all be of the same length. Further efficiencies are achieved by branching the strip-shaped surface regions where appropriate to implement the desired logic combination.

11 Claims, 7 Drawing Figures



United States Patent [19]
David
[11] **4,219,368**
[45] **Aug. 26, 1980**

[54] **SEMICONDUCTOR DEVICE HAVING A NUMBER OF SERIES-ARRANGED PHOTOSENSITIVE CELLS**

[75] Inventor: **Gérard R. David,** Cambes en Plaine, France

[73] Assignee: **U.S. Philips Corporation,** New York, N.Y.

[21] Appl. No.: **37,784**

[22] Filed: **May 10, 1979**

[30] **Foreign Application Priority Data**

May 19, 1978 [FR] France 78 14890

[51] **Int. Cl.**[2] **H01L 31/06**

[52] **U.S. Cl.** ..... **136/89 MS;** 357/30; 357/47; 357/48; 357/55

[58] **Field of Search** ..... 136/89 MS; 357/30, 47, 357/48, 55

[56] **References Cited**

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4,156,309	5/1979	Routh et al.	29/572

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1010476 11/1965 United Kingdom ..... 136/89 MS

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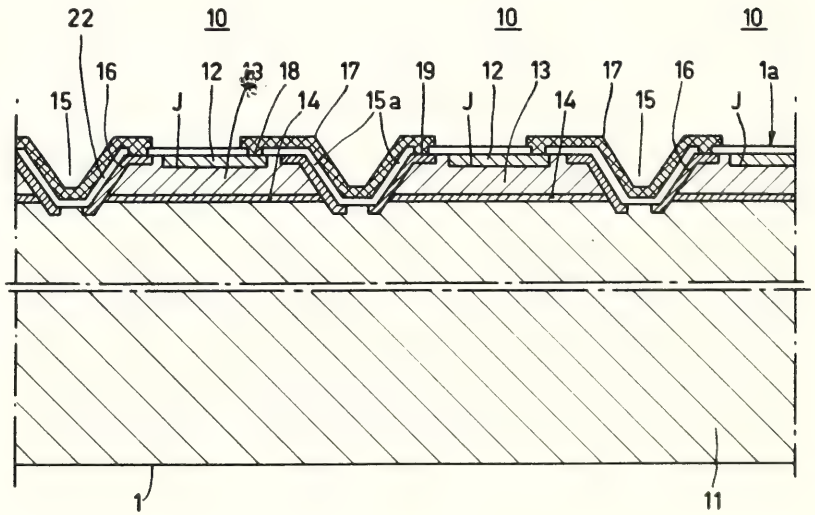
A. I. Bennett et al., "An Integrated High-Voltage Solar Cell," *Conf. Record, IEEE Photovoltaic Specialists' Conf.* (1967), pp. 148-159.

Primary Examiner—Aaron Weisstuch
Attorney, Agent, or Firm—Thomas A. Briody; Steven R. Biren

[57] **ABSTRACT**

A semiconductor device having a number of series-arranged photosensitive cells which are provided on a common substrate of a first conductivity type and which are separated by grooves extending down to the substrate. The cells consist of first regions of a first conductivity type which form planar photosensitive junctions with second regions of the second conductivity type. According to the invention, a highly doped layer of the second conductivity type is present between the substrate and the second region and each photosensitive cell is provided, along at least a part of its circumference, with a highly doped semiconductor zone of the second conductivity type which extends along the wall of the groove down to the highly doped layer and is separated from the adjacent cell by the substrate.

5 Claims, 6 Drawing Figures



United States Patent [19]
Moussie
[11] **4,229,757**
[45] **Oct. 21, 1980**

[54] **PROGRAMMABLE MEMORY CELL HAVING SEMICONDUCTOR DIODES**

[75] Inventor: **Michel Moussie**, Caen, France

[73] Assignee: **U.S. Philips Corporation**, New York, N.Y.

[21] Appl. No.: **938,470**

[22] Filed: **Aug. 31, 1978**

[30] **Foreign Application Priority Data**

Sep. 30, 1977 [FR] France 77 29476

[51] **Int. Cl.**[2] **H01L 27/10**; G11C 17/06; H01L 29/04

[52] **U.S. Cl.** **357/59**; 357/4; 357/45; 365/96; 365/105

[58] **Field of Search** 357/45, 51, 59, 4, 68, 357/71; 307/238; 365/96, 103, 105

[56] **References Cited**

U.S. PATENT DOCUMENTS

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3,634,929	1/1972	Yoshida et al.	357/45
3,641,516	2/1972	Castrucci	357/45
3,781,825	12/1973	Buirker et al.	357/45
4,145,702	3/1979	Rau	357/45
4,146,902	3/1979	Tanimoto et al.	357/23

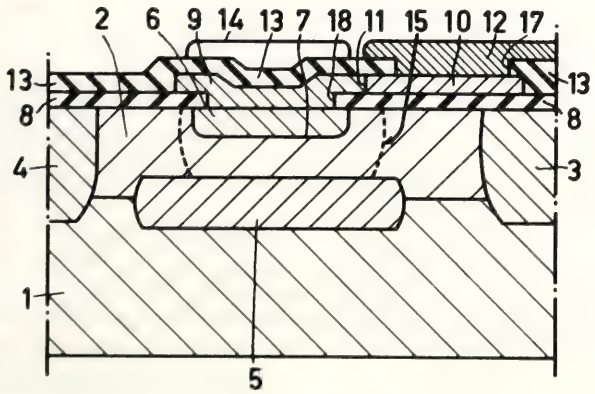
Primary Examiner—William D. Larkins
Attorney, Agent, or Firm—Thomas A. Briody; Jack Oisher; James J. Cannon, Jr.

[57] **ABSTRACT**

Integrated electrically programmable read only memory cell having at least two back-to-back diodes.

A first diode is formed by a planar junction (7) between two superimposed regions (2, 6), the second diode is programmable and is formed by a lateral junction (11) between two coplanar zones (9, 10) of a thin semi-conductor layer isolated from the body by an insulating layer (8) having a contact aperture (18).

9 Claims, 6 Drawing Figures



United States Patent [19]
Uehara et al.
[11] **4,197,555**
[45] **Apr. 8, 1980**

[54] **SEMICONDUCTOR DEVICE**

[75] Inventors: **Takao Uehara**, Tokyo; **Takamitsu Tsuchimoto**, Machida; **Katsuyuki Hamada**, Kawasaki; **Hideo Masuzawa**, Tokyo; **Makoto Mukai**, Hino, all of Japan

[73] Assignee: **Fujitsu Limited**, Japan

[21] Appl. No.: **925,788**

[22] Filed: **Jul. 18, 1978**

Related U.S. Application Data

[63] Continuation of Ser. No. 752,922, Dec. 21, 1976, abandoned.

[30] **Foreign Application Priority Data**

Dec. 29, 1975 [JP] Japan 50-159004
Feb. 28, 1976 [JP] Japan 51-21418
Feb. 28, 1976 [JP] Japan 51-21419

[51] **Int. Cl.**[2] **H01L 23/48**

[52] **U.S. Cl.** **357/70**; 357/40; 357/68; 357/71

[58] **Field of Search** 357/40, 68, 70, 71

[56] **References Cited**

U.S. PATENT DOCUMENTS

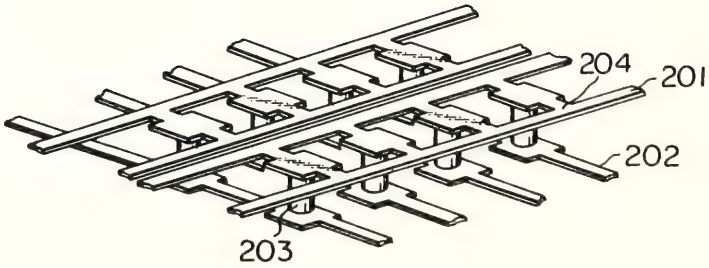
3,936,865	2/1976	Robinson	357/68
4,006,492	2/1977	Eichelberger	357/68

Primary Examiner—Edward J. Wojciechowicz
Attorney, Agent, or Firm—Staas & Halsey

[57] **ABSTRACT**

An electronic device which includes at least one semiconductor chip with at least one circuit element thereon and connection patterns thereon being connected to the circuit element or elements. The connection patterns comprise a lower connection pattern, which is standardized and widely applicable to many kinds of circuits, and an upper connection pattern, which is positioned on the upper side of said lower connection pattern. The upper connection pattern and the lower connection pattern are connected in conformity with the desired circuit to be obtained.

11 Claims, 28 Drawing Figures



United States Patent [19]

Takagi et al.

[11] **4,210,473**

[45] **Jul. 1, 1980**

[54] **PROCESS FOR PRODUCING A SEMICONDUCTOR DEVICE**

[75] Inventors: **Mikio Takagi**, Kawasaki; **Hajime Kamioka**, Yokohama; **Haruo Shimoda**, Tokyo; **Hidekazu Miyamoto**, Machida, all of Japan

[73] Assignee: **Fujitsu Limited**, Japan

[21] Appl. No.: **955,754**

[22] Filed: **Oct. 30, 1978**

[30] **Foreign Application Priority Data**

Nov. 29, 1977 [JP] Japan 52-143189

[51] **Int. Cl.**[2] **H01L 21/223**

[52] **U.S. Cl.** **148/189**; 29/571; 148/187; 148/188

[58] **Field of Search** 148/189, 187, 188; 29/571

[56] **References Cited**

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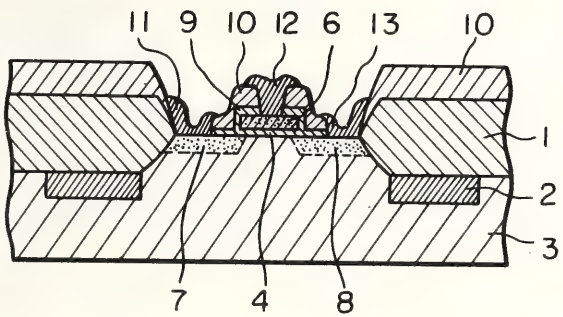
3,658,606	4/1972	Lyons et al.	148/187
3,699,646	10/1972	Vadasz	29/571
3,852,128	12/1974	Kreuzer	148/189
3,883,372	5/1975	Lin	148/188 X
3,972,756	8/1976	Nagase et al.	148/187 X
3,986,903	10/1976	Watrous	148/187

Primary Examiner—G. Ozaki
Attorney, Agent, or Firm—Staas & Halsey

[57] **ABSTRACT**

Disclosed is a process for producing a semiconductor device, especially, a high speed silicon gate field effect semiconductor device, by diffusing an impurity substance, such as arsenic or phosphorus, into a polycrystalline silicon layer to be converted into a silicon gate having a high electroconductivity and into portions of a single crystal silicon substrate to be converted into source and drain regions, in a sealed capsule, at an elevated temperature, under a vacuum. During the above-mentioned diffusing operation, the impurity substance can diffuse into the polycrystalline silicon layer at a higher diffusing speed than into the single crystal silicon substrate.

26 Claims, 8 Drawing Figures



United States Patent [19]

Mogi et al.

[11] **4,224,633**

[45] **Sep. 23, 1980**

[54] **IGFET STRUCTURE WITH AN EXTENDED GATE ELECTRODE END**

[75] Inventors: **Jun-ichi Mogi**, Kawasaki; **Kiyoshi Miyasaka**; **Seiji Enomoto**, both of Yokohama, all of Japan

[73] Assignee: **Fujitsu Limited**, Kawasaki, Japan

[21] Appl. No.: **908,835**

[22] Filed: **May 23, 1978**

[51] **Int. Cl.**[2] **H01L 29/78**

[52] **U.S. Cl.** **357/23**; 357/41; 357/68

[58] **Field of Search** 357/23, 41, 68

[56] **References Cited**

U.S. PATENT DOCUMENTS

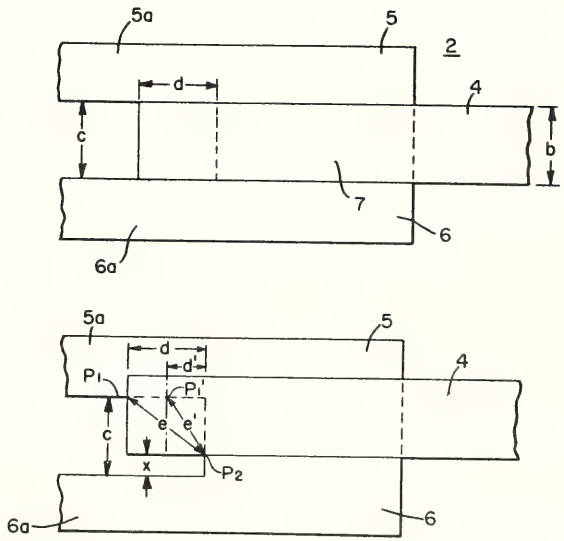
3,694,673	9/1972	Au	307/304

Primary Examiner—Martin H. Edlow
Attorney, Agent, or Firm—Staas & Halsey

[57] **ABSTRACT**

Self-aligned IGFET structure having a source region, a drain region and a gate electrode placed between the source and drain regions to define a channel region. The gate electrode is provided with an extended end portion on a relatively thick field oxide layer and having a length no less than a predetermined channel length on one side of the channel region so that the breakdown voltage is not decreased on that one side of the channel region.

8 Claims, 7 Drawing Figures



United States Patent [19]

Togei

[11] **4,228,444**

[45] **Oct. 14, 1980**

[54] **SEMICONDUCTOR DEVICE**

[75] Inventor: **Ryoiku Togei**, Kawasaki, Japan

[73] Assignee: **Fujitsu Limited**, Kanagawa, Japan

[21] Appl. No.: **947,050**

[22] Filed: **Sep. 29, 1978**

Related U.S. Application Data

[63] Continuation of Ser. No. 794,518, May 6, 1977, abandoned.

[30] **Foreign Application Priority Data**

May 28, 1976 [JP] Japan 51/62606

[51] **Int. Cl.**[2] **H01L 29/80**

[52] **U.S. Cl.** **357/22**; 357/23; 357/13; 357/45

[58] **Field of Search** 357/23, 22, 13, 45

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,896,483 7/1975 Whelan 357/23

3,988,761 10/1976 Kanazawa 357/23

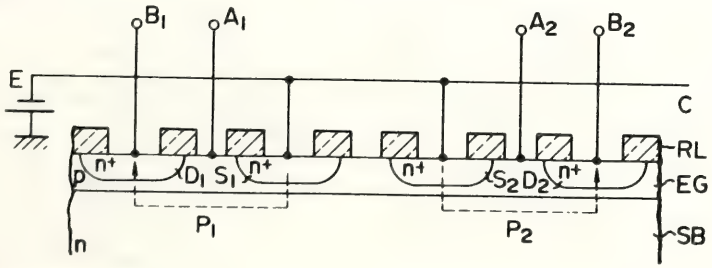
Primary Examiner—Edward J. Wojciechowicz

Attorney, Agent, or Firm—Staas & Halsey

[57] **ABSTRACT**

On a semiconductor substrate (or layer) of one conductivity type, a semiconductor layer of the opposite conductivity type is formed and a source and a drain region of the same conductivity type as the semiconductor substrate are formed in the semiconductor layer. Junctions are respectively formed between the source and drain regions and the semiconductor layer at such positions where punch-through may easily occur between the source and drain regions and the semiconductor substrate when operating voltages are applied to these regions. A local potential distribution generation electrode, which makes an ohmic contact with the semiconductor layer, is formed between the source and drain regions. By applying voltages to both the local potential distribution generation electrode and a drain electrode at substantially the same time, a potential barrier normally formed in the semiconductor layer is removed, thereby to inject carriers from the source region to the drain region through the semiconductor substrate (or layer).

8 Claims, 6 Drawing Figures



United States Patent [19]

Momma et al.

[11] **4,231,057**

[45] **Oct. 28, 1980**

[54] **SEMICONDUCTOR DEVICE AND METHOD FOR ITS PREPARATION**

[75] Inventors: **Yoshinobu Momma**, Sagamihara; **Yunosuke Kawabe**, Yokohama; **Osamu Hataishi**, Kawasaki, all of Japan

[73] Assignee: **Fujitsu Limited**, Kawasaki, Japan

[21] Appl. No.: **960,228**

[22] Filed: **Nov. 13, 1978**

[51] **Int. Cl.**[3] **H01L 27/04**

[52] **U.S. Cl.** **357/50**; 357/47; 357/23; 357/55

[58] **Field of Search** 357/49, 55, 50, 23

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,047,195 9/1977 Allison 357/55

4,048,649 9/1977 Bohn 357/4.3

4,051,506 9/1977 Horie 357/55

4,106,050 8/1978 Riseman 357/49

4,140,558 2/1979 Murphy 148/175

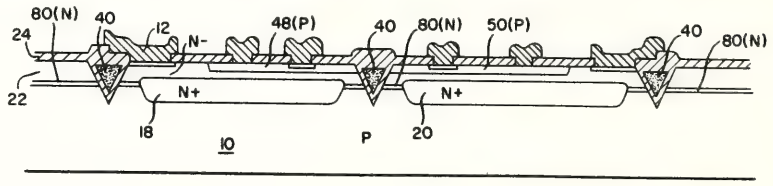
Primary Examiner—Martin H. Edlow

Attorney, Agent, or Firm—Staas & Halsey

[57] **ABSTRACT**

An improved means and method for isolating semiconductor devices on a semiconductor substrate, comprising a shallow region formed between the semiconductor substrate and an epitaxial layer of each device, and between a buried layer of each device and an isolation region separating adjacent devices. The shallow region has conductivity type opposite to that of the semiconductor substrate and higher impurity concentration than that of the epitaxial layer.

10 Claims, 21 Drawing Figures



100

United States Patent [19]
Redfern
[11] **4,190,854**
[45] **Feb. 26, 1980**

[54] **TRIM STRUCTURE FOR INTEGRATED CAPACITORS**

[75] Inventor: **Thomas P. Redfern**, San Jose, Calif.

[73] Assignee: **National Semiconductor Corporation**, Santa Clara, Calif.

[21] Appl. No.: **877,915**

[22] Filed: **Feb. 15, 1978**

[51] **Int. Cl.**[2] **H01L 27/00**

[52] **U.S. Cl.** ..... **357/51**; 219/121 LM; 361/271; 357/67

[58] **Field of Search** ..... 357/14, 23, 41, 51, 357/67; 29/574, 576 OC; 219/121 L, 121 LM; 361/271, 277, 278, 292, 402

[56] **References Cited**

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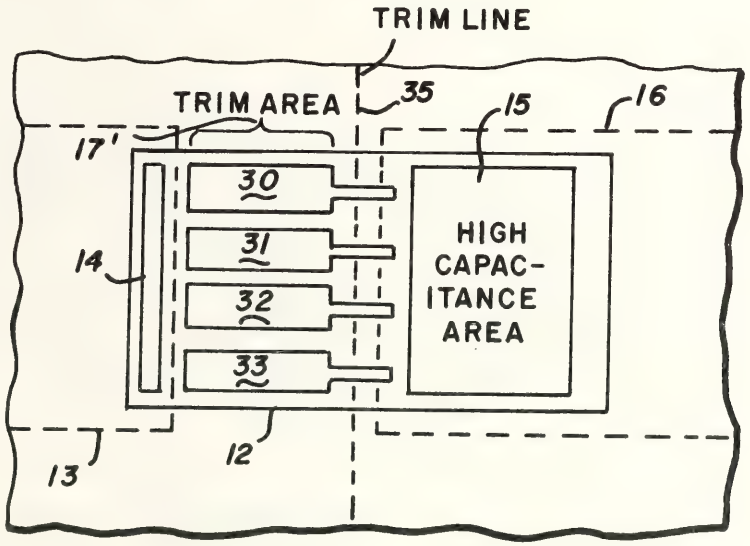
3,860,836	1/1975	Pedersen	357/51
3,890,631	6/1975	Tiemann	357/23
4,001,869	1/1977	Brown	357/14
4,016,483	4/1977	Rudin	357/51
4,017,885	4/1977	Kendall et al.	357/14

Primary Examiner—William D. Larkins
Attorney, Agent, or Firm—Gail W. Woodward

[57] **ABSTRACT**

A capacitor suitable for integration into a monolithic integrated circuit is fabricated in two parallel connected sections. One section, using a thin oxide, constitutes most of the capacitance. A second section fabricated on a thick oxide constitutes a smaller capacitance per unit area but can be laser trimmed to provide a precise capacitance without damage to the integrated circuit. The trimmable section is desirably made using a conductive electrode material that is readily removed with laser energy.

4 Claims, 4 Drawing Figures



United States Patent [19]
Culmer
[11] **4,198,580**
[45] **Apr. 15, 1980**

[54] **MOSFET SWITCHING DEVICE WITH CHARGE CANCELLATION**

[75] Inventor: **Daniel D. Culmer**, Sunnyvale, Calif.

[73] Assignee: **National Semiconductor Corporation**, Santa Clara, Calif.

[21] Appl. No.: **910,698**

[22] Filed: **May 30, 1978**

[51] **Int. Cl.**[2] **H03K 17/72**; H03K 17/16; H03K 17/66; H01L 29/78

[52] **U.S. Cl.** ..... **307/251**; 307/200 B; 307/304; 357/23; 357/41

[58] **Field of Search** ..... 307/200 B, 251, 304; 357/23, 41; 328/162

[56] **References Cited**

U.S. PATENT DOCUMENTS

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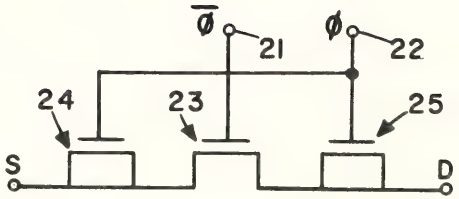
4,081,699	3/1978	Hirt et al.	307/251 X
4,130,766	12/1978	Patel et al.	307/200 B X

Primary Examiner—Larry N. Anagnos
Attorney, Agent, or Firm—Brown & Martin

[57] **ABSTRACT**

A MOSFET switching device, including first and second control terminals; a first MOSFET having its gate connected to the first control terminal; a second MOSFET having its gate connected to the second control terminal and its source and drain both connected to the source of the first MOSFET; and a third MOSFET having its gate connected to the second control terminal and its source and drain both connected to the drain of the first MOSFET. When complementary control signals are applied to the first and second control terminals, charge spikes occurring at the source and drain of the first MOSFET when the conduction state of the first MOSFET is changed are cancelled by charge spikes occurring simultaneously in the second and third MOSFET's.

3 Claims, 5 Drawing Figures



United States Patent [19]

Klein

[11] **4,205,330**

[45] **May 27, 1980**

[54] **METHOD OF MANUFACTURING A LOW VOLTAGE N-CHANNEL MOSFET DEVICE**

[75] Inventor: **Thomas Klein**, Saratoga, Calif.

[73] Assignee: **National Semiconductor Corp.**, Santa Clara, Calif.

[21] Appl. No.: **896,658**

[22] Filed: **Apr. 17, 1978**

Related U.S. Application Data

[62] Division of Ser. No. 783,914, Apr. 1, 1977, Pat. No. 4,104,784.

[51] **Int. Cl.**[2] **H01L 29/78**; H01L 27/02

[52] **U.S. Cl.** **357/23**; 357/41; 357/42

[58] **Field of Search** 357/23, 41, 42

[56] **References Cited**

U.S. PATENT DOCUMENTS

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3,748,545	7/1973	Beale	357/42
3,920,481	11/1975	Hu	357/42
3,983,572	9/1976	Johnson	357/42
4,003,071	1/1977	Takagi	357/42
4,006,491	2/1977	Alaspa et al.	357/23
4,052,229	10/1977	Pashley	357/42
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4,085,498	4/1978	Rideout	357/42

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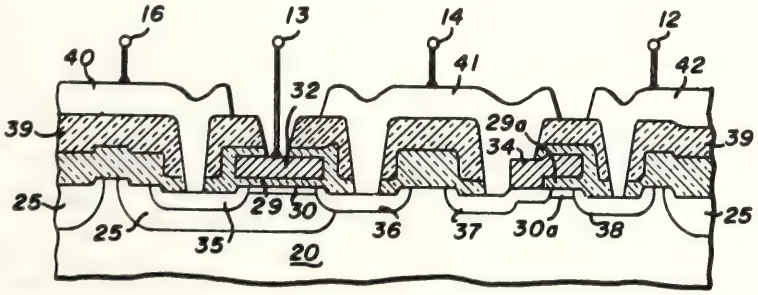
Getting the Most Out of C-MOS Devices for Analog Switching Jobs, by Thibodeaux; Electronics, Dec. 25, 1975, pp. 69–74.

Primary Examiner—Andrew J. James

[57] **ABSTRACT**

A novel MOSFET circuit and method of manufacture utilizing a double ion implant process for manufacturing a low voltage high performance n-channel device that includes an enhancement transistor inverter combined with a depletion transistor load. The process starts with high resistivity material and uses a first ion implant process to dope the field region and to give the required threshold voltage for an enhancement device. A second ion implant is used to dope the channel region for the depletion device.

8 Claims, 11 Drawing Figures



United States Patent [19]

Huang

[11] **4,219,797**

[45] **Aug. 26, 1980**

[54] **INTEGRATED CIRCUIT RESISTANCE LADDER HAVING CURVILINEAR CONNECTING SEGMENTS**

[75] Inventor: **Jen-yen Huang**, San Jose, Calif.

[73] Assignee: **National Semiconductor Corporation**, Santa Clara, Calif.

[21] Appl. No.: **21,484**

[22] Filed: **Mar. 19, 1979**

[51] **Int. Cl.**[2] **H01C 7/00**

[52] **U.S. Cl.** **338/333**; 338/308; 338/325; 357/51

[58] **Field of Search** ..... 338/307–309, 338/322, 323, 325, 326, 333, 334; 357/51; 323/94 R; 29/610, 589

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,460,026	8/1969	Dow et al.	338/305 X
3,617,959	11/1971	Cicero	323/94 R X
3,644,802	2/1972	Dingwall	357/51
3,922,707	11/1975	Freed et al.	357/51 X
4,116,102	9/1978	Tsunoo et al.	357/51 X

Primary Examiner—C. L. Albritton

Attorney, Agent, or Firm—Brown & Martin

[57] **ABSTRACT**

A resistance ladder having a plurality of resistance branches in an integrated circuit chip, including a layer of resistive material defining a plurality of discrete linear segments and a plurality of connector tabs extending from each of the linear segments at predetermined intervals for defining each resistance branch: wherein the layer of resistive material further defines a number of curvilinear segments for connecting the linear segments to provide a continuous resistive material layer for defining said resistance ladder. Each curvilinear segment is approximately a segment of a circle. The resistive material layer also defines a plurality of connector tabs extending from each curvilinear segment; with the angular separation of the tabs being approximately defined by

$$\theta=(R/\rho)\ln(r_2/r_1),$$

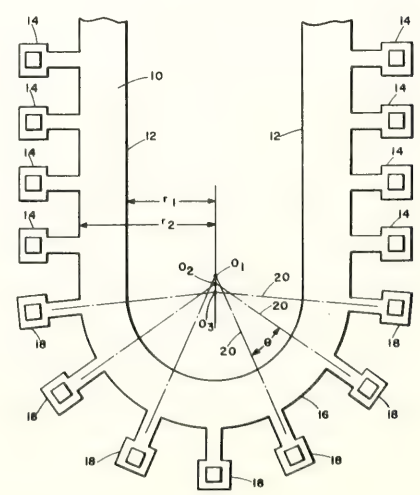
wherein R is the resistance required for each leg of the resistance ladder;

ρ is the sheet resistance of the resistive material;

r_1 is the inner radius of said circle; and

r_2 is the outer radius of said circle.

6 Claims, 1 Drawing Figure



United States Patent [19]
Dobkin
[11] **4,225,878**
[45] **Sep. 30, 1980**

[54] **INTEGRATED CIRCUIT ON CHIP TRIMMING**

[75] Inventor: **Robert C. Dobkin**, Hillsborough, Calif.

[73] Assignee: **National Semiconductor Corporation**, Santa Clara, Calif.

[21] Appl. No.: **18,815**

[22] Filed: **Mar. 8, 1979**

[51] **Int. Cl.**[2] **H01L 27/10**
[52] **U.S. Cl.** **357/51**; 357/13; 357/45; 357/86
[58] **Field of Search** 357/51, 13, 45, 76, 357/86, 40

[56] **References Cited**

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3,848,238	11/1974	Rizzi et al.	357/51
4,016,483	4/1977	Rudin	357/51

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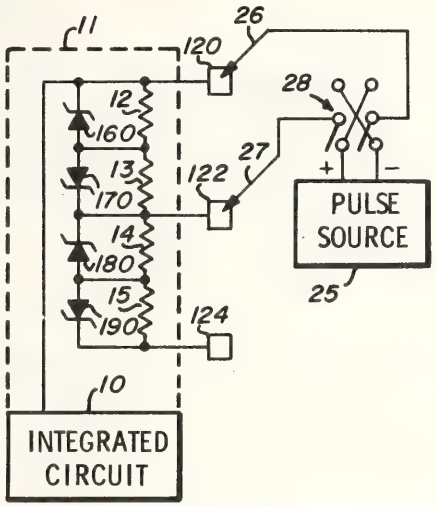
Erdi, "Precision Trim . . . ", IEEE Int. Solid State Circuits Conf. Tech. Digest, Feb. 1975, pp. 192–193.

Primary Examiner—William D. Larkins
Attorney, Agent, or Firm—Gail W. Woodward; James A. Sheridan; Michael L. Sherrard

[57] **ABSTRACT**

In a monolithic integrated circuit, on-chip trimming is implemented by connecting a zener diode across each element of a plural element trimmable resistor. Adjacent diodes are connected back to back and a pair of conventional bonding pads connected thereto. In trimming, when it is desired to short out one of the trimmable elements, the associated diode is subjected to an overload pulse by means of test probes applied to the bonding pads. Since the diodes are connected back to back, the pulse polarity will determine which diode is overloaded in the reverse bias condition. Thus, the trimmable element to be shorted is determined by pulse polarity and only one bonding pad is needed for each pair of trimmable elements.

8 Claims, 4 Drawing Figures



United States Patent [19]
Copeland, III
[11] **4,189,739**
[45] **Feb. 19, 1980**

[54] **SEMICONDUCTOR OVERLOAD PROTECTION STRUCTURE**

[75] Inventor: **John A. Copeland, III**, Fair Haven, N.J.

[73] Assignee: **Bell Telephone Laboratories, Incorporated**, Murray Hill, N.J.

[21] Appl. No.: **884,414**

[22] Filed: **Mar. 8, 1978**

[51] **Int. Cl.**[2] **H01L 27/02**
[52] **U.S. Cl.** **357/51**; 357/13; 357/23; 357/41
[58] **Field of Search** 357/13, 23, 41, 51

[56] **References Cited**

U.S. PATENT DOCUMENTS

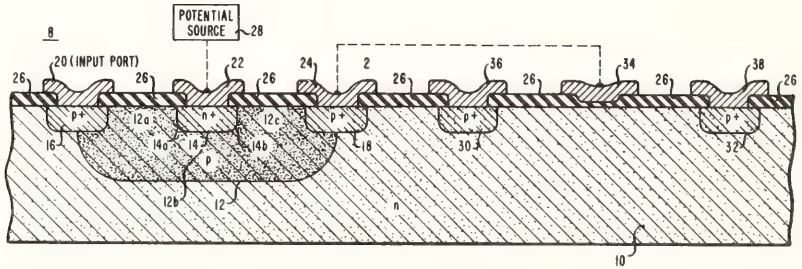
3,967,295	6/1976	Stewart	357/42

Primary Examiner—Edward J. Wojciechowicz
Attorney, Agent, or Firm—Irwin Ostroff

[57] **ABSTRACT**

An input voltage overload protection semiconductor structure useful with MOS circuitry consists of a p-region in an n-substrate with p+ type regions formed on both sides of the p-region and an n+ type region centrally located in the p-region. Input signals are applied to the first p+ region. The gate of an MOS structure to be protected from voltage overload is connected to the second p+ type region. A power supply used with the MOS structure is connected to the n+ region. This structure provides significantly greater load protection than the standard resistor-diode-resistor circuit.

4 Claims, 2 Drawing Figures



United States Patent [19]
Agraz-Guerena et al.
[11] **4,199,775**
[45] **Apr. 22, 1980**

[54] **INTEGRATED CIRCUIT AND METHOD FOR FABRICATION THEREOF**

[75] Inventors: **Jorge Agraz-Guerena**, Puebla, Mexico; **Alan W. Fulton**, Batavia, Ill.

[73] Assignee: **Bell Telephone Laboratories, Incorporated**, Murray Hill, N.J.

[21] Appl. No.: **502,674**

[22] Filed: **Sep. 3, 1974**

[51] **Int. Cl.**[2] **H01L 27/10**
[52] **U.S. Cl.** **357/46**; 357/15; 357/44; 357/48; 357/89; 357/92
[58] **Field of Search** ..... 357/91, 15, 36, 44, 357/46, 48; 307/317 A, 213, 214, 215, 303

[56] **References Cited**

U.S. PATENT DOCUMENTS

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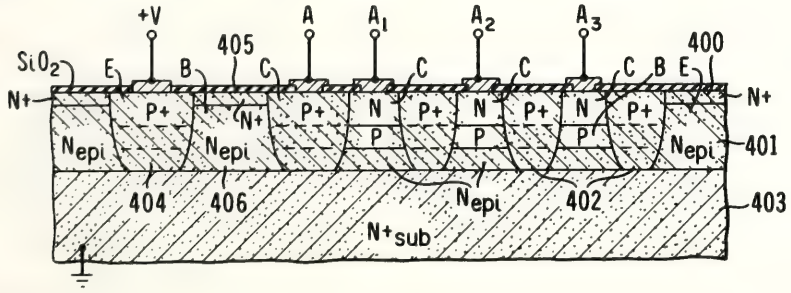
Berger, "Bipolar Devices for Low Power Digital Applications . . .", *Solid State Devices 1973*, (The Institute of Physics, London) (Proc. 3rd European Solid State Device Research Conference, Munich, Sep. 18–21, 1973), pp. 118–123.

Primary Examiner—William D. Larkins
Attorney, Agent, or Firm—John C. Albrecht; Arthur J. Torsiglieri

[57] **ABSTRACT**

An integrated transistor circuit arrangement provides a multicollector transistor with Schottky diodes and ohmic connections selectively formed at the collector terminals. In the illustrative example, a vertical transistor is formed in an N-type epitaxial layer overlying an N+ substrate. A through-extending region of P+ material encircles the region of the epitaxial layer in which the vertical transistor is formed. The base of the vertical transistor is formed by the implanting of P-type impurity in a location spaced apart from the surfaces of the epitaxial layer. The resulting base has a symmetrical profile relative to the faces of the epitaxial layer. Therefore, the transistor may be operated with the collector at the surface without penalty of electrical operation. In the illustrative example, a PNP lateral transistor is utilized as a current source for the vertical transistor.

22 Claims, 9 Drawing Figures



United States Patent [19]
Fraser, Jr. et al.
[11] **4,210,950**
[45] **Jul. 1, 1980**

[54] **HIGH-RATIO-ACCURACY CAPACITOR GEOMETRIES FOR INTEGRATED CIRCUITS**

[75] Inventors: **Donald L. Fraser, Jr.**, Warren Township, Somerset County; **Michael F. Tompsett**, New Providence, both of N.J.

[73] Assignee: **Bell Telephone Laboratories, Incorporated**, Murray Hill, N.J.

[21] Appl. No.: **947,020**

[22] Filed: **Sep. 29, 1978**

[51] **Int. Cl.**[2] **H01G 4/38**
[52] **U.S. Cl.** **361/329**; 357/51; 361/303
[58] **Field of Search** 361/328, 329, 303, 271, 361/306

[56] **References Cited**

U.S. PATENT DOCUMENTS

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2,694,185	11/1954	Kodama	361/329 X
3,273,033	9/1966	Rossmeisl	361/329 X
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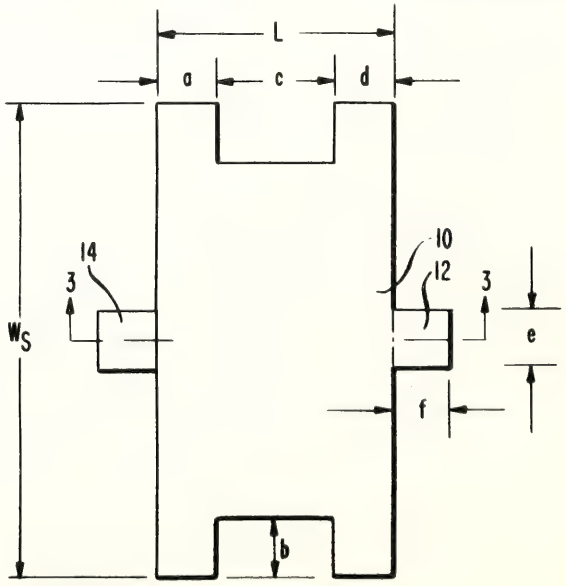
"Analog Sample Data Filters", pp. 302–304, IEEE Journal Solid State Circuits, vol. SC7 #4, 8/72.

Primary Examiner—E. A. Goldberg
Attorney, Agent, or Firm—Lucian C. Canepa

[57] **ABSTRACT**

A number of known circuit configurations require high-ratio-accuracy capacitors. Maintaining such ratios during the various processing steps involved in fabricating the configurations in integrated-circuit form has been found to be difficult. In accordance with this invention, ratio capacitors are made in integrated-circuit form utilizing a unique geometry. In one specific embodiment, a so-called H-section geometry that is largely insensitive to processing variations is utilized to form the capacitors. In this way, high-yield low-parasitic precisely matched pairs of ratio capacitors are achieved.

8 Claims, 4 Drawing Figures



United States Patent [19]

Clemens et al.

[11] **4,216,489**

[45] **Aug. 5, 1980**

[54] **MOS DYNAMIC MEMORY IN A DIFFUSION CURRENT LIMITED SEMICONDUCTOR STRUCTURE**

[75] Inventors: **James T. Clemens**, Allentown; **Dinesh A. Mehta**, Bethlehem; **James T. Nelson**, Coopersburg; **Charles W. Pearce**, Emmaus; **Robert C. Sun**, Whitehall, all of Pa.

[73] Assignees: **Bell Telephone Laboratories, Incorporated; Western Electric Co., Inc.**, both of New York, N.Y.

[21] Appl. No.: **5,639**

[22] Filed: **Jan. 22, 1979**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 848,000, Nov. 3, 1977, abandoned.

[51] **Int. Cl.**[2] **H01L 27/02**

[52] **U.S. Cl.** **357/41**; 357/23; 357/41; 357/51; 357/89; 357/90

[58] **Field of Search** 357/23, 41, 46, 51, 357/89, 90

[56] **References Cited**

U.S. PATENT DOCUMENTS

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3,997,368	12/1976	Petroff et al.	357/23
4,007,478	2/1977	Yagi	357/23
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FOREIGN PATENT DOCUMENTS

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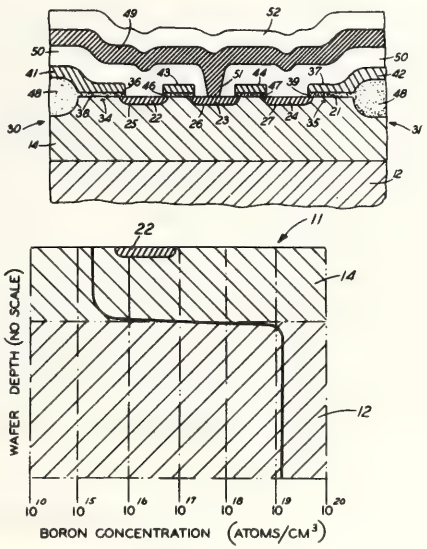
7831052	of 0000	France	357/23

Primary Examiner—Edward J. Wojciechowicz
Attorney, Agent, or Firm—W. O. Schellin; A. J. Torsiglieri

[57] **ABSTRACT**

In a dynamic MOS (Metal Oxide Semiconductor) random access memory, reverse bias leakage currents which deplete stored charges are reduced by minimizing minority carrier generation-type currents. By so minimizing these currents, the leakage currents become dominated by minority carrier diffusion currents. The memory is ideally formed in an upper semiconductor layer (14) of a layered structure (11). The semiconductor layer (14) is grown epitaxially with a relatively low dopant concentration on a semiconductor substrate (12) with a dopant concentration of the same conductivity type and about three orders of magnitude greater than that of the epitaxially grown layer. The epitaxially grown structure is advantageously suited for the memory circuits in that it may be formed with very low leakage currents. The material further offers by its layered structure a basis for optimizing dynamic memory device characteristics.

10 Claims, 6 Drawing Figures



United States Patent [19]

Nicolay

[11] **4,198,744**

[45] **Apr. 22, 1980**

[54] **PROCESS FOR FABRICATION OF FUSE AND INTERCONNECTS**

[75] Inventor: **Hugh C. Nicolay**, Melbourne Village, Fla.

[73] Assignee: **Harris Corporation**, Melbourne, Fla.

[21] Appl. No.: **934,150**

[22] Filed: **Aug. 16, 1978**

[51] **Int. Cl.**[2] **H01H 69/2**

[52] **U.S. Cl.** **29/623**; 29/578; 357/51

[58] **Field of Search** 29/623, 620, 578; 357/51, 67

[56] **References Cited**

U.S. PATENT DOCUMENTS

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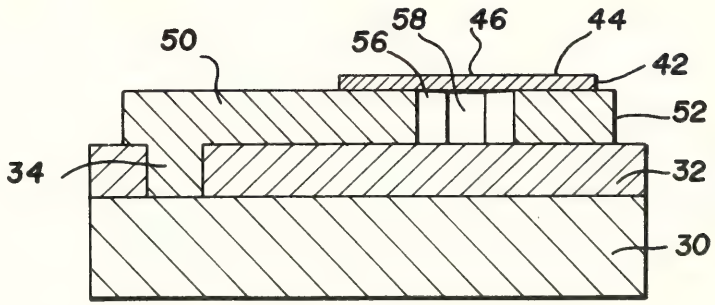
3,996,551	12/1976	Croson	29/620
4,032,949	6/1977	Bierig	357/51
4,135,295	1/1979	Price	29/623

Primary Examiner—Francis S. Husar
Assistant Examiner—Gene P. Crosby
Attorney, Agent, or Firm—Leitner, Palan, Martin & Bernstein

[57] **ABSTRACT**

Fuses and interconnects are fabricated by applying a metallic layer on a substrate and a fusible layer on the metallic layer. Portions of the fusible layer are removed to define discrete fuse elements having a necked portion. Portions of the metallic layer are removed to define interconnects. A portion of the metallic layer coextensive with the necked portion of the fuse elements is removed by selective side etching to form tapering portions separated by a gap without etching of the interconnects. The interconnects are protected from side etching by a separate mask layer or a mask layer used to form the interconnects may be heated to flow down over the sides of the interconnects.

9 Claims, 9 Drawing Figures



United States Patent [19]

Morcom et al.

[11] **4,210,925**

[45] **Jul. 1, 1980**

[54] **I²L INTEGRATED CIRCUIT AND PROCESS OF FABRICATION**

[75] Inventors: **William R. Morcom**, Melbourne Beach; **Hugh C. Nicolay**, Melbourne Village; **Eugene R. Cox**, Palm Bay, all of Fla.

[73] Assignee: **Harris Corporation**, Melbourne, Fla.

[21] Appl. No.: **875,824**

[22] Filed: **Feb. 7, 1978**

[51] **Int. Cl.**² **H01L 27/02**

[52] **U.S. Cl.** **357/46**; 357/49; 357/55; 357/92

[58] **Field of Search** 357/92, 46, 49, 55

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,993,513	11/1976	O'Brien	357/92
4,082,571	4/1978	Graul et al.	357/92
4,140,559	2/1979	Van Vonno	357/92

Primary Examiner—Edward J. Wojciechowicz
Attorney, Agent, or Firm—Leitner, Palan, Lyman, Martin & Bernstein

[57] **ABSTRACT**

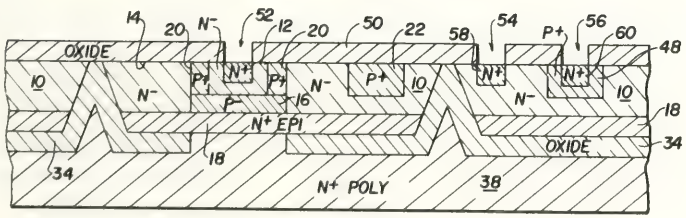
In a complementary pair of bipolar transistors, one vertical and one lateral, the vertical transistor includes a heavily doped buried emitter, lightly doped buried graded base and a heavily doped surface collector and the lateral transistor includes a lightly doped substrate base and heavily doped emitter and collector. The lateral transistor's collector isolates the lateral transistor's base from the vertical transistor's collector.

This integrated circuit approach includes the I²L structure of the present invention and T²L devices. The I²L transistors are in dielectrically isolated regions with the vertical transistors emitter being connected to the polycrystalline support through a vertical opening in the dielectric isolation.

The process of fabrication includes forming the vertical transistor's base by diffusion into a first surface of a substrate of opposite conductivity type, forming the vertical transistor's emitter epitaxially on the first surface and forming the vertical transistor's collector and the lateral transistor's emitter and collector by diffusion into the opposite surface of the substrate. The lateral transistor's collector diffusion is from the opposite surface down to the vertical transistor's base and separates the vertical transistor 's collector from the portion of the substrate which is the lateral transistor's base.

For integrated circuits, the process includes dividing the substrate into a plurality of dielectrically insulated regions after forming the epitaxial emitter and depositing a polycrystalline support.

18 Claims, 8 Drawing Figures



United States Patent [19]

Gasner et al.

[11] **4,223,334**

[45] **Sep. 16, 1980**

[54] **HIGH VOLTAGE CMOS WITH LOCAL OXIDATION FOR SELF-ALIGNED GUARD RINGS AND PROCESS OF FABRICATION**

[75] Inventors: **John T. Gasner**, Melbourne; **Anthony L. Rivoli**, Palm Bay, both of Fla.

[73] Assignee: **Harris Corporation**, Melbourne, Fla.

[21] Appl. No.: **937,697**

[22] Filed: **Aug. 29, 1978**

Related U.S. Application Data

[62] Division of Ser. No. 835,263, Sep. 21, 1977.

[51] **Int. Cl.**² **H01L 27/02**

[52] **U.S. Cl.** **357/42**; 357/48; 357/52; 357/50

[58] **Field of Search** 357/42, 48, 52, 50

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,967,295	6/1976	Stewart	357/51
3,983,620	10/1976	Spadea	29/571
4,052,229	10/1977	Pashley	148/1.5

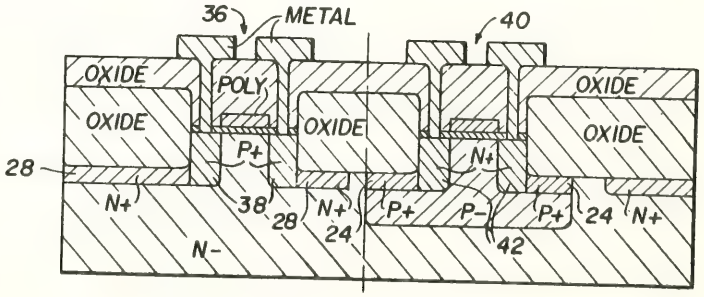
Primary Examiner—Martin H. Edlow
Attorney, Agent, or Firm—Leitner, Palan, Lyman, Martin & Bernstein

[57] **ABSTRACT**

Complementary MOS devices having spaced guard rings are fabricated by applying an oxide layer to an N substrate with an opening for doping P-type impurities to form a well, applying a nitride layer over a portion of the oxide and of the well portions, doping the area in the well between the nitride and the oxide to form P-type guard rings, masking the well and adjacent portion of the oxide, doping the area between the mask and the exposed nitride layer to form N-type guard rings and exposing the substrate to an oxidizing atmosphere to oxidize the substrate except where covered by the nitride layer. The nitride layer is removed and standard device processing is used to form complementary MOS in the areas previously covered by the nitride.

The resulting integrated circuit includes a P-type guard ring extending laterally from the outer edge of the N-channel source and drain to the edge of the P-type well and a N-type guard ring extending laterally from the outer edge of the P-channel device source and drain to a point adjacent, but spaced from the P-type well. The inner lateral edges of the guard rings are laterally aligned with the outer edges of the source and drains and the top surface of the guard rings are vertically displaced from the top surface of the source and drains by the oxide formed in the substrate.

2 Claims, 6 Drawing Figures



United States Patent [19]

Taylor

[11] **4,231,056**

[45] **Oct. 28, 1980**

[54] **MOAT RESISTOR RAM CELL**

[75] Inventor: **David L. Taylor**, Melbourne, Fla.

[73] Assignee: **Harris Corporation**, Melbourne, Fla.

[21] Appl. No.: **953,137**

[22] Filed: **Oct. 20, 1978**

[51] **Int. Cl.**[2] **H01L 27/04**; H01L 27/12; H01L 27/02

[52] **U.S. Cl.** **357/50**; 357/49; 357/51; 357/59; 357/55; 357/23

[58] **Field of Search** 357/55, 59, 23, 91, 357/49, 51, 50

[56] **References Cited**

U.S. PATENT DOCUMENTS

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3,956,033	5/1976	Roberson	357/59
3,998,673	12/1976	Chow	357/59
4,037,306	7/1977	Gutteridge	357/55
4,048,649	9/1977	Bohn	357/59
4,085,499	4/1978	Kuninobu	357/59
4,110,776	8/1978	Rao et al.	357/59
4,149,177	4/1979	Alter	357/55
4,157,269	6/1979	Ning et al.	357/59

Primary Examiner—Andrew J. James

Attorney, Agent, or Firm—Leitner, Palan, Lyman, Martin & Bernstein

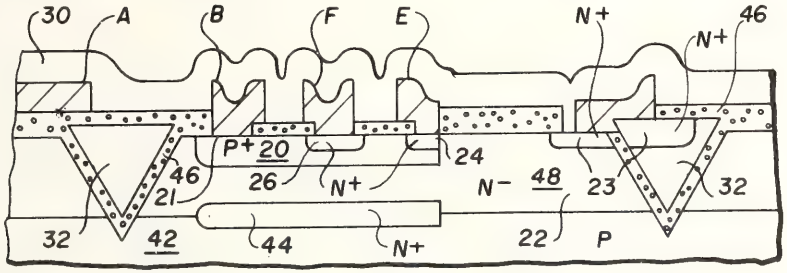
[57] **ABSTRACT**

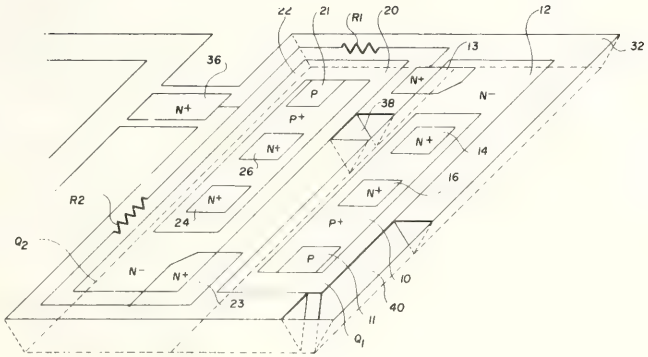
A RAM cell having a pair of transistors formed in two adjacent wells laterally separated from each other and surrounded laterally by a common doped polycrystalline semiconductor moat. Dielectrical insulation separate the wells from the moat. The moat is discontinuous, forming thereby a pair of resistors connected together at one end and disconnected at the discontinuity. Surface contacts bridge adjacent areas of the well and the moat which are of the same conductivity type whereby the moat forms the load resistor for the transistor. Each transistor includes a second emitter.

First level interconnects include a first interconnect interconnecting an emitter from each transistor, a second interconnect parallel to the first contacting the connected end of the moat resistors, a pair of interconnects each interconnecting the bridge contact of one transistor to the base of the other, and a pair of contacts for the other emitter regions. Second level interconnects include a pair of parallel interconnects connected to a respective emitter contact and orthogonal to the first interconnect.

A method of fabrication is also described.

17 Claims, 5 Drawing Figures





United States Patent [19]

Nonaka et al.

[11] **4,200,879**

[45] **Apr. 29, 1980**

[54] **INTEGRATED SEMICONDUCTOR DEVICE INCLUDING STATIC INDUCTION TRANSISTOR**

[75] Inventors: **Terumoto Nonaka; Tadahiko Hotta; Shin Yamashita**, all of Hamamatsu, Japan

[73] Assignee: **Nippon Gakki Seizo Kabushiki Kaisha**, Hamamatsu, Japan

[21] Appl. No.: **954,917**

[22] Filed: **Oct. 26, 1978**

[30] **Foreign Application Priority Data**

Nov. 5, 1977 [JP] Japan 52/132756

[51] **Int. Cl.**[2] **H01L 27/04**

[52] **U.S. Cl.** **357/43**; 357/20; 357/22; 357/46; 357/92

[58] **Field of Search** 357/22, 20, 43, 46, 357/92

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,295,030	12/1966	Allison	357/22
3,453,507	7/1969	Archer	307/311
3,721,839	3/1973	Shannon	357/30
3,947,707	3/1976	Shannon et al.	357/22

FOREIGN PATENT DOCUMENTS

2730373	1/1978	Fed. Rep. of Germany	357/92

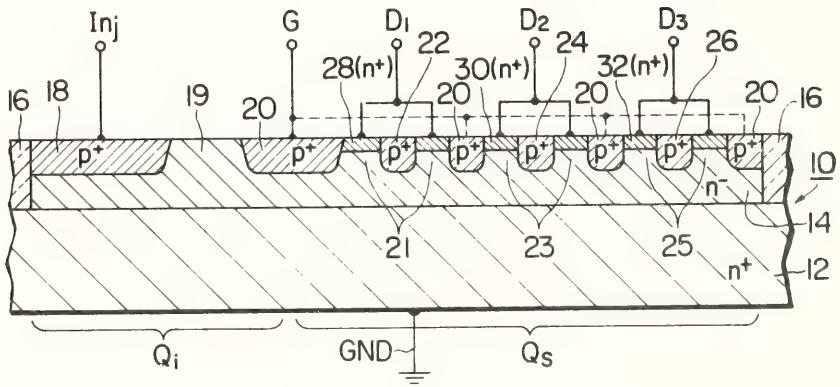
Primary Examiner—William D. Larkins

Attorney, Agent, or Firm—Cushman, Darby & Cushman

[57] **ABSTRACT**

In an integrated semiconductor device of the IIL type which includes a switching transistor and an injector transistor for supplying carriers to drive the switching transistor, the switching transistor is a static induction transistor which comprises: cylindrical current channels for providing current paths between a source and drains; a control gate surrounding the outer boundaries of the channels to form pn junctions therebetween and being injected with carriers from the injector transistor to control the current flow in the channels; and floating gates disposed inside the respective channels to form pn junctions therebetween. The floating gates are electrically floating and have a potential affected by the potential of the control gate to contribute to the channel conduction controlling action together with the control gate.

6 Claims, 3 Drawing Figures



United States Patent [19]

Nonaka et al.

[11] **4,205,334**

[45] **May 27, 1980**

[54] **INTEGRATED SEMICONDUCTOR DEVICE**

[75] Inventors: **Terumoto Nonaka; Tadahiko Hotta; Shin Yamashita**, all of Hamamatsu, Japan

[73] Assignee: **Nippon Gakki Seizo Kabushiki Kaisha**, Hamamatsu, Japan

[21] Appl. No.: **925,624**

[22] Filed: **Jul. 17, 1978**

[30] **Foreign Application Priority Data**

Jul. 27, 1977 [JP] Japan 52-90146

[51] **Int. Cl.**[2] **H01L 27/02**

[52] **U.S. Cl.** **357/41**; 357/22; 357/50; 357/55

[58] **Field of Search** 357/41, 22, 50, 55

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,117,587 10/1978 Kano et al. 357/41

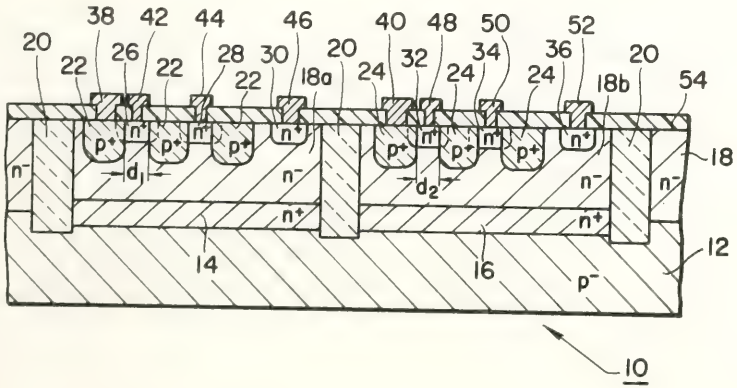
Primary Examiner—Edward J. Wojciechowicz

Attorney, Agent, or Firm—Cushman, Darby & Cushman

[57] **ABSTRACT**

An integrated semiconductor device including at least one first vertical-type junction field effect transistor (vertical JFET) having a triode-like unsaturated voltage-current characteristic and at least one second vertical JFET having a bipolar-transistor-like saturated voltage-current characteristic, both being integrally formed in a semiconductor body. Both the first and second vertical JFET are much similar in general arrangement to each other, thus allowing simultaneous forming thereof by the same manufacturing process, without sacrificing the good characteristics of these two types of transistors.

6 Claims, 4 Drawing Figures



United States Patent [19]

Nonaka

[11] **4,209,795**

[45] **Jun. 24, 1980**

[54] **JSIT-TYPE FIELD EFFECT TRANSISTOR WITH DEEP LEVEL CHANNEL DOPING**

[75] Inventor: **Terumoto Nonaka**, Hamamatsu, Japan

[73] Assignee: **Nippon Gakki Seizo Kabushiki Kaisha**, Hamamatsu, Japan

[21] Appl. No.: **854,040**

[22] Filed: **Nov. 22, 1977**

[30] **Foreign Application Priority Data**

Dec. 6, 1976 [JP] Japan 51-146251

[51] **Int. Cl.**[2] **H01L 29/80**

[52] **U.S. Cl.** **357/22**; 357/21; 357/43; 357/64; 357/92

[58] **Field of Search** 357/21, 22, 64, 43, 357/92

[56] **References Cited**

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1390034	4/1975	United Kingdom	357/43

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"Junction Field-Effect Transistor Designed for Speedy Logic," Electronics, Aug. 19, 1976, vol. 49, #7, International Edition, pp. 4E, 6E.

J. Porter, "JFET-Transistor Yields Device with Negative Resistance," IEEE Trans. on Elec. Dev., Sep. 1976, pp. 1098-1099.

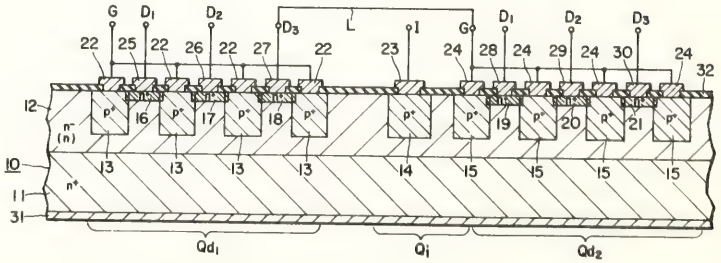
Primary Examiner—Joseph E. Clawson, Jr.

Attorney, Agent, or Firm—Cushman, Darby & Cushman

[57] **ABSTRACT**

A field effect transistor of the type wherein the conductivity of the channel thereof is variable by injecting the minority carriers into the channel from the gate thereof, is disclosed. The channel of the transistor includes minority carrier recombination centers in such an amount that the lifetime of the minority carriers in the channel may be shortened so as to sufficiently reduce the minority carrier storage effect in the channel. The recombination centers may comprise elements such as gold doped in the channel region. This field effect transistor is hardly subject to the minority carrier storage effect and is capable of effecting a turn-off action at a markedly high speed.

17 Claims, 3 Drawing Figures



United States Patent [19]

Nishizawa et al.

[11] **4,216,038**

[45] **Aug. 5, 1980**

[54] **SEMICONDUCTOR DEVICE AND MANUFACTURING PROCESS THEREOF**

[75] Inventors: **Jun-ichi Nishizawa**, Sendai; **Yasunori Mochida**, Hamamatsu; **Terumoto Nonaka**, Hamamatsu; **Tadahiko Hotta**, Hamamatsu; **Shin Yamashita**, Hamamatsu, all of Japan

[73] Assignee: **Nippon Gakki Seizo Kabushiki Kaisha**, Hamamatsu, Japan

[21] Appl. No.: **913,006**

[22] Filed: **Jun. 5, 1978**

[30] **Foreign Application Priority Data**

Jun. 11, 1977 [JP] Japan 52-69325

[51] **Int. Cl.**[2] **H01L 21/22**

[52] **U.S. Cl.** **148/187**; 148/188; 357/43

[58] **Field of Search** 148/187, 188; 357/43

[56] **References Cited**

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3,846,821	11/1974	Nagata et al.	148/187 X
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4,076,557	2/1978	Huang et al.	148/1.5

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Electronics (International Edition), Aug. 19, 1976, pp. 4E and 6E.

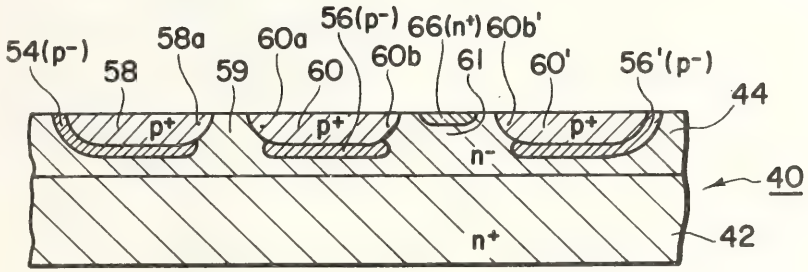
Primary Examiner—G. Ozaki

Attorney, Agent, or Firm—Cushman, Darby & Cushman

[57] **ABSTRACT**

In a semiconductor device of the type arranged so that the minority carriers are injected into a lightly-doped n type semiconductor layer from a heavily-doped p type semiconductor layer provided in the n type layer, that portion of the p type layer excluding a certain portion is separated from the n type layer by a separator layer to cause the p type layer to contact the n type layer only at the certain portion, whereby the carrier injection is restricted to occur within a limited region of the n type layer contacting the certain portion of the p type layer. The separator and the p type layer are formed, by relying on a self-alignment technique using a double-mask layer, as diffused regions partially overlapping each other with a good relative alignment in the n type layer.

11 Claims, 7 Drawing Figures



United States Patent [19]

Kant

[11] **4,191,964**

[45] **Mar. 4, 1980**

[54] **HEADLESS RESISTOR**

[75] Inventor: **Rajni Kant**, San Jose, Calif.

[73] Assignee: **Fairchild Camera & Instrument Corp.**, Mountain View, Calif.

[21] Appl. No.: **914,637**

[22] Filed: **Jun. 12, 1978**

Related U.S. Application Data

[63] Continuation of Ser. No. 760,593, Jan. 19, 1977, abandoned.

[51] **Int. Cl.**[2] **H01L 27/02**

[52] **U.S. Cl.** **357/51**; 357/15; 357/20

[58] **Field of Search** 357/15, 51, 20

[56] **References Cited**

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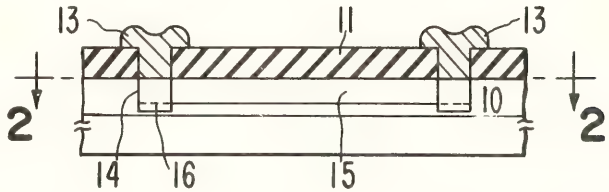
Primary Examiner—Joseph E. Clawson, Jr.

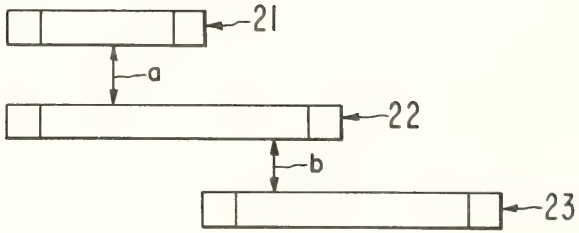
Attorney, Agent, or Firm—Alan H. MacPherson; Robert C. Colwell

[57] **ABSTRACT**

A diffused resistor included in a Schottky device formed in a planar semiconductor material comprises a resistor diffusion formed in the surface of the material and a contact diffusion formed in the surface of the material, the configuration of the contact diffusion being essentially coincident with the shape of the resistor at the location at which ohmic contact to the resistor diffusion is made.

5 Claims, 6 Drawing Figures





United States Patent [19]

Berry

[11] **4,197,143**

[45] **Apr. 8, 1980**

[54] **METHOD OF MAKING A JUNCTION FIELD-EFFECT TRANSISTOR UTILIZING A CONDUCTIVE BURIED REGION**

[75] Inventor: **Robert Berry**, Cupertino, Calif.

[73] Assignee: **Fairchild Camera & Instrument Corporation**, Mountain View, Calif.

[21] Appl. No.: **921,637**

[22] Filed: **Jul. 3, 1978**

Related U.S. Application Data

[62] Division of Ser. No. 720,467, Sep. 3, 1976, Pat. No. 4,118,728.

[51] **Int. Cl.**[2] **H01L 29/80**; H01L 21/263

[52] **U.S. Cl.** **148/1.5**; 148/187; 357/23; 357/41; 357/91

[58] **Field of Search** 148/1.5, 187; 357/23, 357/22, 91, 41

[56] **References Cited**

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4,118,728	10/1978	Berry	357/22

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Moline et al., "Self-Aligned . . . Chan. Stops . . . ", IEEE Trans., vol. ED20, 1973, 1129.

Primary Examiner—L. Dewayne Rutledge

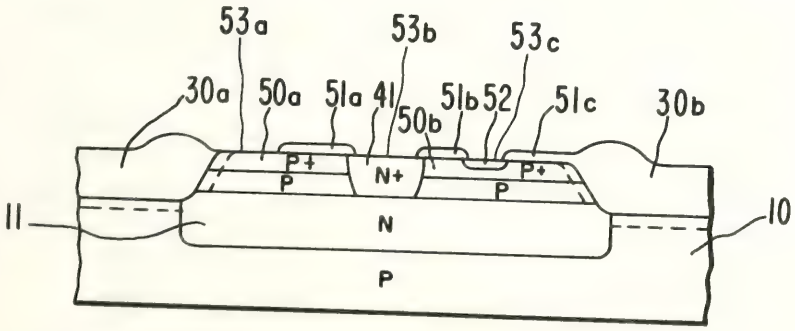
Assistant Examiner—Upendra Roy

Attorney, Agent, or Firm—Alan H. MacPherson; Robert C. Colwell

[57] **ABSTRACT**

In an oxide isolated semiconductor structure having an epitaxial layer formed on a monocrystalline substrate, a buried, laterally extending PN isolation junction in said structure, and oxidized isolation regions extending through said epitaxial layer to said PN isolation junction, thereby to form a plurality of electrically isolated pockets of semiconductor material, a dopant is located in those regions of the semiconductor material directly adjacent the oxidized isolation regions to prevent unwanted current flow called "channeling." The region formed by this dopant is often referred to as the field predeposition region. Typically, to form the field predeposition region, a selected dopant is placed in the exposed surface regions of the epitaxial semiconductor material just prior to the formation of the oxidized isolation regions. The field predeposition and oxidation of the epitaxial semiconductor material also cause the formation of a conductive buried region from that portion of the field predeposition dopant in the epitaxial pockets directly adjacent the oxidized semiconductor material. If desired, a collector sink then may be formed in the epitaxial pocket without disrupting the function of the conductive buried region. The conductive buried region may be utilized to facilitate manufacture of smaller memory circuits than heretofore available, compact junction field effect transistors, and other integrated circuit structures.

8 Claims, 18 Drawing Figures



United States Patent [19]

Berry

[11] **4,198,649**

[45] **Apr. 15, 1980**

[54] **MEMORY CELL STRUCTURE UTILIZING CONDUCTIVE BURIED REGIONS**

[75] Inventor: **Robert Berry**, Cupertino, Calif.

[73] Assignee: **Fairchild Camera and Instrument Corporation**, Mountain View, Calif.

[21] Appl. No.: **921,375**

[22] Filed: **Jul. 3, 1978**

Related U.S. Application Data

[62] Division of Ser. No. 720,467, Sep. 3, 1976, Pat. No. 4,118,728.

[51] **Int. Cl.**[2] **H01L 27/04**

[52] **U.S. Cl.** **357/50**; 357/49; 357/51; 357/22

[58] **Field of Search** 357/50, 49, 51, 22

[56] **References Cited**

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4,111,724	9/1978	Qgiue	148/175

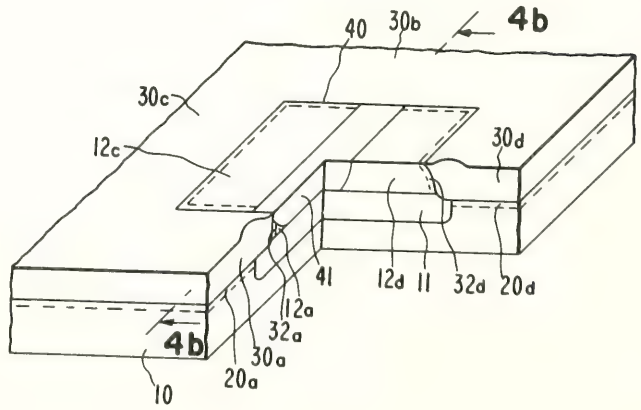
Primary Examiner—Martin H. Edlow

Attorney, Agent, or Firm—Alan MacPherson; Robert C. Colwell

[57] **ABSTRACT**

In an oxide isolated semiconductor structure having an epitaxial layer formed on a monocrystalline substrate, a buried, laterally extending PN isolation junction in said structure, and oxidized isolation regions extending through said epitaxial layer to said PN isolation junction, thereby to form a plurality of electrically isolated pockets of semiconductor material, a dopant is located in those regions of the semiconductor material directly adjacent the oxidized isolation regions to prevent unwanted current flow called "channeling." The region formed by this dopant is often referred to as the field predeposition region. Typically, to form the field predeposition region, a selected dopant is placed in the exposed surface regions of the epitaxial semiconductor material just prior to the formation of the oxidized isolation regions. The field predeposition and oxidation of the epitaxial semiconductor material also cause the formation of a conductive buried region from that portion of the field predeposition dopant in the epitaxial pockets directly adjacent the oxidized semiconductor material. If desired, a collector sink then may be formed in the epitaxial pocket without disrupting the function of the conductive buried region. The conductive buried region may be utilized to facilitate manufacture of smaller memory circuits than heretofore available, compact junction field effect transistors, and other integrated circuit structures.

12 Claims, 18 Drawing Figures



United States Patent [19]
Powell
[11] **4,190,849**
[45] **Feb. 26, 1980**

[54] **ELECTRONIC-BEAM PROGRAMMABLE SEMICONDUCTOR DEVICE STRUCTURE**

[75] Inventor: **Michael W. Powell**, Mesa, Ariz.
[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **834,081**
[22] Filed: **Sep. 19, 1977**
[51] **Int. Cl.**[2] **H01L 29/78**; H01L 29/34; H01L 27/10; G11C 11/40
[52] **U.S. Cl.** **357/23**; 357/29; 357/45; 357/54; 357/59; 365/185
[58] **Field of Search** 357/23, 45, 54, 29; 365/185, 128, 217, 237

[56] **References Cited**

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3,721,962	3/1973	Foster et al.	365/217
3,736,571	5/1973	Cohen et al.	357/29
3,825,946	7/1974	Frohman-Bentchkowsky	357/54
3,886,530	5/1975	Huber et al.	357/29
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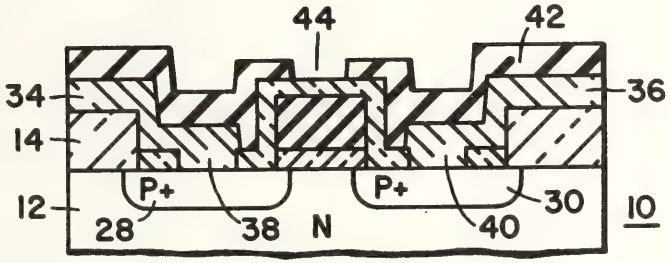
Thornton, *Scanning Electron Microscopy*, Chapman & Hall, London, (1968), pp. 111–114.

Primary Examiner—William D. Larkins
Assistant Examiner—Gene M. Munson
Attorney, Agent, or Firm—John A. Fisher

[57] **ABSTRACT**

A semiconductor device structure is provided in which an electrically isolated or "floating" conductor is adapted to receive electric charge from an electron beam. The resultant stored charge provides the basis for useful electronic functions such as floating gate MOS read-only-memories.

1 Claim, 9 Drawing Figures



United States Patent [19]
Farrell et al.
[11] **4,199,380**
[45] **Apr. 22, 1980**

[54] **INTEGRATED CIRCUIT METHOD**

[75] Inventors: **Michael G. Farrell**, Phoenix; **Sal T. Mastroianni**, Mesa, both of Ariz.
[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **960,143**
[22] Filed: **Nov. 13, 1978**
[51] **Int. Cl.**[2] **H01L 21/26**
[52] **U.S. Cl.** **148/1.5**; 148/187; 148/175; 357/34
[58] **Field of Search** 148/1.5, 187, 175; 357/34

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,060,427	11/1977	Barile et al.	148/1.5
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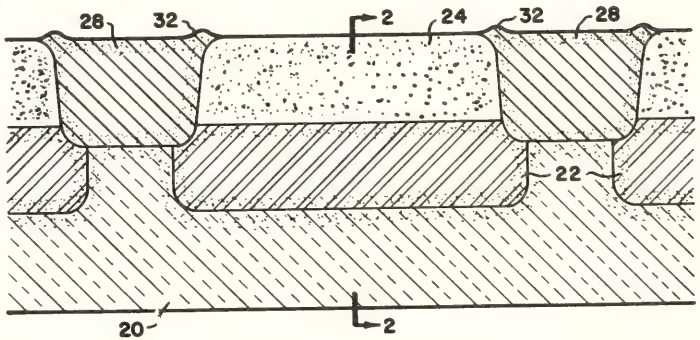
4,155,777	5/1979	Dunkley et al.	148/1.5
4,155,778	5/1979	Antipav	148/1.5

Primary Examiner—G. Ozaki
Attorney, Agent, or Firm—John A. Fisher

[57] **ABSTRACT**

A method for fabricating self-aligned, walled emitter, oxide isolated integrated circuits. A layer of oxidation resistant material is formed on an oxide isolated epitaxial layer on a silicon substrate. A pattern of apertures is opened in the oxidation resistant layer to expose portions of the epitaxial layer. The apertures extend across the oxide isolated silicon material and define the spaces between the contacts of the active devices of the circuit. Dopant impurities are applied through these apertures to form an inactive base region. The substrate is heated in an oxidizing ambient to form a relatively thick oxide on a portion of the epitaxial layer exposed through the apertures. The oxidation resistant layer is again selectively etched to expose those portions of the epitaxial layer where the active device regions are to be formed. In this step a single mask is used to open a plurality of device regions. The mask is used in conjunction with the oxide isolation and the relatively thick oxide to precisely define the spacing between these regions. Dopant impurities are applied through selected openings to form the active base region. Opposite type dopant impurities are applied through the same openings to form the emitter regions. Dopant impurities are also applied through further selected openings to form base contact areas and collector contact areas. The integrated circuit device thus formed has a base and emitter structure which is bounded on its edges by the isolation oxide or by the relatively thick oxide.

11 Claims, 12 Drawing Figures



United States Patent [19]

Parkinson

[11] **4,221,977**

[45] **Sep. 9, 1980**

[54] **STATIC I²L RAM**

[75] Inventor: **Ward D. Parkinson**, Dallas, Tex.

[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **968,051**

[22] Filed: **Dec. 11, 1978**

[51] **Int. Cl.**³ **G11C 11/40**; H01L 27/04

[52] **U.S. Cl.** **307/238**; 357/92; 357/50; 365/155; 365/156; 365/179; 365/181; 365/188

[58] **Field of Search** 357/92; 307/238; 365/154, 155, 156, 174, 179, 181, 188

[56] **References Cited**

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4,112,511	9/1978	Heald	307/238
4,158,237	6/1979	Wiedmann	307/238

FOREIGN PATENT DOCUMENTS

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481941	10/1975	U.S.S.R.	357/92

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Wiedmann, IBM Tech. Discl. Bulletin, vol. 14, No. 6, Nov. 1971, pp. 1721–1722.

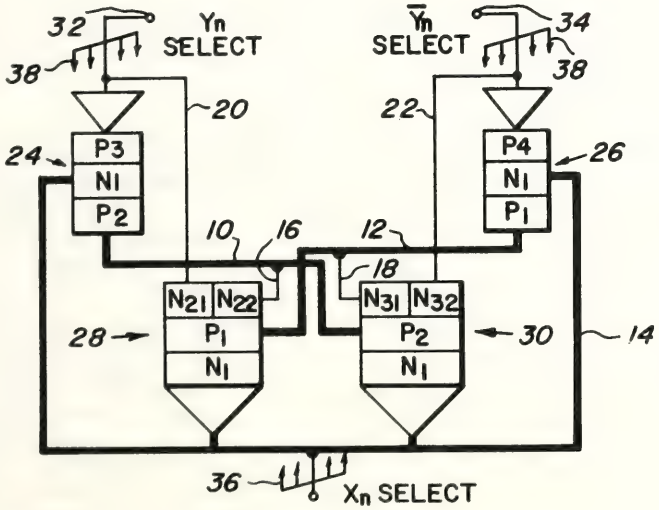
Primary Examiner—William D. Larkins

Attorney, Agent, or Firm—Vincent B. Ingrassia

[57] **ABSTRACT**

A unique topography of I²L bipolar semiconductor elements provides Read-Write Random Access Memory (RAM) with very high packing density, low cost, and good power and speed characteristics and with a very simple metallization pattern.

2 Claims, 5 Drawing Figures



United States Patent [19]

Takahashi

[11] **4,184,085**

[45] **Jan. 15, 1980**

[54] **SEMICONDUCTOR MEMORY DEVICE COMPRISING A P-N JUNCTION IN A POLYCRYSTALLINE SEMICONDUCTOR LAYER**

[75] Inventor: **Sakari Takahashi**, Tokyo, Japan

[73] Assignee: **Nippon Electric Co., Ltd.**, Tokyo, Japan

[21] Appl. No.: **868,321**

[22] Filed: **Jan. 10, 1978**

[30] **Foreign Application Priority Data**

Jan. 12, 1977 [JP] Japan 52/2623

[51] **Int. Cl.**² **G11C 11/40**; H01L 27/04

[52] **U.S. Cl.** **307/238**; 357/23; 357/41; 357/59; 365/186

[58] **Field of Search** 357/23, 24, 41, 59; 365/186; 307/238

[56] **References Cited**

U.S. PATENT DOCUMENTS

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3,858,232	12/1974	Boyle et al.	357/24
3,865,654	2/1975	Chang et al.	357/42
3,943,545	3/1976	Kim	357/24
4,060,738	11/1977	Tasch, Jr. et al.	357/59

OTHER PUBLICATIONS

Ho et al., IBM Tech. Discl. Bulletin, vol. 15, No. 2, Jul. 1972, pp. 412–413.

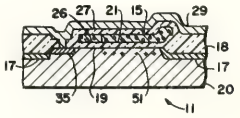
Primary Examiner—William D. Larkins

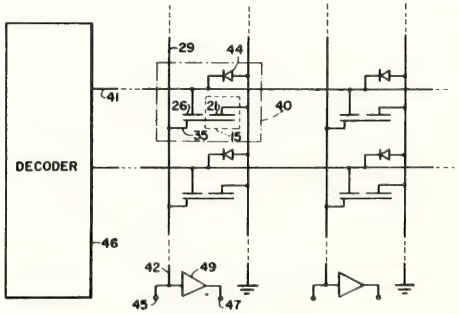
Attorney, Agent, or Firm—Hopgood, Calimafde, Kalil, Blaustein & Lieberman

[57] **ABSTRACT**

A semiconductor memory device of a surface-charge type comprises a p-type silicon substrate having a silicon dioxide film thereon and memory cells partly in the substrate and partly thereon in rows and columns. Each cell comprises an n+-type region beneath the oxide film, a polysilicon layer on the oxide film, and an insulator film integral on the polysilicon layer with the oxide films at positions where the polysilicon layer is not present. The polysilicon layer comprises a p-type portion serving as a storage capacitor electrode and an n-type portion forming a p-n junction with the p-type portion. The n-type portion is common to cells of each column to serve as a transfer gate electrode and a word line. A metal film formed on the insulator film is connected to the n+-type region of cells of each row to serve as a bit line. That region of the substrate which is opposite to the capacitor electrode is doped with a donor to insure storage of information-representative charges even with the capacitor electrode grounded. To reduce the resistance of the capacitor electrode, an intermediate metal film may be formed on the capacitor electrode except at its portion adjacent to the p-n junction.

19 Claims, 13 Drawing Figures





United States Patent [19]
Aomura et al.
[11] **4,191,595**
[45] **Mar. 4, 1980**

[54] **METHOD OF MANUFACTURING PN JUNCTIONS IN A SEMICONDUCTOR REGION TO REACH AN ISOLATION LAYER WITHOUT EXPOSING THE SEMICONDUCTOR REGION SURFACE**

[75] Inventors: **Kunio Aomura; Fujiki Tokuyoshi; Masahiko Nakamae**, all of Tokyo, Japan

[73] Assignee: **Nippon Electric Co., Ltd.**, Tokyo, Japan

[21] Appl. No.: **835,328**

[22] Filed: **Sep. 21, 1977**

[30] **Foreign Application Priority Data**

Sep. 22, 1976 [JP] Japan 51/114052

[51] **Int. Cl.**[2] **H01L 29/72; H01L 21/225**

[52] **U.S. Cl.** **148/1.5**; 357/20; 357/34; 357/50; 357/91

[58] **Field of Search** 357/20, 50, 34, 91; 148/1.5

[56] **References Cited**

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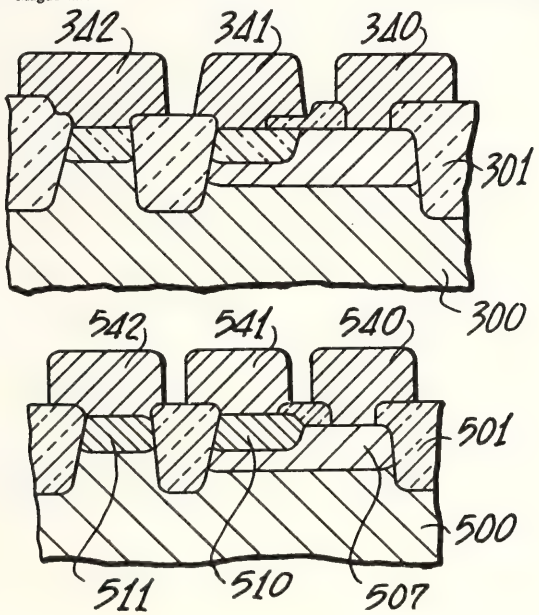
Ko, "Recessed Oxide Isolation Method", IBM-TDB, 19 (1976), 1222.

Primary Examiner—L. Dewayne Rutledge
Assistant Examiner—Upendra Roy
Attorney, Agent, or Firm—Hopgood, Calimafde, Kalil, Blaustein & Lieberman

[57] **ABSTRACT**

In a semiconductor device including at least one active semiconductor region isolated by an oxide layer in a semiconductor substrate having a principal surface, at least two PN junctions, terminating at the oxide layer, are formed in the active region, by introduction of impurities into the active region with the active region surface never exposed during their formation. The junctions may partly reach the principal surface. The impurities may be introduced by ion implantation through a thin oxide film overlying the active region, and through use of other films placed on the oxide film, or by the known melt-through technique. At least one junction may be formed by epitaxial growth of a semiconductor layer of the opposite conductivity type.

6 Claims, 52 Drawing Figures



United States Patent [19]
Kojima et al.
[11] **4,223,337**
[45] **Sep. 16, 1980**

[54] **SEMICONDUCTOR INTEGRATED CIRCUIT WITH ELECTRODE PAD SUITED FOR A CHARACTERISTIC TESTING**

[75] Inventors: **Hideto Kojima; Hisashi Funakoshi**, both of Tokyo, Japan

[73] Assignee: **Nippon Electric Co., Ltd.**, Tokyo, Japan

[21] Appl. No.: **942,730**

[22] Filed: **Sep. 15, 1978**

[30] **Foreign Application Priority Data**

Sep. 16, 1977 [JP] Japan 52-112064

[51] **Int. Cl.**[2] **H01L 23/48**; H01L 29/44; H01L 29/52

[52] **U.S. Cl.** **357/68**; 357/65; 357/46; 357/71; 307/315

[58] **Field of Search** 357/65, 68, 70, 71, 357/46; 307/315

[56] **References Cited**

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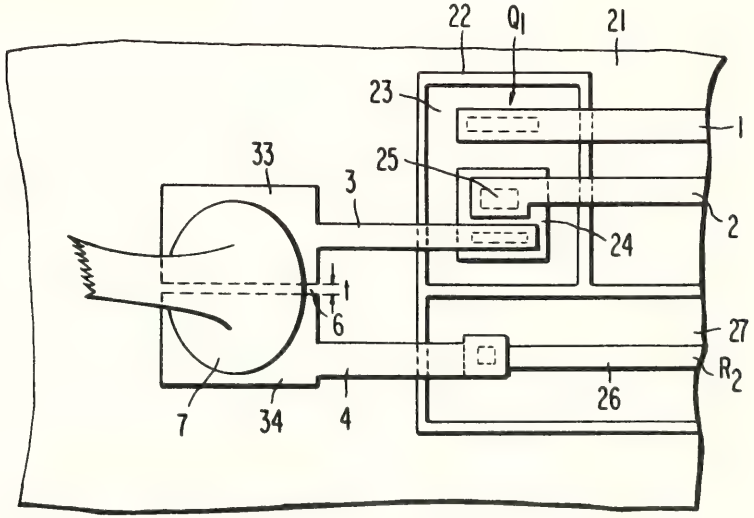
1315922	5/1973	United Kingdom	357/68

Primary Examiner—Andrew J. James
Attorney, Agent, or Firm—Sughrue, Rothwell, Mion, Zinn and Macpeak

[57] **ABSTRACT**

An integrated circuit device is provided with a divided electrode pad which permits checking the electrical characteristics of individual circuit elements before assembly into a package housing. After testing, the divided electrode pad is connected by thermally bonding one end of a single lead wire or the like to the divided parts.

10 Claims, 3 Drawing Figures



United States Patent [19]

Godejahn, Jr.

[11] **4,221,045**

[45] **Sep. 9, 1980**

[54] **SELF-ALIGNED CONTACTS IN AN ION IMPLANTED VLSI CIRCUIT**

[75] Inventor: **Gordon C. Godejahn, Jr.**, Santa Ana, Calif.

[73] Assignee: **Rockwell International Corporation**, El Segundo, Calif.

[21] Appl. No.: **913,184**

[22] Filed: **Jun. 6, 1978**

[51] **Int. Cl.**[3] **B01J 17/00**

[52] **U.S. Cl.** ..... **29/571**; 29/577 R; 29/578; 29/589; 29/590; 357/23; 357/41; 357/59

[58] **Field of Search** 29/571, 577, 578, 589, 29/590, 591; 357/23, 41, 59

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,072,545 2/1978 De La Moneda 357/59

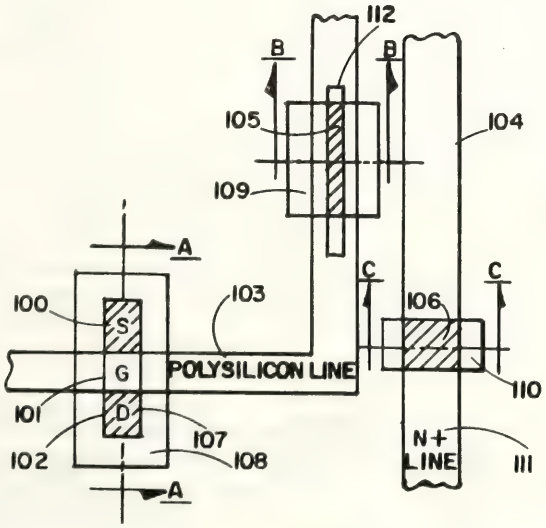
Primary Examiner—W. C. Tupman

Attorney, Agent, or Firm—H. Fredrick Hamann; Harry J. Staas

[57] **ABSTRACT**

A process for producing VLSI (very large scale integrated) circuits employs techniques of self-aligned gates and contacts for FET devices and for both diffused conducting lines in the substrate and polysilicon conducting lines situated on isolating field oxide formed on the substrate. Mask alignment tolerances are increased and rendered non-critical. The use of materials in successive layers having different etch characteristics permits selective oxidation of only desired portions of the structure without need for masking and removal of selected material from desired locations by batch removal processes again without use of masking. There results VLSI circuits having increased density and reliability. The process allows the simultaneous doping of two or more regions resulting in uniformity of device characteristics.

20 Claims, 14 Drawing Figures



United States Patent [19]

Custode

[11] **4,229,755**

[45] **Oct. 21, 1980**

[54] **FABRICATION OF VERY LARGE SCALE INTEGRATED CIRCUITS CONTAINING N-CHANNEL SILICON GATE NONVOLATILE MEMORY ELEMENTS**

[75] Inventor: **Frank Z. Custode**, Norco, Calif.

[73] Assignee: **Rockwell International Corporation**, El Segundo, Calif.

[21] Appl. No.: **934,223**

[22] Filed: **Aug. 15, 1978**

[51] **Int. Cl.**[3] **H01L 27/02**

[52] **U.S. Cl.** ..... **357/41**; 29/571; 29/578; 29/577 R

[58] **Field of Search** 29/571, 577, 578; 357/41

[56] **References Cited**

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4,161,417 7/1979 Yim 29/571

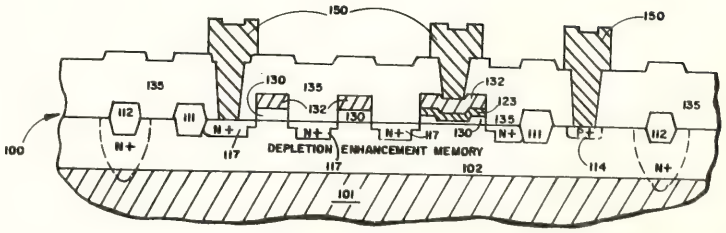
Primary Examiner—W. C. Tupman

Attorney, Agent, or Firm—H. Fredrick Hamann; Harry John Staas

[57] **ABSTRACT**

A method of fabricating very large scale integrated circuits including N-channel silicon gate nonvolatile memory elements and additional peripheral transistor elements. The nonvolatile memory elements are fabricated as PDS protected drain-source devices composed of a variable threshold memory device having a thin silicon dioxide gate insulator in combination with a pair of fixed threshold devices having a thicker silicon dioxide gate insulator arranged with a common silicon nitride layer and common gate electrode. The additional fixed threshold peripheral transistors are fabricated without a silicon nitride layer. In addition, the method contains no processing steps subsequent to the fabrication of the PDS devices which necessitate the application of temperatures in excess of 900° C.

10 Claims, 22 Drawing Figures



United States Patent [19]

Custode et al.

[11] **4,231,051**

[45] **Oct. 28, 1980**

[54] **PROCESS FOR PRODUCING MINIMAL GEOMETRY DEVICES FOR VSLI APPLICATIONS UTILIZING SELF-ALIGNED GATES AND SELF-ALIGNED CONTACTS, AND RESULTANT STRUCTURES**

[75] Inventors: **Frank Z. Custode**, Norco; **Matthias L. Tam**, Monterey Park, both of Calif.

[73] Assignee: **Rockwell International Corporation**, El Segundo, Calif.

[21] Appl. No.: **913,258**

[22] Filed: **Jun. 6, 1978**

[51] **Int. Cl.**[2] **H01L 29/78**

[52] **U.S. Cl.** ..... **357/23**; 29/571; 29/577 C; 29/589; 357/41; 357/59

[58] **Field of Search** 29/571, 577, 578, 589, 29/590, 591; 357/23, 41, 59

[56] **References Cited**

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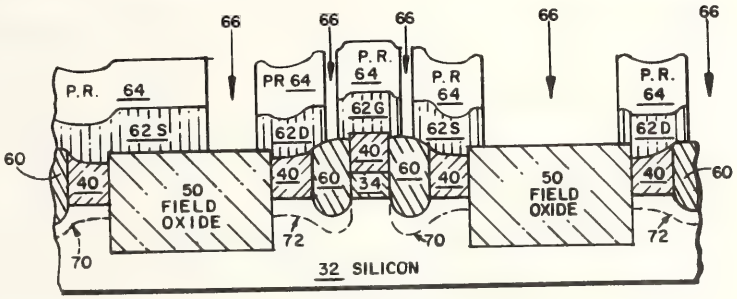
Primary Examiner—W. C. Tupman
Attorney, Agent, or Firm—H. Fredrick Hamann; Harry John Staas

[57] **ABSTRACT**

A process for producing VLSI (very large scale integrated) circuits employs techniques of self-aligned gates and contacts for FET devices and for diffused conducting lines in the substrate. Mask alignment tolerances are increased and rendered non-critical. The use of materials in successive layers having oxidation and etch characteristics permits selective oxidation of desired portions only of the structure without need for masking, and removal of selected material from desired locations by batch removal processes again without use of masking. There results semiconductor devices of minimum geometry with selective interconnection capabilities, affording VLSI circuits having increased density with improved yield and reliability.

10 Claims, 27 Drawing Figures



United States Patent [19]

Sato et al.

[11] **4,217,599**

[45] **Aug. 12, 1980**

[54] **NARROW CHANNEL MOS DEVICES AND METHOD OF MANUFACTURING**

[75] Inventors: **Shuichi Sato**, Beaverton; **Tadanori Yamaguchi**, Portland, both of Oreg.; **Arthur D. Ritchie**, San Diego, Calif.

[73] Assignee: **Tektronix, Inc.**, Beaverton, Oreg.

[21] Appl. No.: **862,715**

[22] Filed: **Dec. 21, 1977**

[51] **Int. Cl.**[2] **H01L 29/78**; H01L 27/02; H01L 29/06

[52] **U.S. Cl.** **357/23**; 357/41; 357/56; 357/91

[58] **Field of Search** 357/23, 91, 41, 56

[56] **References Cited**

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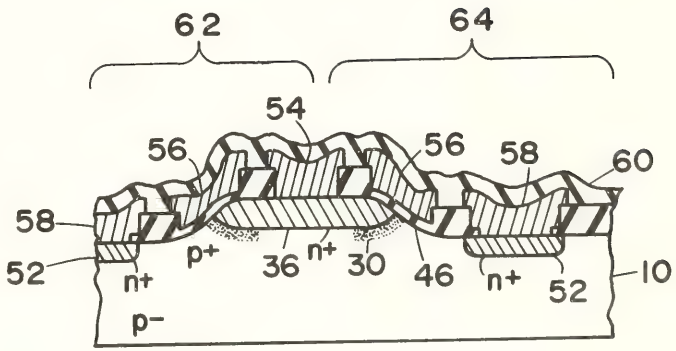
Primary Examiner—Andrew J. James
Attorney, Agent, or Firm—John D. Winkelman

[57] **ABSTRACT**

Improved, high performance MOS transistors are provided by a method that includes providing an oxygen-impermeable mask on a selected region of a semiconductor substrate, oxidizing the unmasked portion of the surface to provide a thick oxide at least partially recessed in the substrate, which layer includes a smoothly tapered beak that extends between the margin of the mask and the underlying silicon surface, and, after removing the mask, implanting a selected impurity in the substrate beneath the selected region to form a thin impurity layer that terminates at a sloped portion of the substrate formed by the oxidation step.

10 Claims, 16 Drawing Figures



United States Patent [19]

Sato et al.

[11] **4,228,447**

[45] **Oct. 14, 1980**

[54] **SUBMICRON CHANNEL LENGTH MOS INVERTER WITH DEPLETION-MODE LOAD TRANSISTOR**

[75] Inventors: **Shuichi Sato**, Beaverton; **Tadanori Yamaguchi**, Hillsboro, both of Oreg.

[73] Assignee: **Tektronix, Inc.**, Beaverton, Oreg.

[21] Appl. No.: **11,598**

[22] Filed: **Feb. 12, 1979**

[51] **Int. Cl.**[2] **H01L 27/02**

[52] **U.S. Cl.** **357/42**; 357/23; 357/41; 357/46; 357/55; 357/56

[58] **Field of Search** 357/23, 41, 42, 46, 357/55, 56

[56] **References Cited**

U.S. PATENT DOCUMENTS

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Research and Education Assn., N. Y. (1972), p. 602, Fogiel.

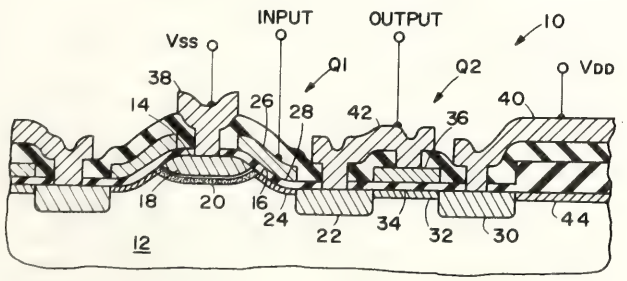
Primary Examiner—Edward J. Wojciechowicz

Attorney, Agent, or Firm—John D. Winkelman

[57] **ABSTRACT**

An improved, high speed n-channel MOS inverter structure including a self-aligned silicon gate depletion-mode load device integrated in series with a nonplanar, submicron channel enhancement-mode switching transistor. The enhancement-mode switching device is formed on a field of the substrate that includes an elevated, plateau region joined to a surrounding planar area by a slope. The MOS load transistor is formed on an adjoining planar portion of the surface. The process for fabricating the devices features successive ion implation of boron and arsenic through an oxide layer that includes a smoothly tapered "beak" formed by a local oxidation technique.

5 Claims, 9 Drawing Figures



United States Patent [19]

Sato et al.

[11] **4,229,756**

[45] **Oct. 21, 1980**

[54] **ULTRA HIGH SPEED COMPLEMENTARY MOS DEVICE**

[75] Inventors: **Shuichi Sato**, Beaverton; **Tadanori Yamaguchi**, Hillsboro; **Jack Sachitano**, Portland, all of Oreg.

[73] Assignee: **Tektronix, Inc.**, Beaverton, Oreg.

[21] Appl. No.: **10,665**

[22] Filed: **Feb. 9, 1979**

[51] **Int. Cl.**[2] **H01L 27/02**

[52] **U.S. Cl.** **357/42**; 357/23; 357/41; 357/46; 357/55; 357/56

[58] **Field of Search** 357/23, 41, 42, 46, 357/55, 56

[56] **References Cited**

U.S. PATENT DOCUMENTS

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4,063,274 12/1977 Dingwall 357/53

OTHER PUBLICATIONS

Electronics-Dec. 7, 1978, pp. 41–42.

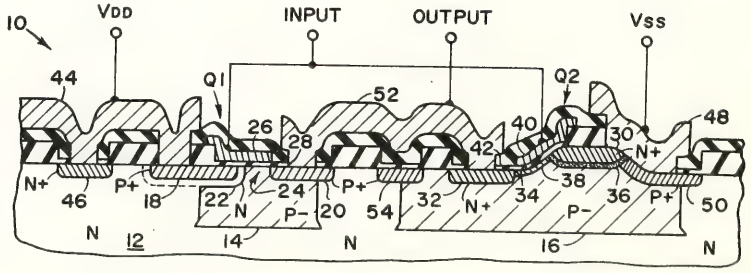
Primary Examiner—Edward J. Wojciechowicz

Attorney, Agent, or Firm—John D. Winkelman

[57] **ABSTRACT**

An improved, ultra high speed (2GHz) CMOS inverter structure comprising a double-diffused, planar p-channel transistor and a nonplanar n-channel transistor formed within adjacent surface fields on the same substrate. The n-channel device includes a source region formed in an elevated, plateau region on the substrate, and a narrow, implanted channel-forming layer that extends through the plateau beneath the source region and terminates at a slope joining the plateau to surrounding lower elevation portions of the substrate. A drain region is formed adjacent the foot of the slope, spaced from the channel to provide a drift region between them.

8 Claims, 9 Drawing Figures



United States Patent [19]
Trotter et al.
[11] **4,222,062**
[45] **Sep. 9, 1980**

[54] **VMOS FLOATING GATE MEMORY DEVICE**

[75] Inventors: **James D. Trotter**, Saratoga; **Thurman J. Rodgers**, Menlo Park, both of Calif.

[73] Assignee: **American Microsystems, Inc.**, Santa Clara, Calif.

[21] Appl. No.: **683,185**

[22] Filed: **May 4, 1976**

[51] **Int. Cl.**[2] **H01L 27/10;** G11C 11/40
[52] **U.S. Cl.** **357/45;** 357/23; 357/55; 357/59; 357/60; 357/71; 365/185
[58] **Field of Search** 357/23, 41, 54, 60, 357/59, 45; 365/184, 185

[56] **References Cited**

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OTHER PUBLICATIONS

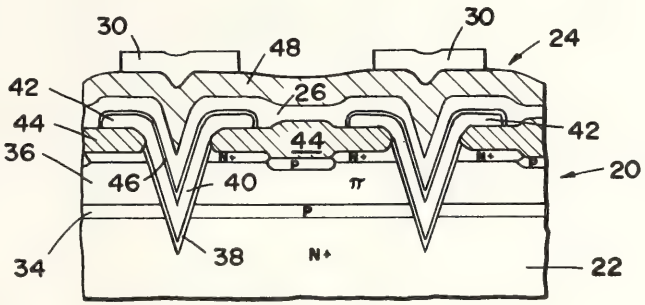
Rogers et al., "VMOS: . . . ", IEEE J. of Solid-State Circuits, vol. SC9, No. 5, Oct. 1974, pp. 247-249.

Primary Examiner—William D. Larkins
Attorney, Agent, or Firm—Owen, Wickersham & Erickson

[57] **ABSTRACT**

A semiconductor programmable read only memory device (PROM) utilizes an array of memory cells each having an area basically defined by the intersection of a bit line and a word address line. On a substrate of one conductivity type is an upper layer of material of the opposite conductivity within which are diffused bit lines of the same conductivity material as the substrate. The crossing address lines are conductive material formed on an insulating layer that covers the diffused bit lines and the upper layer. Each cell is a single transistor element in the form of a V-type MOSFET which achieves the normal AND function (Data-Word Address) using a capacitance coupled version of threshold logic. Each MOSFET is formed by a V-shaped recess at the intersection of each bit line and address line that extends through the diffused bit line, (which serves as the transistor drain) and into the substrate (which serves as the source and ground plane of the device). A similarly V-shaped floating gate is isolated below and above the crossing bit and address lines by thin oxide layers. Data is written into the cell when hot electrons are injected into the gate oxide near the drain junction and attracted to the floating gate which has been charged positive by capacitance coupling from the word line. The hot electrons are generated from the channel current via impact ionization at the pinched-off drain junction.

2 Claims, 14 Drawing Figures



United States Patent [19]
Rodgers
[11] **4,222,063**
[45] **Sep. 9, 1980**

[54] **VMOS FLOATING GATE MEMORY WITH BREAKDOWN VOLTAGE LOWERING REGION**

[75] Inventor: **Thurman J. Rodgers**, Palo, Calif.

[73] Assignee: **American Microsystems**, Santa Clara, Calif.

[21] Appl. No.: **910,789**

[22] Filed: **May 30, 1978**

[51] **Int. Cl.**[2] **H01L 27/10;** G11C 11/40
[52] **U.S. Cl.** **357/45;** 357/23; 357/55; 357/59; 357/60; 357/89; 365/185
[58] **Field of Search** 357/23, 45, 60, 59; 365/184, 185

[56] **References Cited**

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4,016,588	4/1977	Ohya et al.	357/54

OTHER PUBLICATIONS

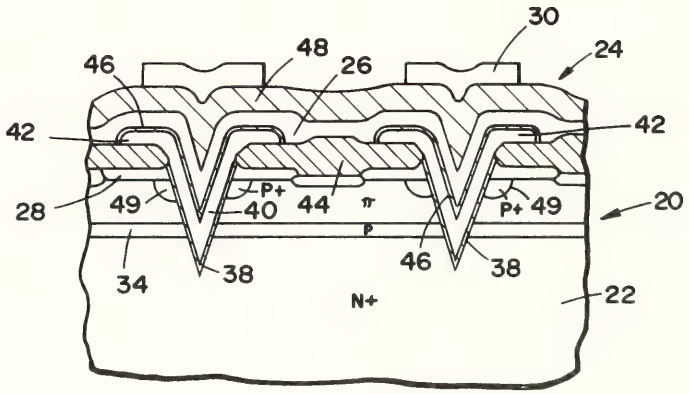
Rodgers et al., VMOS Memory Technology, IEEE Journal of Solid-State Circuits, vol. SC-12, No. 5, Oct. 1977, pp. 515-524.
Jenne' et al., "VMOS EPROM and Buried Source RAM Structures", *IEDM Late News Papers*, (Suppl. to *1976 IEDM Technical Digest*), pub. Dec. 5, 1976.

Primary Examiner—William D. Larkins
Attorney, Agent, or Firm—Owen, Wickersham & Erickson

[57] **ABSTRACT**

A semiconductor electrically programmable read only memory device (EPROM) utilizes an array of memory cells each in the form of a single V-type MOSFET which achieves the normal AND function (Data-Word Address) using a capacitance coupled version of threshold logic. Each MOSFET is formed by a V-shaped recess at the intersection of each bit line and word line that extends across the diffused bit line, (which serves as the transistor drain) and into the substrate (which serves as the source and ground plane of the device). A similarly V-shaped floating gate is isolated below and above the crossing bit and word lines by thin oxide layers. A ring of P-type conductive material around the upper end of each V-shaped recess and adjacent its surrounding N-type drain region serves to lower the required programming voltage without increasing the device threshold voltage.

2 Claims, 11 Drawing Figures



United States Patent [19]

Shanks

[11] **4,203,123**

[45] **May 13, 1980**

[54] **THIN FILM MEMORY DEVICE EMPLOYING AMORPHOUS SEMICONDUCTOR MATERIALS**

[75] Inventor: **Roy R. Shanks**, San Diego, Calif.

[73] Assignee: **Burroughs Corporation**, Detroit, Mich.

[21] Appl. No.: **859,580**

[22] Filed: **Dec. 12, 1977**

[51] **Int. Cl.**[2] **H01L 27/24**

[52] **U.S. Cl.** **357/2**; 357/45; 357/15; 365/163

[58] **Field of Search** 357/1, 2, 4, 45

[56] **References Cited**

U.S. PATENT DOCUMENTS

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Cole et al., IBM Tech. Discl. Bulletin, vol. 15, No. 6, Nov. 1971, pp. 2015–2016.

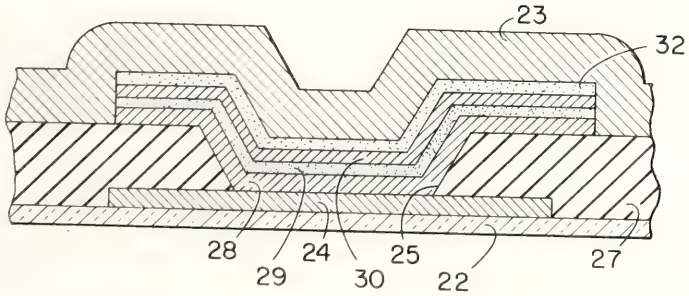
Primary Examiner—William D. Larkins
Attorney, Agent, or Firm—Mervyn L. Young; Kevin R. Peterson

[57] **ABSTRACT**

This disclosure relates to a thin film amorphous memory cell which can be fabricated upon the surface of a semiconductor substrate in such a manner as to minimize the surface area requirements for each cell thereby increase the packing density of the memory array. Furthermore, since the cell can be fabricated on top of the semiconductor substrate, other active devices can be fabricated in the substrate so as to further increase the packing density of the integrated circuit chip containing memory array or other circuits.

The memory cell is formed of a thin film diode of one or more amorphous semiconductor layers that are doped to form either a PN junction diode or, with one such layer, a Schottky diode, and the memory cell includes an amorphous layer of a tellurium based chalcogenide material that may be employed in either a memory mode or a threshold mode so that the memory cell may be operated in either a non-volatile or volatile manner.

3 Claims, 11 Drawing Figures



United States Patent [19]

Vinson

[11] **4,225,879**

[45] **Sep. 30, 1980**

[54] **V-MOS FIELD EFFECT TRANSISTOR FOR A DYNAMIC MEMORY CELL HAVING IMPROVED CAPACITANCE**

[75] Inventor: **Mark A. Vinson**, San Diego, Calif.

[73] Assignee: **Burroughs Corporation**, Detroit, Mich.

[21] Appl. No.: **6,660**

[22] Filed: **Jan. 26, 1979**

Related U.S. Application Data

[63] Continuation of Ser. No. 864,383, Dec. 27, 1977, abandoned.

[51] **Int. Cl.**[2] **H01L 29/06**

[52] **U.S. Cl.** **357/55**; 357/23; 357/41; 357/45

[58] **Field of Search** 357/23, 41, 45, 55

[56] **References Cited**

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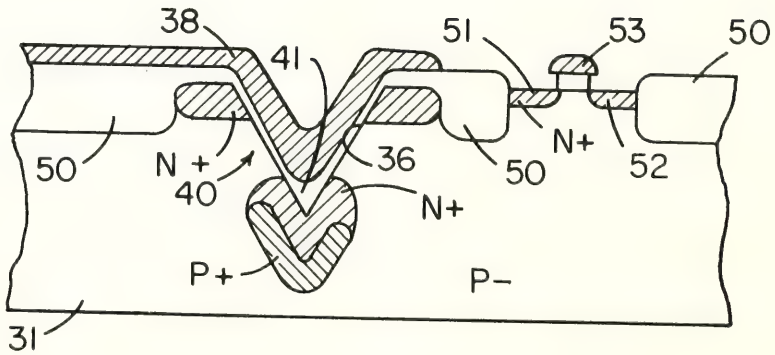
Primary Examiner—Edward J. Wojciechowicz
Attorney, Agent, or Firm—Charles J. Fassbender; Mervyn L. Young; Kevin R. Peterson

[57] **ABSTRACT**

This disclosure relates to a V-MOS field effect transistor which is provided with enhanced source capacitance to provide a single transistor dynamic memory cell. The formation of the source area is achieved by masking the silicon substrate, opening an aperture in the mask and then etching the silicon substrate in such a manner as to undercut the mask so that the mask provides a shield to subsequent ion implanting of the source area. Both P and N type dopants can be separately implanted with different energy levels so as to form an enhanced PN junction capacitance for the device. Such a field effect transistor can be achieved without the formation of a graded dopant concentration in the channel between the source and drain areas of the transistor.

8 Claims, 12 Drawing Figures



United States Patent [19]
Maruyama et al.
[11] **4,199,777**
[45] **Apr. 22, 1980**

[54] **SEMICONDUCTOR DEVICE AND A METHOD OF MANUFACTURING THE SAME**

[75] Inventors: **Eiichi Maruyama**, Kodaira; **Hideaki Yamamoto**, Hachioji, both of Japan

[73] Assignee: **Hitachi, Ltd.**, Japan

[21] Appl. No.: **764,845**

[22] Filed: **Feb. 2, 1977**

[30] **Foreign Application Priority Data**

Feb. 2, 1976 [JP] Japan 51/9381

[51] **Int. Cl.**[2] **H01L 29/06**
[52] **U.S. Cl.** **357/55**; 357/49; 357/59; 357/68; 357/69; 357/71
[58] **Field of Search** 357/71, 55, 49, 59, 357/68, 69

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,699,407	10/1972	Gurtler et al.	357/55
3,754,161	8/1973	Johnson	357/59
3,761,782	9/1973	Youmans	357/55
3,858,237	12/1974	Sawazaki et al.	357/59
3,864,817	2/1975	Lapham et al.	357/59
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FOREIGN PATENT DOCUMENTS

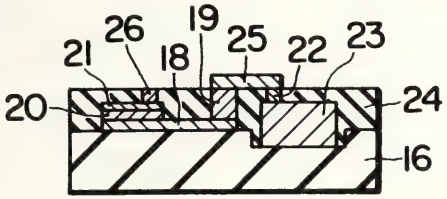
2031444	6/1970	Fed. Rep. of Germany	357/55
1165187	9/1969	United Kingdom	357/55

Primary Examiner—Edward J. Wojciechowicz
Attorney, Agent, or Firm—Craig and Antonelli

[57] **ABSTRACT**

A semiconductor device includes at least two different elements having different functions. At least one of the elements is fixed within a recess provided in a substrate, and wirings are provided on an insulating film deposited commonly on the elements and the substrate, so that there is no step or clearance between the elements or between the element and the substrate, making it possible to easily form good interconnections.

22 Claims, 25 Drawing Figures



United States Patent [19]
Okabe et al.
[11] **4,213,140**
[45] **Jul. 15, 1980**

[54] **INSULATED-GATE SEMICONDUCTOR DEVICE**

[75] Inventors: **Takeaki Okabe**, Kokubunji; **Isao Yoshida**, Tokyo; **Mineo Katsueda**, Kokubunji; **Hidefumi Ito**; **Masatomo Furumi**, both of Takasaki; **Shikayuki Ochi**, Akishima, all of Japan

[73] Assignee: **Hitachi, Ltd.**, Tokyo, Japan

[21] Appl. No.: **922,371**

[22] Filed: **Jul. 6, 1978**

[30] **Foreign Application Priority Data**

Jul. 22, 1977 [JP] Japan 52-87396

[51] **Int. Cl.**[2] **H01L 27/07**
[52] **U.S. Cl.** **357/41**; 357/23; 307/251
[58] **Field of Search** 357/23, 41, 42; 307/251

[56] **References Cited**

U.S. PATENT DOCUMENTS

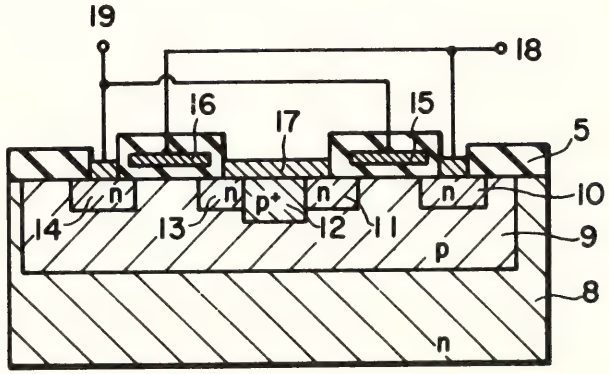
4,074,151	2/1978	Buckley et al.	307/251

Primary Examiner—Edward J. Wojciechowicz
Attorney, Agent, or Firm—Craig and Antonelli

[57] **ABSTRACT**

An insulated-gate semiconductor device wherein a first region is formed in the surface of a semiconductor substrate, the first region having a conductivity type opposite to that of the substrate, two insulated-gate FET's are formed within the first region, the drain of the first insulated-gate FET and that of the second insulated-gate FET are made common, the drains are electrically connected to the first region, and the gate of the first insulated-gate FET and the source of the second insulated-gate FET, and the gate of the second insulated-gate FET and the source of the first insulated-gate FET are respectively connected, thereby to prevent the occurrence of a negative resistance.

16 Claims, 10 Drawing Figures



United States Patent [19]
Raffel et al.

[11] **4,184,172**
[45] **Jan. 15, 1980**

[54] **DIELECTRIC ISOLATION USING SHALLOW OXIDE AND POLYCRYSTALLINE SILICON**

[75] Inventors: **Jack I. Raffel**, Lexington; **Stephen E. Bernacki**, Worcester, both of Mass.

[73] Assignee: **Massachusetts Institute of Technology**, Cambridge, Mass.

[21] Appl. No.: **773,637**

[22] Filed: **Feb. 28, 1977**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 747,743, Dec. 6, 1976, abandoned.

[51] **Int. Cl.**[2] **H01L 27/04**
[52] **U.S. Cl.** **357/50**; 357/49; 357/51; 357/52; 357/55; 357/59
[58] **Field of Search** 357/49, 50, 51, 52, 357/55, 59

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,009,484 2/1977 Ogiue et al. 357/50
4,016,596 4/1977 Magdo et al. 357/50

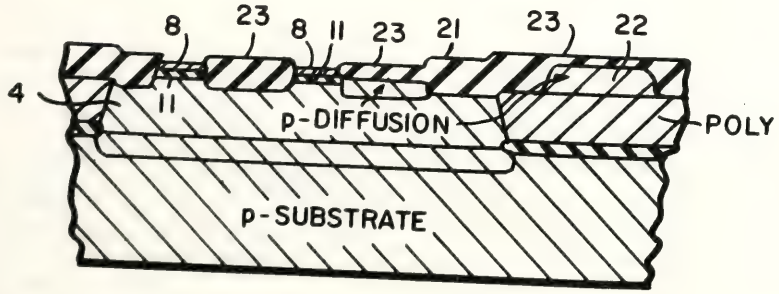
Primary Examiner—Edward J. Wojciechowicz
Attorney, Agent, or Firm—Arthur A. Smith, Jr.; Gary A. Walpert

[57] **ABSTRACT**

A process is described which combines polycrystalline isolation of collectors and shallow oxide isolation of bases. This approach is capable of providing deep dielectric isolation, surface planarity and the high density of walled emitter geometries, a combination heretofore unobtainable by any other means.

This isolation scheme has been used to fabricate ECL gate chains. The transistors were located in 2.5 micron thick n-epi islands surrounded by 5×10^5 ohm-cm polysilicon selectively oxidized with silicon nitride masking to a thickness of one micron. The oxide "bump" at the nitride mask was typically 3000 Å and the epi-poly step height was as small as 2600 Å. The circuits have polysilicon resistors and were fabricated using both thermal diffusion and ion implantation. The power-delay product of these circuits was approximately one-half that of junction isolated circuits.

19 Claims, 13 Drawing Figures



United States Patent [19]
Senturia

[11] **4,209,796**
[45] **Jun. 24, 1980**

[54] **CHARGE-FLOW TRANSISTORS HAVING METALLIZATION PATTERNS**

[75] Inventor: **Stephen D. Senturia**, Cambridge, Mass.

[73] Assignee: **Massachusetts Institute of Technology**, Cambridge, Mass.

[21] Appl. No.: **853,059**

[22] Filed: **Nov. 21, 1977**

[51] **Int. Cl.**[2] **H01L 29/76**
[52] **U.S. Cl.** **357/23**; 357/41; 357/25; 357/52
[58] **Field of Search** 357/23, 41

[56] **References Cited**

U.S. PATENT DOCUMENTS

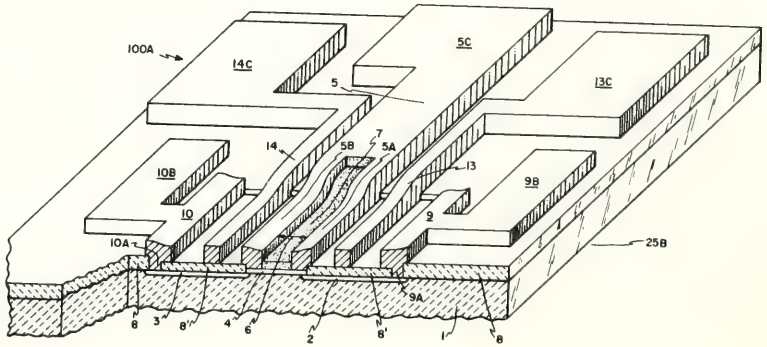
4,044,373 8/1977 Nomiya et al. 357/41
4,062,039 12/1977 Nishimura 357/41
4,065,782 12/1977 Gray 357/23

Primary Examiner—Edward J. Wojciechowicz
Attorney, Agent, or Firm—Arthur A. Smith, Jr.; Robert Shaw

[57] **ABSTRACT**

A charge-flow transistor having a source region and a drain region in a semiconductor substrate, a gate insulator, and a gapped gate electrode with a thin-film material having some electrical conductance disposed in the gap thereof. Metallization patterns are provided to reduce the detrimental effect of parasitic currents that appear within the transistor. There is disclosed also a plurality of such transistors in a single die with metallization to reduce any effect of parasitic currents between the transistors of the plurality.

45 Claims, 12 Drawing Figures



United States Patent [19]
DeLise
[11] **4,194,174**
[45] **Mar. 18, 1980**

[54] **METHOD FOR FABRICATING BALLASTED FINGER ELECTRODE**

[75] Inventor: **Michael F. DeLise**, Doylestown, Pa.

[73] Assignee: **Microwave Semiconductor Corp.**, Somerset, N.J.

[21] Appl. No.: **916,904**

[22] Filed: **Jun. 19, 1978**

[51] **Int. Cl.**[2] **H01C 1/012**
[52] **U.S. Cl.** **338/308**; 427/101; 427/103
[58] **Field of Search** 338/308, 20; 357/68; 29/589, 590; 427/101, 102, 103

[56] **References Cited**

U.S. PATENT DOCUMENTS

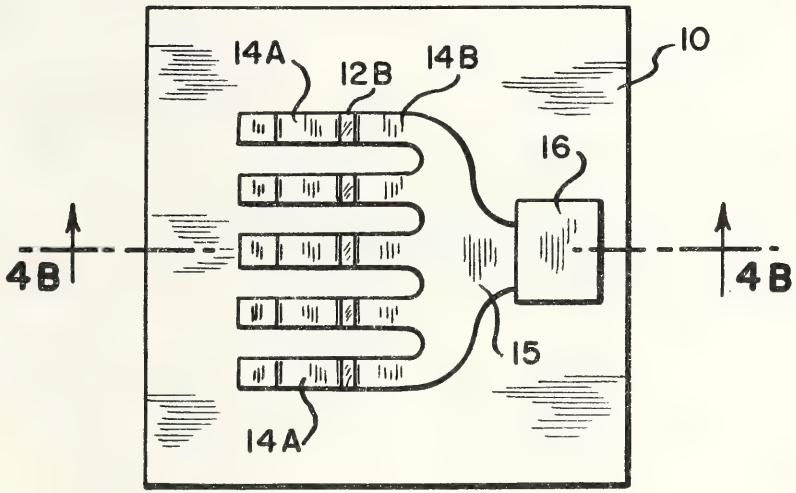
3,225,261	12/1965	Wolf	357/28 X
3,742,319	6/1973	Bryan et al.	357/68 X
4,091,409	5/1978	Wheatley, Jr.	357/68 X

Primary Examiner—C. L. Albritton
Attorney, Agent, or Firm—Pennie & Edmonds

[57] **ABSTRACT**

A ballasted finger electrode structure is fabricated on a substrate by the steps of depositing on the substrate a layer of resistive material, forming one or more dielectric regions on the resistive layer; and forming two or more finger electrode segments spaced apart over one or more of the dielectric regions but electrically connected by the resistive region underlying the dielectric region. The result is a finger electrode structure with a precisely defined length of resistive ballasting.

6 Claims, 7 Drawing Figures



United States Patent [19]
Frey
[11] **4,200,880**
[45] **Apr. 29, 1980**

[54] **MICROWAVE TRANSISTOR WITH DISTRIBUTED OUTPUT SHUNT TUNING**

[75] Inventor: **Richard H. Frey**, Hampton, N.J.

[73] Assignee: **Microwave Semiconductor Corp.**, Somerset, N.J.

[21] Appl. No.: **891,009**

[22] Filed: **Mar. 28, 1978**

[51] **Int. Cl.**[2] **H01L 27/02**
[52] **U.S. Cl.** **357/51**; 357/55; 357/68; 357/80
[58] **Field of Search** 357/51, 55, 68, 80

[56] **References Cited**

U.S. PATENT DOCUMENTS

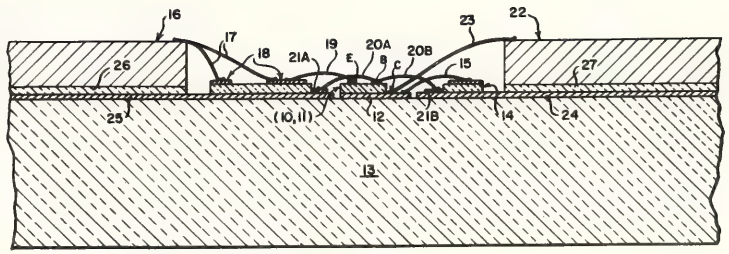
3,825,805	7/1974	Belohoubeck et al.	357/51

Primary Examiner—Edward J. Wojciechowicz
Attorney, Agent, or Firm—Pennie & Edmonds

[57] **ABSTRACT**

A microwave transistor having a base and an elongated collector is provided with an elongated, grounded, DC blocking capacitor co-extensive with the collector and the output capacitance (C_{ob}) is tuned within the transistor package by distributing along the collector a plurality of inductive wire leads connecting the collector to the base through the DC blocking capacitor. Ground returns are provided by base connections to ground on both the input and output sides of the transistor. Such an arrangement provides isolation between input and output while uniformly distributing the reactance of the tuning elements across the entire active area. The result is an increased power output as compared to conventional shunt tuning arrangements.

13 Claims, 3 Drawing Figures



United States Patent [19]

Brower

[11] **4,210,465**

[45] **Jul. 1, 1980**

[54] **CISFET PROCESSING INCLUDING SIMULTANEOUS IMPLANTATION OF SPACED POLYCRYSTALLINE SILICON REGIONS AND NON-MEMORY FET CHANNEL**

[75] Inventor: **Ronald W. Brower**, Dayton, Ohio

[73] Assignee: **NCR Corporation**, Dayton, Ohio

[21] Appl. No.: **962,422**

[22] Filed: **Nov. 20, 1978**

[51] **Int. Cl.**[2] **H01L 7/34**; H01L 11/00; B01J 17/00

[52] **U.S. Cl.** **148/1.5**; 148/187; 357/23; 357/40; 357/59; 357/91

[58] **Field of Search** 148/1.5, 187; 357/23, 357/41, 91, 59, 40; 29/571

[56] **References Cited**

U.S. PATENT DOCUMENTS

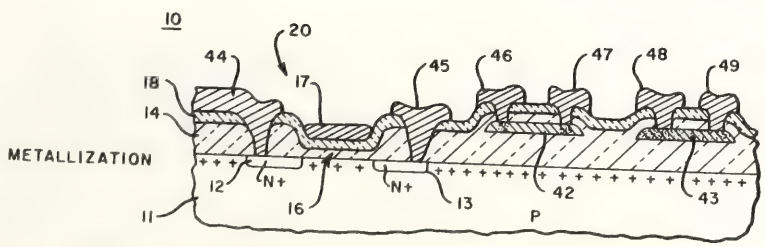
3,841,926	10/1974	Garnache et al.	148/188
3,889,358	6/1971	Bierhenke	29/571
3,891,190	6/1975	Vadasz	357/41
3,996,657	12/1976	Simko	29/571
4,011,105	3/1977	Paivinen et al.	148/1.5
4,019,197	4/1977	Lohstroh et al.	357/23
4,075,045	2/1978	Rideout	148/175
4,080,718	3/1978	Richman	29/571
4,080,719	3/1978	Wilting	29/571
4,099,317	7/1978	Su	29/571
4,102,733	7/1978	De La Moneda et al.	156/633

Primary Examiner—L. Dewayne Rutledge
Assistant Examiner—Upendra Roy
Attorney, Agent, or Firm—J. T. Cavender; Philip A. Dalton

[57] **ABSTRACT**

A process for forming a CIS (conductor-insulator-semiconductor) integrated circuit having one or more non-memory field-effect transistors, and one or more polysilicon resistors and/or polysilicon conductors. A single mask and implant sequence is used to establish the threshold voltage of the field-effect transistor and the resistance (conductance) of the polysilicon components. The polysilicon components are formed to predetermined sizes, as needed, so that the threshold-determining implant provides the desired polysilicon resistance value(s).

6 Claims, 12 Drawing Figures



United States Patent [19]

Brower

[11] **4,212,684**

[45] **Jul. 15, 1980**

[54] **CISFET PROCESSING INCLUDING SIMULTANEOUS DOPING OF SILICON COMPONENTS AND FET CHANNELS**

[75] Inventor: **Ronald W. Brower**, Dayton, Ohio

[73] Assignee: **NCR Corporation**, Dayton, Ohio

[21] Appl. No.: **962,423**

[22] Filed: **Nov. 20, 1978**

[51] **Int. Cl.**[2] **H01L 29/78**; H01L 21/96; B01J 17/00; H01L 11/14

[52] **U.S. Cl.** **148/1.5**; 29/571; 148/187; 357/23; 357/41; 357/59; 357/91

[58] **Field of Search** 148/1.5, 187; 357/23, 357/41, 91, 59; 29/571

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,750,268	8/1973	Wang	29/571
3,868,274	2/1975	Hubar et al.	148/1.5
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4,080,718	3/1978	Richman	29/571
4,095,251	6/1978	Dennard	357/23
4,101,921	7/1978	Shimada et al.	357/23
4,104,784	8/1978	Klein	29/571
4,110,776	8/1978	Rao et al.	357/23

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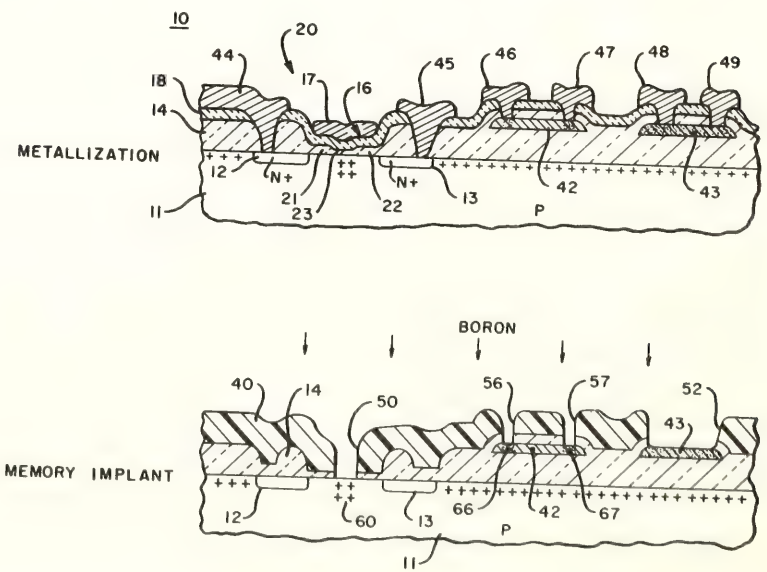
Tsuchimoto et al., "Ion Impl^n . . . Polycrystalline Si", Ion Implantation in Semiconductors, Ed. Namba, Plenum, New York, 1974.

Primary Examiner—L. Dewayne Rutledge
Assistant Examiner—Roy Upendra
Attorney, Agent, or Firm—J. T. Cavender; Philip A. Dalton

[57] **ABSTRACT**

A process for forming a CIS (conductor-insulator-semiconductor) integrated circuit having one or more field-effect memory transistors, and one or more polysilicon resistors and/or polysilicon conductors. The polysilicon components are formed to predetermined sizes, as needed, so that the implant used to establish the memory threshold voltage of the transistor also provides the desired polysilicon resistance value(s). The process may be used to simultaneously form both memory and non-memory transistors.

12 Claims, 13 Drawing Figures



United States Patent [19]
Nishimura et al.
[11] **4,216,451**
[45] **Aug. 5, 1980**

[54] **VARIABLE CAPACITANCE DEVICE HAVING A PLURALITY OF CAPACITANCE ELEMENTS AND A PLURALITY OF SWITCHING ELEMENTS THEREFOR FORMED ON A SINGLE COMMON SUBSTRATE**

[75] Inventors: **Itsuro Nishimura**, Takatsuki; **Tsutomu Ohgishi**, Yahata, both of Japan

[73] Assignee: **Sanyo Electric Co., Ltd.**, Osaka, Japan

[21] Appl. No.: **885,281**

[22] Filed: **Mar. 10, 1978**

[30] **Foreign Application Priority Data**

Mar. 10, 1977 [JP] Japan 52-27827

[51] **Int. Cl.**[2] **H03J 5/24**; H03J 3/18
[52] **U.S. Cl.** **334/15**; 307/303; 307/304; 334/55; 357/51
[58] **Field of Search** 307/304; 357/23, 51; 334/15, 55

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,427,514	2/1969	Olmstead et al.	357/23
3,657,560	4/1972	Proebsting	307/304
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4,141,027	2/1979	Baldwin et al.	357/23 X

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1566228	9/1969	France .

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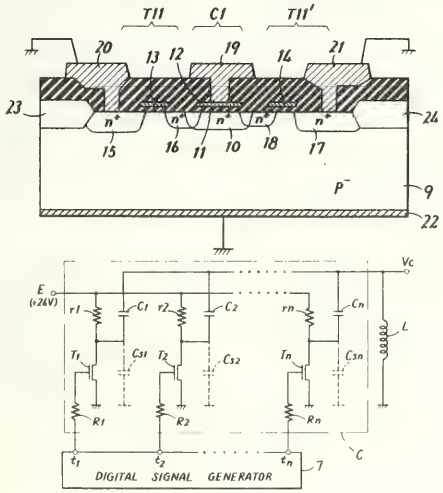
Eaton, S. S. "Sapphire Brings Out the Best in C-Mos", Electronics, Jun. 1975, pp. 115-118.
Benz, H. F. et al, "A Linear Voltage-Tunable Distributed Null Device", IEEE Journal of Solid-State Circuits, Dec. 1972, pp. 499-503.

Primary Examiner—Paul L. Gensler
Attorney, Agent, or Firm—Armstrong, Nikaido, Marmelstein & Kubovcik

[57] **ABSTRACT**

A variable capacitance semiconductor device is provided wherein a plurality of capacitance elements each having a fixed capacitance value are coupled in parallel with each other and at least two insulated gate field effect transistors are provided for each of the plurality of capacitance elements, whereby the total length of the insulated gate field effect transistors is made as long as possible and accordingly the resistance across the transistors when these are turned on becomes small. Each capacitance element may comprise a single semiconductor substrate of one conductivity type, an opposite conductivity type region formed on one surface of the substrate, an insulating layer formed on the opposite conductivity type region and an electrode formed on the insulating layer. The above described at least two insulated gate field effect transistors are formed such that the above described substrate is shared. Preferably, a direct current voltage is applied to the opposite conductivity type region in the direction for decreasing the junction capacitance between the opposite conductivity type region and the substrate occuring when the above described transistors are turned off.

35 Claims, 13 Drawing Figures



United States Patent [19]
Sawazaki
[11] **4,217,149**
[45] **Aug. 12, 1980**

[54] **METHOD OF MANUFACTURING COMPLEMENTARY INSULATED GATE FIELD EFFECT SEMICONDUCTOR DEVICE BY MULTIPLE IMPLANTATIONS AND DIFFUSION**

[75] Inventor: **Tamaki Sawazaki**, Gunma, Japan

[73] Assignees: **Sanyo Electric Co., Ltd.**, Moriguchi; **Tokyo Sanyo Electric Co., Ltd.**, Gunma, both of Japan

[21] Appl. No.: **14,922**

[22] Filed: **Feb. 26, 1979**

Related U.S. Application Data

[62] Division of Ser. No. 828,852, Aug. 29, 1977, abandoned.

[30] **Foreign Application Priority Data**

Sep. 8, 1976 [JP] Japan 51-108602

[51] **Int. Cl.**[2] **H01L 21/263**; H01L 7/54; H01L 21/225
[52] **U.S. Cl.** **148/1.5**; 148/187; 357/23; 357/44; 357/91
[58] **Field of Search** 148/1.5, 187; 357/91, 357/23, 44

[56] **References Cited**

U.S. PATENT DOCUMENTS

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4,013,484	3/1977	Boleky et al.	148/1.5
4,016,594	4/1977	Shappir	357/41
4,033,797	7/1977	Dill et al.	148/187
4,035,207	7/1977	Meusburger et al.	156/628
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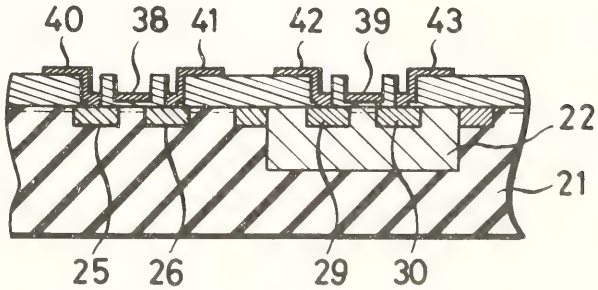
4,046,606	9/1977	Lambert	148/187
4,074,301	2/1978	Paivinen et al.	357/23
4,104,784	8/1978	Klein	29/571
4,108,686	8/1978	Jacobus, Jr.	148/1.5
4,139,402	2/1979	Steinmaier et al.	148/188
4,151,635	5/1979	Kashkogli et al.	29/571

Primary Examiner—R. Dean
Assistant Examiner—Upendra Roy
Attorney, Agent, or Firm—W. G. Fasse; D. F. Gould

[57] **ABSTRACT**

A semiconductor substrate of an N type is formed partially of a well region of a P type by means of a first ion implantation process, then subjected to selective diffusion to form source and drain regions of a P type on the surface of the original substrate, whereby a first insulated gate field effect transistor is formed, and further subjected to selective diffusion to form source and drain region of an N type in the well, whereby a second insulated gate field effect transistor is formed. The semiconductor device is then subjected to a second ion implantation process such that an impurity of an N type is simultaneously ion implanted in the substrate surface surrounding at least the first field effect transistor and the channel region of the second field effect transistor, and is then subjected to formation of an insulation film such that a thick insulation film is formed on the surface of the original substrate and the well, while a thin gate insulation film is formed on the channel regions of the first and second field effect transistors. Then the device is further subjected to a third ion implantation process such that an impurity of a P type is ion planted to the channel regions of the first and second field effect transistors through the thin gate insulation films.

6 Claims, 11 Drawing Figures



United States Patent [19]

Svedberg

[11] **4,224,634**

[45] **Sep. 23, 1980**

[54] **EXTERNALLY CONTROLLED SEMICONDUCTOR DEVICES WITH INTEGRAL THYRISTOR AND BRIDGING FET COMPONENTS**

[75] Inventor: **Per Svedberg**, Vällingby, Sweden

[73] Assignee: **ASEA Aktiebolag**, Vesteras, Sweden

[21] Appl. No.: **691,618**

[22] Filed: **Jun. 1, 1976**

[30] **Foreign Application Priority Data**

Jun. 19, 1975 [SE] Sweden 7507080

[51] **Int. Cl.**[2] **H01L 29/74**

[52] **U.S. Cl.** ..... **357/38**; 357/23; 357/30; 357/39; 357/43; 357/86; 307/252 C

[58] **Field of Search** ..... 357/38, 30, 22, 42, 357/43, 39, 238 C; 307/252 C, 238

[56] **References Cited**

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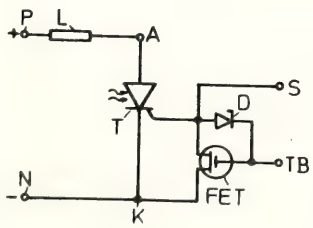
Primary Examiner—Joseph E. Clawson, Jr.
Attorney, Agent, or Firm—Watson, Cole, Grindle & Watson

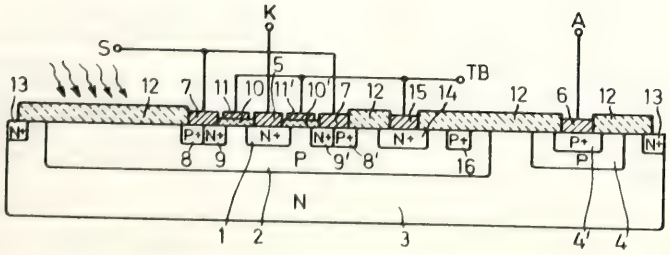
[57] **ABSTRACT**

A semi-conductor device includes a semi-conductor body with four layers of alternate P and N conducting types, these layers constituting a thyristor whose outermost layers form emitter junctions with adjacent layers. The semi-conductor body also includes an integrated field effect transistor part for bridging one of the emitter junctions of the thyristor. The source and drain of the field effect transistor include regions of the same conductivity type, one of which forms the emitter layer adjacent to the bridged emitter junction and the other of which comprises a region ohmically connected to the layer adjacent to the emitter layer and of the same type of conductivity as the emitter layer.

The field effect transistor has a control electrode and a protective diode is provided in the semi-conductor body for limiting voltage between the control electrode of the field effect transistor and the semi-conductor body. The thyristor is arranged for optical ignition.

7 Claims, 9 Drawing Figures





United States Patent [19]

Yundt

[11] **4,199,649**

[45] **Apr. 22, 1980**

[54] **AMORPHOUS MONOMOLECULAR SURFACE COATINGS**

[75] Inventor: **Albert P. Yundt**, Medfield, Mass.

[73] Assignee: **Bard Laboratories, Inc.**, Amherst, N.H.

[21] Appl. No.: **895,754**

[22] Filed: **Apr. 12, 1978**

[51] **Int. Cl.**[2] **B32B 9/04**

[52] **U.S. Cl.** ..... **428/411**; 148/33; 148/33.3; 204/159.13; 260/18 S; 354/354; 357/40; 427/82; 427/96; 427/259; 427/385.5; 427/386; 427/387; 427/407.2; 427/409; 428/426; 428/429; 428/441; 428/449; 428/451; 427/53.1; 427/412.1; 430/5; 430/319; 430/327

[58] **Field of Search** ..... 427/54, 82, 96, 259, 427/407 A, 407 C, 409, 385 R, 386, 387; 428/429, 411, 441, 426, 447, 451; 204/159.13, 159.14; 96/35.1, 36.2, 67, 86 R, 86 P; 260/18 S, 46.5 G, 46.5 R; 354/354; 357/40; 148/33, 33.3

[56] **References Cited**

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3,942,982	3/1976	Yanazawa et al.	96/36.2 X
4,001,870	1/1977	Saiki et al.	427/82 X

Primary Examiner—John D. Smith
Assistant Examiner—Thurman K. Page
Attorney, Agent, or Firm—Fitch, Even & Tabin

[57] **ABSTRACT**

The self-aligning characteristics of surface-active molecules are used to provide a multiply-coupled thin film surface coating on a substrate, comprising an outermost layer of normally fluid, flexible backbone chain polymer units of at least about 30 atoms in length, the ends of which are attached by chemical bonds to a relatively highly polar second layer of atoms serving to anchor the relatively fluid outer surface layer polymer chains to the surface of the substrate.

22 Claims, No Drawings

United States Patent [19]
Ruetsch et al.
[11] **4,231,054**
[45] **Oct. 28, 1980**

[54] **THYRISTOR WITH STARTING AND GENERATING CATHODE BASE CONTACTS FOR USE IN RECTIFIER CIRCUITS**

[75] Inventors: **Christian Ruetsch**, Turgi; **Roland Sittig**, Umiken, both of Switzerland

[73] Assignee: **BBC Brown, Boveri & Company, Limited**, Baden, Switzerland

[21] Appl. No.: **41,332**

[22] Filed: **May 22, 1979**

[30] **Foreign Application Priority Data**

Jun. 15, 1978 [CH] Switzerland 6522/78

[51] **Int. Cl.**[2] **H01L 29/74**

[52] **U.S. Cl.** ..... **357/38**; 357/51; 357/55; 357/86; 307/252 G; 307/252 K

[58] **Field of Search** ..... 357/38, 51, 55, 86; 307/252 G, 252 K

[56] **References Cited**

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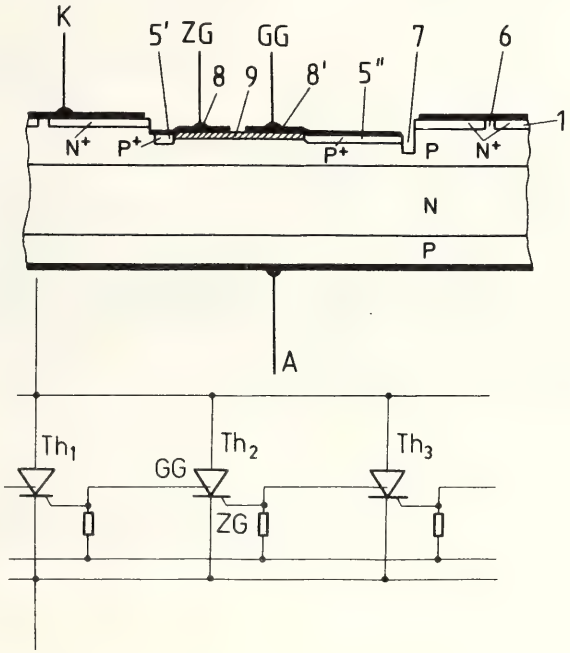
3,740,584	6/1973	McIntyre et al.	307/252 G

Primary Examiner—Joseph E. Clawson, Jr.
Attorney, Agent, or Firm—Oblon, Fisher, Spivak, McClelland & Maier

[57] **ABSTRACT**

An output thyristor with at least two electrodes located on the cathode side base zone, whereby one of the two electrodes is used as a control electrode (starting gate) and the second electrode is used for the output of current (generator gate), wherein the existing lateral resistance R_{GK}' between the generator gate and the cathode zone and/or the edge length of the generator gate is selected such that at the generator gate of the started thyristor, with an anode current which is smaller than the surge limit of the thyristor in question, the current I_G removable therefrom is sufficient when applied to the starting gate of a corresponding thyristor connected in parallel to start the parallel connected thyristor. The lateral resistance between the starting gate and the cathode zone—R_{GK}—is selected as small as possible ($R_{GK} < R_{GK}'$) so that the starting voltage on the starting gate can act directly on the semiconductor junction between the thyristor cathode zone and the cathode base zone.

8 Claims, 5 Drawing Figures



United States Patent [19]
Corwin et al.
[11] **4,199,377**
[45] **Apr. 22, 1980**

[54] **SOLAR CELL**

[75] Inventors: **Rudolph E. Corwin**, Seattle; **Dietrich E. Riemer**, Auburn, both of Wash.

[73] Assignee: **The Boeing Company**, Seattle, Wash.

[21] Appl. No.: **16,245**

[22] Filed: **Feb. 28, 1979**

[51] **Int. Cl.**[2] **H01L 31/06**; H01L 21/223; H01L 21/76

[52] **U.S. Cl.** ..... **136/89 SJ**; 29/572; 136/89 CC; 148/187; 148/188; 357/30; 357/52

[58] **Field of Search** ..... 136/89 CC, 89 SJ, 89 SG; 357/30, 52; 29/572; 148/187, 188

[56] **References Cited**

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3,156,593	11/1964	Ligenza	148/187
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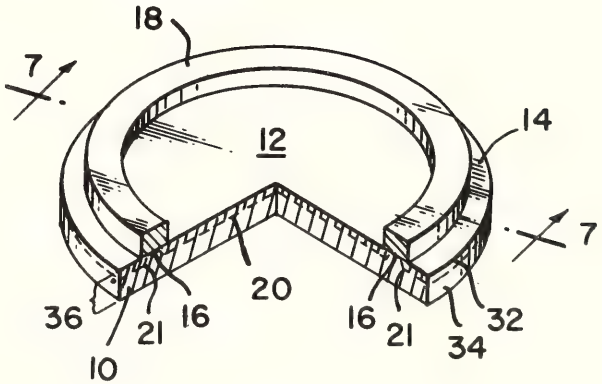
H. M. Demsky et al., "Technique for Counteracting Epitaxial Autodoping," *IBM Tech. Disc Bull.*, vol. 13, pp. 807-808 (1970).

Primary Examiner—Aaron Weisstuch
Attorney, Agent, or Firm—David G. Pursel; Robert L. Gullette

[57] **ABSTRACT**

A solar cell including a dielectric isolation member to electrically isolate an active region of the cell from the unfinished edge thereof and to protect the p-n junction from surface contaminants. The isolation member is fabricated on top of a semiconductor wafer before diffusion.

14 Claims, 8 Drawing Figures



United States Patent [19]

Lalumia et al.

[11] 4,228,448

[45] Oct. 14, 1980

[54] BIPOLAR INTEGRATED SEMICONDUCTOR STRUCTURE INCLUDING I²L AND LINEAR TYPE DEVICES AND FABRICATION METHODS THEREFOR

[75] Inventors: **Thomas M. Lalumia; James N. Fordemwalt**, both of Tucson, Ariz.

[73] Assignee: **Burr Brown Research Corp.**, Tucson, Ariz.

[21] Appl. No.: **840,397**

[22] Filed: **Oct. 7, 1977**

[51] **Int. Cl.**³ **H01L 27/02**

[52] **U.S. Cl.** **357/46**; 357/48; 357/92

[58] **Field of Search** 357/92, 40, 46, 48

[56] **References Cited**

U.S. PATENT DOCUMENTS

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4,087,900	5/1978	Yiannoulos	357/92

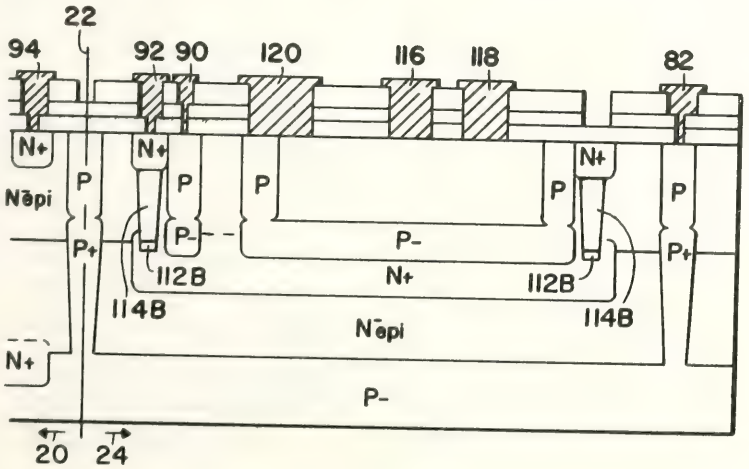
Primary Examiner—Edward J. Wojciechowicz

Attorney, Agent, or Firm—Harry M. Weiss

[57] **ABSTRACT**

This disclosure relates to a bipolar integrated semiconductor structure that has incorporated therein both I²L and linear type bipolar devices. The integrated structure utilizes a double epitaxial layer deposited or formed on a starting substrate wherein at least one linear type bipolar device is incorporated in one portion of the final integrated structure and at least one I²L bipolar device is incorporated in another portion of the final double epitaxial layer integrated structure. For the linear type bipolar device, the subcollector region is selectively located between the starting substrate and the first epitaxial layer whereas for the I²L bipolar device, the sub-emitter region is selectively located between the first and the second epitaxial layers. Other features of the bipolar integrated semiconductor structure include polysilicon isolation for the I²L and linear devices, up and down diffused PN junction isolation type regions, up-diffused base region for the I²L device, Schottky type collectors for the I²L device, up and down diffused base regions for the I²L device isolate the collector contacts, and the use of another subcollector region selectively located between the first and the second epitaxial layer in the linear portion of the integrated semiconductor structure which functions to improve the current gain of the lateral PNP linear transistor device.

29 Claims, 7 Drawing Figures



United States Patent [19]

Yariv et al.

[11] 4,212,020

[45] Jul. 8, 1980

[54] SOLID STATE ELECTRO-OPTICAL DEVICES ON A SEMI-INSULATING SUBSTRATE

[75] Inventors: **Amnon Yariv**, San-Marino; **Shlomo Margalit; Chien-Ping Lee**, both of Pasadena, all of Calif.

[73] Assignee: **California Institute of Technology**, Pasadena, Calif.

[21] Appl. No.: **926,649**

[22] Filed: **Jul. 21, 1978**

[51] **Int. Cl.**² **H01L 33/00**

[52] **U.S. Cl.** ..... **357/17**; 357/18; 357/4; 357/41; 331/94.5 H

[58] **Field of Search** ..... 357/18, 17, 41, 4; 331/94.5 H

[56] **References Cited**

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3,982,207	9/1976	Dingle	331/94.5 H
3,990,096	11/1976	Naimizaki	357/18

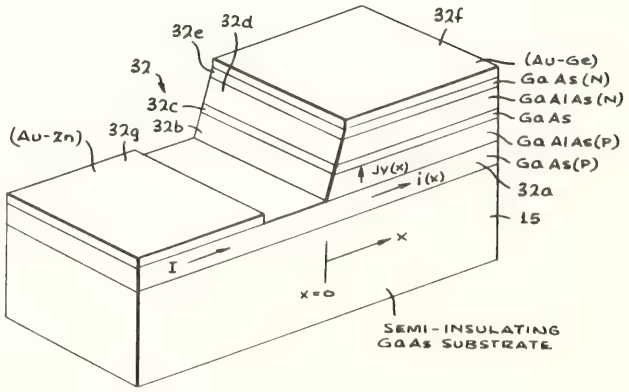
Primary Examiner—Martin H. Edlow

Attorney, Agent, or Firm—Freilich, Hornbaker, Wasserman, Rosen & Fernandez

[57] **ABSTRACT**

Solid state electro-optical devices are formed on a semi-insulating substrate, with all contacts of each device being on the same side of the substrate. These devices include two types of lasers, one operating on current crowding effect and the other by lateral diffusions. Either type laser is integratable with an electronic device e.g. a Gunn oscillator or an FET on the common semi-insulating substrate to form a complex monolithic electro-optical device.

11 Claims, 19 Drawing Figures



United States Patent [19]
Darwish et al.
[11] **4,205,342**
[45] **May 27, 1980**

[54] **INTEGRATED CIRCUIT STRUCTURE HAVING REGIONS OF DOPING CONCENTRATION INTERMEDIATE THAT OF A SUBSTRATE AND A POCKET FORMED THEREIN**

[75] Inventors: **Mougahed Y. Darwish**, Fontaines; **Henri J. Oguey**, Corcelles, both of Switzerland

[73] Assignee: **Centre Electronique Horologer S. A.**, Neuchatel, Switzerland

[21] Appl. No.: **898,681**

[22] Filed: **Apr. 21, 1978**

[30] **Foreign Application Priority Data**

May 5, 1977 [CH] Switzerland 5637/77

[51] **Int. Cl.**[2] **H01L 29/78**; H01L 27/04; H01L 21/22

[52] **U.S. Cl.** **357/23**; 357/20; 357/42; 357/51; 357/89; 148/187

[58] **Field of Search** 357/20, 89, 41, 42, 357/23, 51, 14

[56] **References Cited**

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3,821,776	6/1974	Hayashi et al.	357/42
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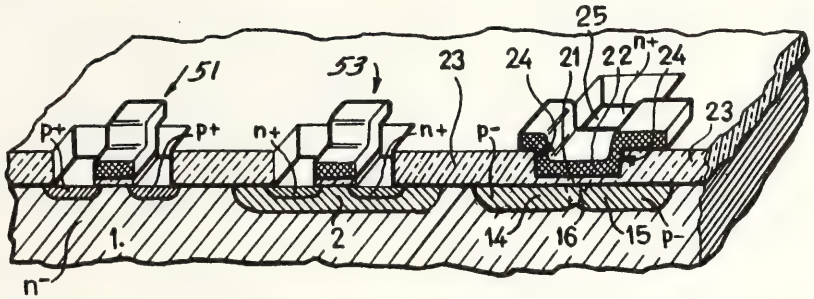
3,967,295	6/1976	Stewart	357/41

Primary Examiner—William D. Larkins
Attorney, Agent, or Firm—Stevens, Davis, Miller & Mosher

[57] **ABSTRACT**

A CMOS integrated circuit structure is provided having circuit elements which can function as high resistances or stable current sources. The circuit elements include a region of intermediate doping which has a surface concentration between that of a substrate and a homogeneous region of a doped pocket formed therein. The region of intermediate doping is formed by the vicinity of two pocket edges, these edges being separated by a distance which is substantially not greater than twice the length of the lateral diffusion of the doping of the pockets.

4 Claims, 14 Drawing Figures



United States Patent [19]
Wickenden
[11] **4,182,025**
[45] **Jan. 8, 1980**

[54] **MANUFACTURE OF ELECTROLUMINESCENT DISPLAY DEVICES**

[75] Inventor: **Dennis K. Wickenden**, London, England

[73] Assignee: **Elliott Brothers (London) Limited**, Chelmsford, England

[21] Appl. No.: **837,611**

[22] Filed: **Sep. 28, 1977**

[30] **Foreign Application Priority Data**

Oct. 7, 1976 [GB] United Kingdom 41744/76

[51] **Int. Cl.**[2] **B01J 17/00**

[52] **U.S. Cl.** ..... **29/577 R**; 29/580; 29/583; 357/45

[58] **Field of Search** ..... 29/577, 580, 583, 576 W; 357/45

[56] **References Cited**

U.S. PATENT DOCUMENTS

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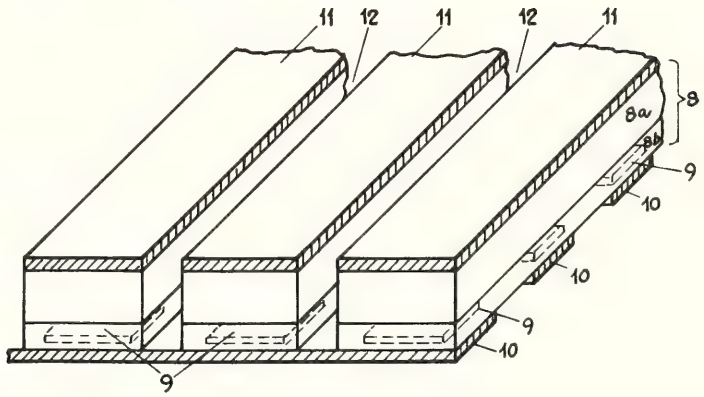
3,673,016	6/1972	Gerstner	29/583
3,781,975	1/1974	Ressel	29/583
3,918,150	11/1975	Gantley	29/583

Primary Examiner—W. C. Tupman
Attorney, Agent, or Firm—Kirschstein, Kirschstein, Ottinger & Cobrin

[57] **ABSTRACT**

In the manufacture of a monolithic light-emitting diode array, electrical isolation between the n-type regions of portions of the array, for example the columns of a matrix array, is effected by mechanically cutting channels between the portions, through the n-type region and the common electrode. This method of forming the isolation channels makes it possible to produce much narrower channels than can be achieved by chemical etching, thus providing a high resolution array.

3 Claims, 4 Drawing Figures



United States Patent [19]

Clark et al.

[11] **4,214,917**

[45] **Jul. 29, 1980**

[54] **PROCESS OF FORMING A SEMICONDUCTOR MEMORY CELL WITH CONTINUOUS POLYSILICON RUN CIRCUIT ELEMENTS**

[75] Inventors: **Kenneth L. Clark**, Pocatello, Id.; **George S. Leach; Robert W. Howard**, both of Phoenix, Ariz.

[73] Assignee: **EMM Semi**, Tempe, Ariz.

[21] Appl. No.: **876,726**

[22] Filed: **Feb. 10, 1978**

[51] **Int. Cl.**[2] **H01L 21/26**; H01L 21/283; H01L 29/78

[52] **U.S. Cl.** ..... **148/1.5**; 29/571; 29/577 C; 29/578; 29/580; 148/174; 148/187; 148/188; 156/653; 156/657; 156/662; 357/23; 357/45; 357/51; 357/59; 357/91; 427/85; 427/86; 427/96; 427/101

[58] **Field of Search** ..... 148/174, 187, 188, 1.5; 29/571, 576 C, 577, 578, 580; 427/85, 86, 88, 96, 101; 156/653, 657, 662; 357/23, 45, 51, 59, 91

[56] **References Cited**

U.S. PATENT DOCUMENTS

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3,825,442	7/1974	Moore	357/23 X
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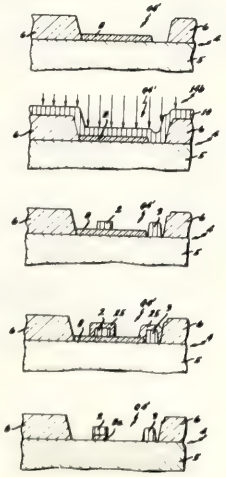
3,891,190	6/1975	Vadasz	357/59 X
4,055,444	10/1977	Rao	148/1.5
4,092,735	5/1978	McElroy	357/59 X
4,110,776	8/1978	Rao et al.	357/59 X
4,133,000	1/1979	Greenstein	357/51 X
4,139,785	2/1979	McElroy	357/59 X
4,139,786	2/1979	Raymond et al.	357/59 X

Primary Examiner—R. Dean
Assistant Examiner—W. G. Saba
Attorney, Agent, or Firm—Harry M. Weiss

[57] **ABSTRACT**

A process is described for forming a plurality of polysilicon runs on the surface of a semiconductor substrate, such as a silicon substrate, at least one of the polysilicon runs having a resistor portion formed therein, and at least one of the polysilicon runs forming the conductive gate electrode of a self-aligned insulated silicon gate field effect device. A specific embodiment of the process involves forming protective oxide layer on the substrate with depressions or wells therein to define active area regions of field effect devices, depositing a layer of polysilicon to overly the protective oxide layers, implanting dopant ions in the polysilicon layer to establish an initial conductivity of the polysilicon corresponding to resistor material, patterning the polysilicon layer to define desired polysilicon runs, with at least one of the polysilicon runs traversing across the gate region and gate oxide of a field effect device to serve as the gate electrode thereof; establishing an oxide layer over the surface and then removing oxide to both expose the active areas of the field effect devices where not protected by the polysilicon gate electrodes and also to define a remaining resistor mask of the oxide which overlies and protects the resistor portions of the polysilicon runs; and applying dopant to render the unprotected portions of the polysilicon runs highly conductive relative to the oxide masked resistor portions thereof and to simultaneously dope the exposed active areas of field effect devices.

9 Claims, 28 Drawing Figures



United States Patent [19]

Marciniec

[11] **4,206,541**

[45] **Jun. 10, 1980**

[54] **METHOD OF MANUFACTURING THIN FILM THERMAL PRINT HEADS**

[75] Inventor: **Edmund T. Marciniec**, Chicago, Ill.

[73] Assignee: **Extel Corporation**, Northbrook, Ill.

[21] Appl. No.: **918,845**

[22] Filed: **Jun. 26, 1978**

[51] **Int. Cl.**[2] **H05B 3/16**

[52] **U.S. Cl.** ..... **29/611**; 29/620; 101/1; 156/656; 156/657; 156/663; 204/15; 219/216; 346/76 PH

[58] **Field of Search** ..... 204/192 E, 192 R, 32 S, 204/32 R, 15; 346/76 PH; 101/1; 219/216; 156/656, 657, 663; 29/611, 620

[56] **References Cited**

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3,973,106	8/1976	Ura	219/216
4,007,352	2/1976	Ura	29/611
4,030,408	6/1977	Miwa	219/216
4,038,517	7/1977	Nelson	219/216
4,059,480	11/1977	Ruh	156/663

FOREIGN PATENT DOCUMENTS

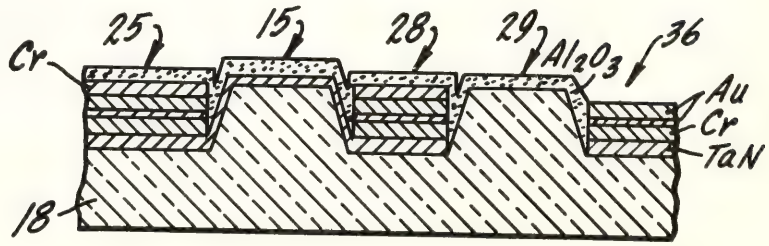
2537142	5/1976	Fed. Rep. of Germany	219/216

Primary Examiner—Jerome W. Massie
Attorney, Agent, or Firm—Kinzer, Plyer, Dorn & McEachran

[57] **ABSTRACT**

A dielectric substrate for a thin film dot matrix thermal print head has its working surface etched or otherwise treated to selectively remove the dielectric material, in all areas which will constitute electrical connectors for the resistance heater print elements, to a depth at least equal to the sum of the thicknesses of all of the conductive films to be applied to the substrate surface in those areas, following which the working surface of the substrate is selectively coated with films of high-resistance electrically conductive material and low-resistance conductive material, with suitable adhesion films as required, to complete the print head. An outer protective wear-resistant film is also employed. The resultant print head has its resistance heater print elements and blank surface elements raised at least to the same level as the outer surfaces of the electrical connectors, and preferably slightly higher, to provide improved performance and operating life.

10 Claims, 6 Drawing Figures



United States Patent [19]

Kane

[11] **4,223,335**

[45] **Sep. 16, 1980**

[54] **SEMICONDUCTOR DEVICE BODY HAVING IDENTICAL ISOLATED COMPOSITE RESISTOR REGIONS**

[75] Inventor: **Jeffrey Kane**, Cheadle Hulme, England

[73] Assignee: **Ferranti Limited**, Hollinwood, England

[21] Appl. No.: **18,985**

[22] Filed: **Mar. 9, 1979**

Related U.S. Application Data

[63] Continuation of Ser. No. 784,464, Apr. 4, 1977, abandoned.

[30] **Foreign Application Priority Data**

Aug. 2, 1975 [GB] United Kingdom 32402/75

[51] **Int. Cl.**[2] **H01L 27/04**; H01L 29/12; H01L 27/02

[52] **U.S. Cl.** **357/48**; 357/47; 357/34; 357/36; 357/51

[58] **Field of Search** 357/34, 36, 47, 48, 357/51

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,766,449	10/1973	Bruchez	357/36
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3,827,034	7/1974	Colaco	357/48
3,922,707	11/1975	Freed et al.	357/48
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3,990,092	11/1976	Yoshimura	357/51
4,013,971	3/1977	Sternbeck	357/51
4,049,975	9/1977	Colaco	357/36
4,053,336	10/1977	Grundy et al.	357/48
4,161,742	7/1979	Kane	357/51

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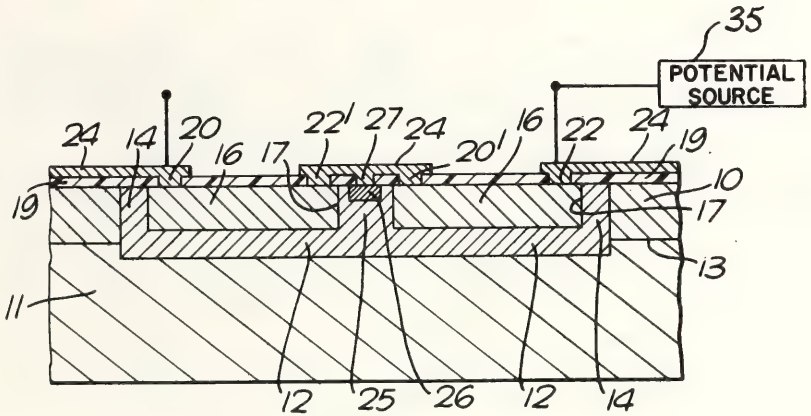
1405285	9/1975	United Kingdom	357/34

Primary Examiner—Andrew J. James
Attorney, Agent, or Firm—Kerkam, Stowell, Kondracki & Clarke

[57] **ABSTRACT**

A resistor comprises two identical resistor regions with each resistor region isolated within the semiconductor body by a P-N junction, and with one electrode-bearing end of each resistor region both connected together and to a common region surrounding the resistor regions within the semiconductor body, so that the common surrounding region is to be at the same potential level as the mid-point of the resistor considered as a whole.

4 Claims, 3 Drawing Figures



United States Patent [19]

Smith

[11] **4,193,126**

[45] **Mar. 11, 1980**

[54] **I²L RAM UNIT**

[75] Inventor: **Kent F. Smith**, Salt Lake City, Utah

[73] Assignee: **General Instrument Corporation**, Clifton, N.J.

[21] Appl. No.: **966,020**

[22] Filed: **Dec. 4, 1978**

[51] **Int. Cl.**[2] **G11C 11/40**

[52] **U.S. Cl.** **365/174**; 357/45; 365/154

[58] **Field of Search** 365/154, 174, 178, 179; 357/40, 45, 46

[56] **References Cited**

U.S. PATENT DOCUMENTS

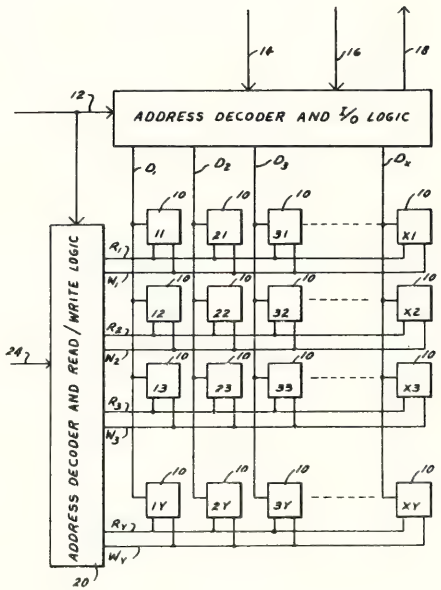
3,177,374	4/1965	Simonian	365/174

Primary Examiner—Terrell W. Fears
Attorney, Agent, or Firm—James and Franklin

[57] **ABSTRACT**

The memory unit comprises a plurality of bipolar inverter transistors and an equal number of injector transistors, each of which acts as a current source for a different one of the inverter transistors. Means are provided for cross-coupling a first and a second of the inverter transistors to form a flip-flop. Third, fourth and fifth inverter transistors provide input data flow from the data line to the cross-coupled first and second inverters, in accordance with a write control sixth inverter transistor connected to receive a write signal. A seventh inverter transistor provides data output flow between the cross-coupled first and second inverter transistors and the data line in accordance with the read control eighth inverter transistor connected to receive a read signal.

13 Claims, 3 Drawing Figures



United States Patent [19]

White

[11] **4,206,470**

[45] **Jun. 3, 1980**

[54] **THIN FILM INTERCONNECT FOR MULTICOLOR IR/CCD**

[75] Inventor: **William J. White**, Chelmsford, Mass.

[73] Assignee: **Honeywell Inc.**, Minneapolis, Minn.

[21] Appl. No.: **961,803**

[22] Filed: **Nov. 17, 1978**

Related U.S. Application Data

[62] Division of Ser. No. 829,744, Sep. 1, 1977.

[51] **Int. Cl.**[2] **H01L 27/14**

[52] **U.S. Cl.** **357/30**; 357/40; 357/45; 357/41; 357/65; 357/24

[58] **Field of Search** 357/30, 24, 40, 45, 357/65, 41

[56] **References Cited**

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3,996,599	12/1976	King	357/30
4,093,957	6/1978	King	357/24
4,106,046	8/1978	Nathanson	357/30
4,142,198	2/1979	Finnila	357/24
4,148,052	4/1979	Nathanson	357/30

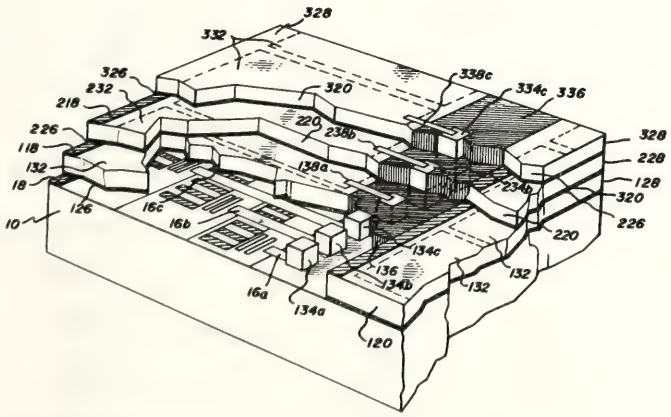
Primary Examiner—Martin H. Edlow

Attorney, Agent, or Firm—Theodore F. Neils; David R. Fairbairn

[57] **ABSTRACT**

A hybrid mosaic IR/CCD focal plane structure is fabricated using planar thin film interconnects. Rows of detectors are formed on an integrated circuit substrate so that the rows of detectors are adjacent to rows of electrical contacts on the integrated circuit. Contact pads are plated onto the rows of contacts and the regions between adjacent rows of detectors are backfilled with an insulating material. The insulating material is then lapped to expose the contact pads and to form an essentially coplanar surface with the detectors. Thin film interconnects are formed over the coplanar surface between the exposed contact pads and detectors in the adjacent row.

1 Claim, 9 Drawing Figures



United States Patent [19]

Nelson

[11] **4,188,610**

[45] **Feb. 12, 1980**

[54] **METHOD OF AND APPARATUS FOR THE GENERATION AND TRANSMISSION OF SIGNALS FOR ECHOLOCATION AND OTHER SIGNALLING PURPOSES, SUCH AS IN GEOPHYSICAL EXPLORATION**

[75] Inventor: **David E. Nelson**, Rochester, N.Y.

[73] Assignee: **Hydroacoustics, Inc.**, Rochester, N.Y.

[21] Appl. No.: **828,698**

[22] Filed: **Aug. 29, 1977**

[51] **Int. Cl.**[2] **G01V 1/14**; G01V 1/28

[52] **U.S. Cl.** ..... **367/14**; 343/17.2 PC; 367/42; 367/23

[58] **Field of Search** ..... 340/15.5 TA, 15.5 CC, 340/15.5 SC; 343/17.2 PC

[56] **References Cited**

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3,326,320	6/1967	Forester	340/15.5 TA
4,004,267	1/1977	Mayne	340/15.5 CP
4,037,190	7/1977	Martin	340/15.5 TA
4,047,173	9/1977	Miller	343/17.2 PC

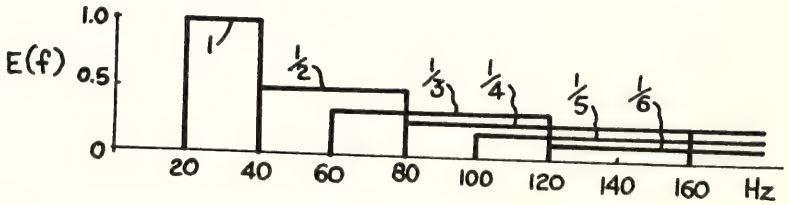
Primary Examiner—Nelson Moskowitz

Attorney, Agent, or Firm—Martin LuKacher

[57] **ABSTRACT**

Methods and apparatus are described for generating and transmitting signals in accordance with a sequence which defines the time relationship of the signals. Each signal has a band width covering several octaves and may be a pulse. During a transmission interval the repetition frequencies of the signals monotonically sweep in a coherent relationship over bands restricted to an octave such that the spectrum of the sequence has substantially constant energy over a frequency range much larger than an octave. The autocorrelation function of the sequence is characterized by an absence of side lobes which would indicate false targets or produce a high noise level upon processing of the signals in an echolocation system, such as a geophysical exploration system in which the seismograms are constructed by cross correlation of the signals which are received from the geological reflection surfaces with a stored replica of the transmitted signals. The signals can be generated by a plurality of sources all of which operate during the transmission interval, thus enabling the transmission of increased energy into the medium (viz., the seismic signal power injected into the earth).

87 Claims, 23 Drawing Figures



United States Patent [19]
Frohman-Bentchkowsky et al.
[11] **4,203,158**
[45] **May 13, 1980**

[54] **ELECTRICALLY PROGRAMMABLE AND ERASABLE MOS FLOATING GATE MEMORY DEVICE EMPLOYING TUNNELING AND METHOD OF FABRICATING SAME**

[75] Inventors: **Dov Frohman-Bentchkowsky**, Haifa, Israel; **Jerry Mar**, Sunnyvale, Calif.; **George Perlegos**, Cupertino, Calif.; **William S. Johnson**, Palo Alto, Calif.

[73] Assignee: **Intel Corporation**, Santa Clara, Calif.

[21] Appl. No.: **969,819**

[22] Filed: **Dec. 15, 1978**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 881,029, Feb. 24, 1978, abandoned.

[51] **Int. Cl.**[2] **G11C 11/40**
[52] **U.S. Cl.** **365/185**; 307/238; 357/41
[58] **Field of Search** 365/185, 189; 307/238; 357/41, 45, 304

[56] **References Cited**

U.S. PATENT DOCUMENTS

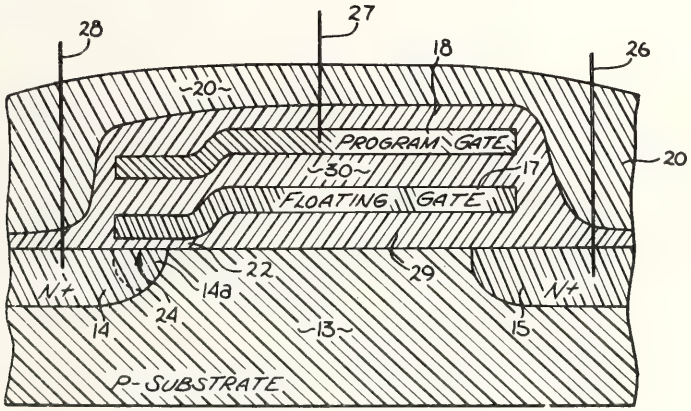
3,500,142	3/1970	Kahng	365/185
4,051,464	9/1977	Huang	365/185

Primary Examiner—Terrell W. Fears
Attorney, Agent, or Firm—Blakely, Sokoloff, Taylor & Zafman

[57] **ABSTRACT**

An electrically programmable and electrically erasable MOS memory device suitable for high density integrated circuit memories is disclosed. Carriers are tunneled between a floating conductive gate and a doped region in the substrate to program and erase the device. A minimum area of thin oxide (70 Å–200 Å) is used to separate this doped region from the floating gate. In one embodiment, a second layer of polysilicon is used to protect the thin oxide region during certain processing steps.

16 Claims, 14 Drawing Figures



United States Patent [19]
Adam
[11] **4,196,441**
[45] **Apr. 1, 1980**

[54] **SEMICONDUCTOR STORAGE CELL**

[75] Inventor: **Fritz G. Adam**, Freiburg, Fed. Rep. of Germany

[73] Assignee: **ITT Industries, Inc.**, New York, N.Y.

[21] Appl. No.: **903,359**

[22] Filed: **May 5, 1978**

[30] **Foreign Application Priority Data**

May 26, 1977 [DE] Fed. Rep. of Germany 2723738

[51] **Int. Cl.**[2] **H01L 27/02**
[52] **U.S. Cl.** **357/41**; 357/23; 357/45; 357/54
[58] **Field of Search** 357/23, 41, 54

[56] **References Cited**

U.S. PATENT DOCUMENTS

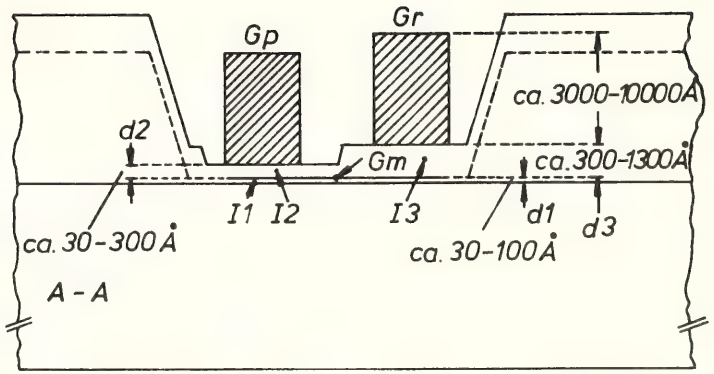
3,836,894	9/1974	Cricchi	357/54
4,063,267	12/1977	Hsia	357/54

Primary Examiner—Edward J. Wojciechowicz
Attorney, Agent, or Firm—John T. O'Halloran; Peter C. Van Der Sluys

[57] **ABSTRACT**

A programmable nonvolatile FET storage cell comprising crosswise to the ribbonlike source region as well as to the drain region a ribbonlike reading electrode and a separate ribbonlike writing electrode. Both electrodes are disposed upon a gate insulator layer into which a storage medium is embedded which is common to both electrodes.

35 Claims, 10 Drawing Figures



United States Patent [19]

Ohki

[11] **4,216,490**

[45] **Aug. 5, 1980**

[54] **STATIC INDUCTION TRANSISTOR**

[75] Inventor: **Toshimi Ohki**, Tokyo, Japan

[73] Assignee: **Kabushiki Kaisha Daini Seikosha**, Tokyo, Japan

[21] Appl. No.: **891,286**

[22] Filed: **Mar. 28, 1978**

[30] **Foreign Application Priority Data**

Mar. 31, 1977 [JP] Japan 52-36775

[51] **Int. Cl.**[2] **H01L 27/02**

[52] **U.S. Cl.** **357/43**; 357/22; 357/89; 357/90; 357/92; 357/41

[58] **Field of Search** 357/22, 23, 41, 43, 357/89, 90, 92

[56] **References Cited**

U.S. PATENT DOCUMENTS

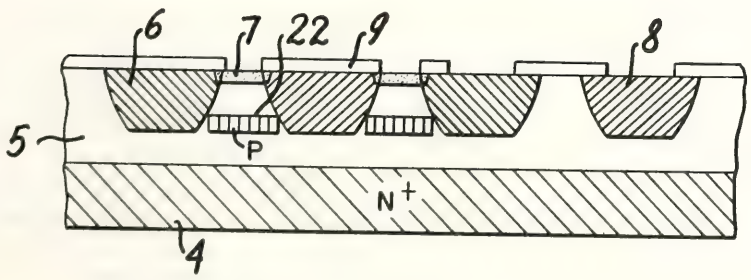
4,067,036	1/1978	Yoshida	357/22
4,086,611	4/1978	Nishizawa	357/38
4,115,793	9/1978	Nishizawa	357/22

Primary Examiner—Martin H. Edlow
Attorney, Agent, or Firm—Robert E. Burns; Emmanuel J. Lobato; Bruce L. Adams

[57] **ABSTRACT**

A static induction transistor having a channel region between a gate region and a source region of the transistor. Current flowing from the drain region to the source region through the channel region is controlled by a voltage applied to the gate region. An impurity region having a conductivity type opposite that of the channel region is formed in the channel region and is effective to decrease the channel current which will flow when the gate region is biased by a low voltage.

6 Claims, 13 Drawing Figures



United States Patent [19]

Bergmann et al.

[11] **4,197,147**

[45] **Apr. 8, 1980**

[54] **METHOD OF MANUFACTURING AN INTEGRATED CIRCUIT INCLUDING AN ANALOG CIRCUIT AND AN I²L CIRCUIT UTILIZING STAGED DIFFUSION TECHNIQUES**

[75] Inventors: **Günther Bergmann**, Blaustein-Arnegg; **Hermann Clauss**, Leingarten, both of Fed. Rep. of Germany

[73] Assignee: **Licentia Patent-Verwaltungs-G.m.b.H**, Frankfurt am Main, Fed. Rep. of Germany

[21] Appl. No.: **893,521**

[22] Filed: **Apr. 4, 1978**

[30] **Foreign Application Priority Data**

Apr. 5, 1977 [DE] Fed. Rep. of Germany 2715158

[51] **Int. Cl.**[2] **H01L 21/22**; H01L 27/04; H01L 29/72

[52] **U.S. Cl.** ..... **148/175**; 29/577 C; 29/578; 148/1.5; 148/187; 357/35; 357/36; 357/44; 357/46; 357/92

[58] **Field of Search** 148/1.5, 175, 187; 29/577, 578; 357/35, 36, 44, 46, 92

[56] **References Cited**

U.S. PATENT DOCUMENTS

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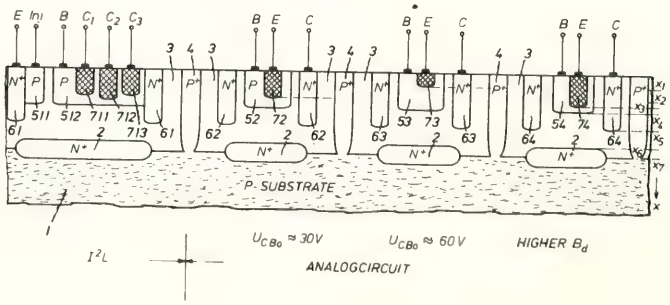
Berger et al., "Integrated Transistor . . . Variable-Current Amplification" I.B.M. Tech. Discl. Bull., vol. 15, No. 5, Oct. 1972, p. 1625.

Primary Examiner—R. Dean
Assistant Examiner—W. G. Saba
Attorney, Agent, or Firm—Spencer & Kaye

[57] **ABSTRACT**

A method of manufacturing an integrated circuit including an analog circuit and an I²L circuit which both contain NPN transistors on a P-type semiconductor chip in which the method includes an N+ diffusion step for producing a flat diffusion for certain NPN transistors having smaller penetration depth than N+ regions of the other NPN transistors for connection of an emitter electrode to the said certain NPN transistors.

5 Claims, 4 Drawing Figures



United States Patent [19]
Mihashi et al.
[11] **4,210,466**
[45] **Jul. 1, 1980**

[54] **PROCESS FOR PREPARING HEAT SENSITIVE SEMICONDUCTOR SWITCH**

[75] Inventors: **Yutaka Mihashi; Josuke Nakata,** both of Itami, Japan

[73] Assignee: **Mitsubishi Denki Kabushiki Kaisha,** Tokyo, Japan

[21] Appl. No.: **966,627**

[22] Filed: **Dec. 5, 1978**

[30] **Foreign Application Priority Data**

Dec. 5, 1977 [JP] Japan 52-146245

[51] **Int. Cl.**[2] **H01L 23/56;** H01L 29/66; H01L 21/263

[52] **U.S. Cl.** **148/1.5;** 357/28; 357/38; 357/91

[58] **Field of Search** 148/1.5; 357/28, 38, 357/39, 91

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,971,056	7/1976	Jaskolski et al.	357/28
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4,081,818	3/1978	Nakata	357/28
4,112,458	9/1978	Jaskolski et al.	357/38
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4,134,778	1/1979	Sheng et al.	148/1.5

FOREIGN PATENT DOCUMENTS

50-146283 11/1975 Japan .

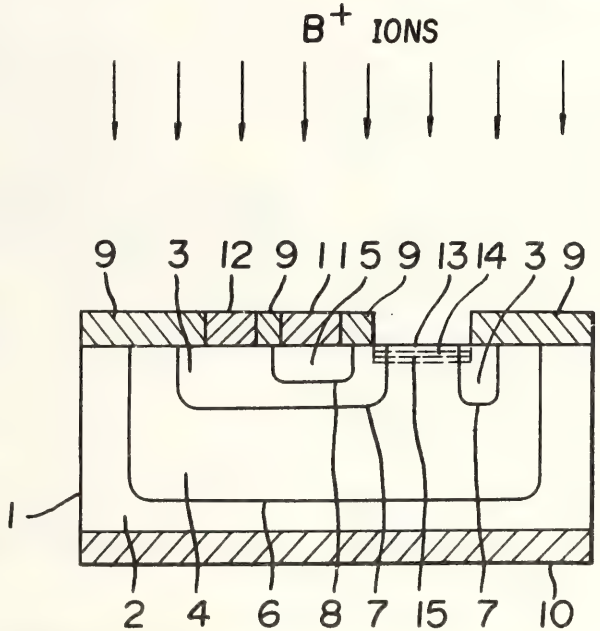
Primary Examiner—R. Dean
Assistant Examiner—Roy Upendra
Attorney, Agent, or Firm—Oblon, Fisher, Spivak, McClelland & Maier

[57] **ABSTRACT**

A process for preparing heat sensitive semiconductor switch which switches from OFF state to ON state at relatively low temperature.

In a heat sensitive thyristor having PNPN four layer structure, an N type base region is exposed at one part of the surface exposed part in the P type base region to form an opening and ions of a P type impurity such as boron, aluminum and gallium are implanted from the opening to form a part having a large leakage current in a collector junction under excellent control, and to provide lower switching temperature for switching from the OFF state to the ON state with high reproducibility.

3 Claims, 4 Drawing Figures



United States Patent [19]
Priel et al.
[11] **4,228,451**
[45] **Oct. 14, 1980**

[54] **HIGH RESISTIVITY SEMICONDUCTOR RESISTOR DEVICE**

[75] Inventors: **Ury Priel,** Cupertino; **Jerry D. Gray,** San Jose; **Allen H. Frederick,** Pacifica, all of Calif.

[73] Assignee: **Monolithic Memories, Inc.,** Sunnyvale, Calif.

[21] Appl. No.: **926,856**

[22] Filed: **Jul. 21, 1978**

Related U.S. Application Data

[62] Division of Ser. No. 805,534, Jun. 10, 1977, Pat. No. 4,152,627.

[51] **Int. Cl.**[3] **H01L 27/02;** H01L 29/78; H01L 29/72; H01C 1/012

[52] **U.S. Cl.** **357/51;** 357/23; 357/34; 357/35; 357/48; 357/91; 338/314

[58] **Field of Search** 357/51, 91; 338/308, 338/314

[56] **References Cited**

U.S. PATENT DOCUMENTS

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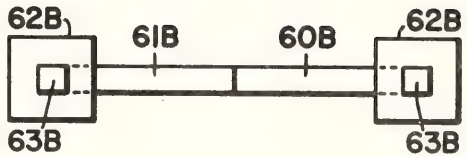
3,947,866	3/1976	Stellrecht	357/51
4,001,869	1/1977	Brown	357/51
4,021,270	5/1977	Hupt et al.	357/91
4,034,395	7/1977	Abdelrahman	357/51

Primary Examiner—Gene M. Munson
Attorney, Agent, or Firm—Harry M. Weiss

[57] **ABSTRACT**

This disclosure relates to a low power write-once, read-only semiconductor memory (PROM or programmable read only memory) array wherein the semiconductor resistors located in the word line decoder and driver and also in the bit line decoder and sense amplifier of the memory array are fabricated to have a high resistivity thereby permitting the semiconductor array to operate with much lower power. The high resistivity semiconductor resistors of this write-once, read-only semiconductor memory array are fabricated using an ion implantation step, preferably, between the base and emitter diffusion process steps in fabricating the NPN transistor structures used in the bit line and word line decoders of the memory array. The high resistivity ion implanted resistor regions are preferably shallow, boron implanted regions that are formed by ion implanting through a thin silicon dioxide layer. Various resistor devices are disclosed using shallow, boron implanted, high resistivity regions. Also disclosed are PNP transistor devices (both vertical and lateral types) having P type emitter regions preferably made with a Boron implant. A P-channel MOS device is also disclosed where the P+ source and drain regions are shallow, implanted regions.

2 Claims, 9 Drawing Figures



United States Patent [19]

Athanas

[11] **4,219,379**

[45] **Aug. 26, 1980**

[54] **METHOD FOR MAKING A SEMICONDUCTOR DEVICE**

[75] Inventor: **Terry G. Athanas**, Lewisville, Tex.

[73] Assignee: **Mostek Corporation**, Carrollton, Tex.

[21] Appl. No.: **945,362**

[22] Filed: **Sep. 25, 1978**

Related U.S. Application Data

[62] Division of Ser. No. 759,803, Jan. 17, 1977, abandoned.

[51] **Int. Cl.**[2] **H01L 21/306**

[52] **U.S. Cl.** **156/653**; 29/571; 148/187; 156/657; 156/659.1; 156/662; 156/904; 357/23; 357/41; 357/59; 427/86; 427/93

[58] **Field of Search** 427/86, 87, 93–95; 156/653, 654, 655, 657, 659, 662, 904; 148/187; 29/571, 580, 591; 357/23, 41, 49, 53, 59, 91

[56] **References Cited**

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3,911,168	10/1975	Schinella et al.	427/94 X
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3,921,283	11/1975	Shappir	29/571
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IBM Technical Disclosure Bulletin, vol. 14, No. 4, Sep. 1971, Surface Protected Etching Technique for Silicon Gate FETs, by Jones et al., pp. 1052–1053.

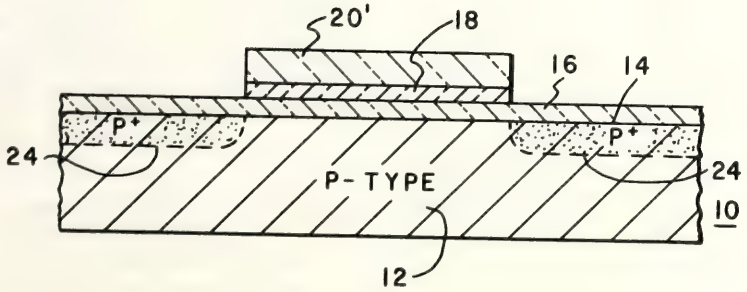
Primary Examiner—William A. Powell

Attorney, Agent, or Firm—G. Roland Love

[57] **ABSTRACT**

A method for making a semiconductor device is described in which polycrystalline silicon is vacuum deposited and then converted to silicon dioxide thereby providing a number of advantages over direct deposition of silicon dioxide. The method has particular applicability to isoplanar MOSFET integrated circuit manufacturing.

3 Claims, 15 Drawing Figures



United States Patent [19]

Amemiya et al.

[11] **4,210,996**

[45] **Jul. 8, 1980**

[54] **TRIMMING METHOD FOR RESISTANCE VALUE OF POLYCRYSTALLINE SILICON RESISTORS ESPECIALLY USED AS SEMICONDUCTOR INTEGRATED CIRCUIT RESISTORS**

[75] Inventors: **Yoshihito Amemiya**, Fuchu; **Kotaro Kato**, Chofu, both of Japan

[73] Assignee: **Nippon Telegraph and Telephone Public Corporation**, Japan

[21] Appl. No.: **900,300**

[22] Filed: **Apr. 26, 1978**

[30] **Foreign Application Priority Data**

May 4, 1977 [JP] Japan 52/51388

[51] **Int. Cl.**[2] **H01H 10/00**

[52] **U.S. Cl.** ..... **29/610 R**; 29/620; 330/199

[58] **Field of Search** ..... 29/610 R, 593, 613, 29/620; 338/195, 308; 330/199; 430/347 CC

[56] **References Cited**

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3,308,528	3/1967	Bullard	29/610
3,890,610	6/1975	Cahen	340/347 CC
4,131,884	12/1978	Comer	340/347 CC
4,138,671	2/1979	Comer	340/347 CC

Primary Examiner—Francis S. Husar

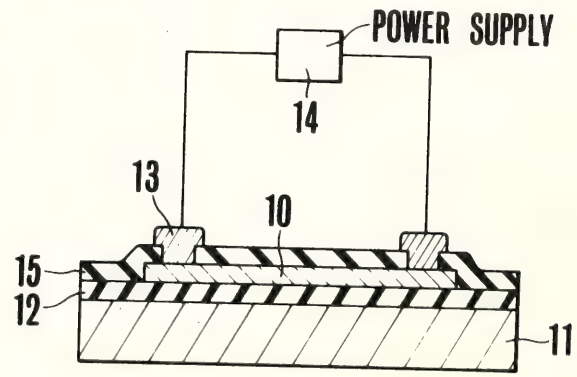
Assistant Examiner—Gene P. Crosby

Attorney, Agent, or Firm—Charles W. Helzer

[57] **ABSTRACT**

Current having a density higher than a critical value is passed through a polycrystalline resistor doped with impurities at a concentration higher than a critical value to decreasingly correct the initial value of the resistance, thereby trimming the resistance value of the resistor. When the resistor is used in a semiconductor integrated circuit, the current is passed through the existing (not additional) terminals of the integrated circuit.

11 Claims, 8 Drawing Figures



United States Patent [19]
Legat et al.
[11] **4,187,516**
[45] **Feb. 5, 1980**

[54] **SEMICONDUCTOR INTEGRATED CIRCUITS**

[75] Inventors: **Wilhelm H. Legat**, Wilmington, Mass.; **Keith G. Taft**, Ben Lomond, Calif.; **Karl H. Tiefert**, Los Altos, Calif.

[73] Assignee: **Raytheon Company**, Lexington, Mass.

[21] Appl. No.: **832,846**

[22] Filed: **Sep. 13, 1977**

Related U.S. Application Data

[60] Division of Ser. No. 719,201, Aug. 30, 1976, which is a continuation of Ser. No. 563,429, Mar. 31, 1975, abandoned, which is a continuation of Ser. No. 401,319, Sep. 27, 1973, abandoned, which is a continuation of Ser. No. 242,457, Apr. 10, 1972, abandoned.

[51] **Int. Cl.**[2] **H01L 29/04**
[52] **U.S. Cl.** **357/60**; 357/49; 357/55
[58] **Field of Search** 357/60, 49, 55

[56] **References Cited**

U.S. PATENT DOCUMENTS

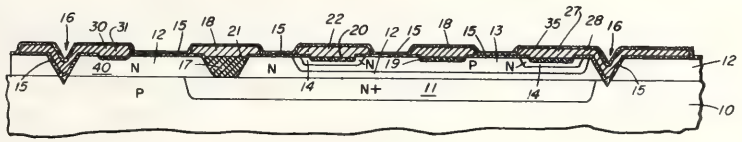
3,316,130	3/1967	Dash et al.	148/175
3,493,820	2/1970	Rosvold	317/234
3,818,289	6/1974	Mudge et al.	357/49

Primary Examiner—Martin H. Edlow
Attorney, Agent, or Firm—Richard M. Sharkansky; Joseph D. Pannone

[57] **ABSTRACT**

A semiconductor integrated circuit which is reduced in size by having active and/or passive elements in an epitaxial layer having a [100] crystallographic surface, and having anisotropically etched regions with sloped [111] crystallographic surface walls which isolate adjacent semiconductor elements and/or regions of semiconductor material beneath said elements. Conductors interconnecting said elements are supported on the [100] and [111] crystallographic surfaces and contact said elements and/or said high conductivity regions through apertures in surface passivating protective coatings on said surfaces.

8 Claims, 7 Drawing Figures



United States Patent [19]
Murari et al.
[11] **4,181,878**
[45] **Jan. 1, 1980**

[54] **INTEGRATED-CIRCUIT CHIP WITH VOLTAGE DIVIDER**

[75] Inventors: **Bruno Murari**, Monza; **Silvano Coccetti**, Vittuone, both of Italy

[73] Assignee: **SGS-ATES Component Elettronici S.p.A.**, Milan, Italy

[21] Appl. No.: **902,282**

[22] Filed: **May 3, 1978**

[30] **Foreign Application Priority Data**

May 4, 1977 [IT] Italy 23145 A/77

[51] **Int. Cl.**[2] **H01L 27/04**; H01C 1/14
[52] **U.S. Cl.** ..... **323/94 R**; 357/20; 357/51
[58] **Field of Search** ..... 357/51, 27, 48; 307/303, 309; 323/94 R

[56] **References Cited**

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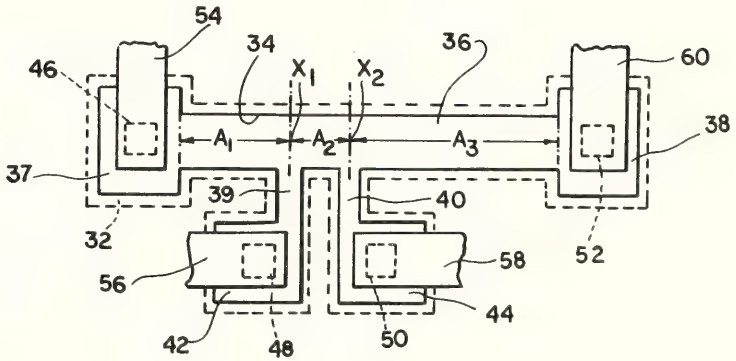
Dorler et al., IBM Technical Disclosure Bulletin, vol. 15, Apr. 1973, p. 3383.
Ting et al., Solid-State Electronics, vol. 14, pp. 433–338 (1971).

Primary Examiner—William D. Larkins
Attorney, Agent, or Firm—Karl F. Ross

[57] **ABSTRACT**

A voltage divider with at least two intermediate taps of almost the same potential is formed in an integrated-circuit chip by diffusing P-type impurities into an N-type substrate along a narrow strip zone ending in enlarged terminal areas. The strip zone has at least two narrower transverse branches which form closely adjoining junctions with it and extend laterally in the same or in opposite directions. Upon application of a voltage difference across the strip zone by means of electrodes placed on the two terminal areas, output terminals in contact with the free ends of the branches remote from the strip zone and connected to high-resistance loads carry potentials substantially equal to those of the corresponding junctions.

3 Claims, 5 Drawing Figures



United States Patent [19]
Awane et al.
[11] **4,194,214**
[45] * **Mar. 18, 1980**

[54] **INTEGRATION OF HIGH VOLTAGE DRIVER AND LOW VOLTAGE LOGIC IN A SEMICONDUCTOR DEVICE**

[75] Inventors: **Katunobu Awane**, Ikoma; **Hironori Hattori**, Suita; **Tetuo Biwa**, Osaka; **Hiroshi Tamaki**, Tenri, all of Japan

[73] Assignee: **Sharp Kabushiki Kaisha**, Osaka, Japan

[*] Notice: The portion of the term of this patent subsequent to Nov. 15, 1994, has been disclaimed.

[21] Appl. No.: **827,677**

[22] Filed: **Aug. 25, 1977**

[30] **Foreign Application Priority Data**

Aug. 26, 1976 [JP] Japan 51-102296

[51] **Int. Cl.**[2] **H01L 27/04**; H01L 29/78
[52] **U.S. Cl.** **357/41**; 315/169.3; 357/13; 357/53; 357/89; 357/23
[58] **Field of Search** 357/23, 41, 4, 53

[56] **References Cited**

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3,564,135	2/1971	Weimer	357/4
3,988,761	10/1976	Kanazawa	357/23
3,996,655	12/1976	Cunningham et al.	357/23
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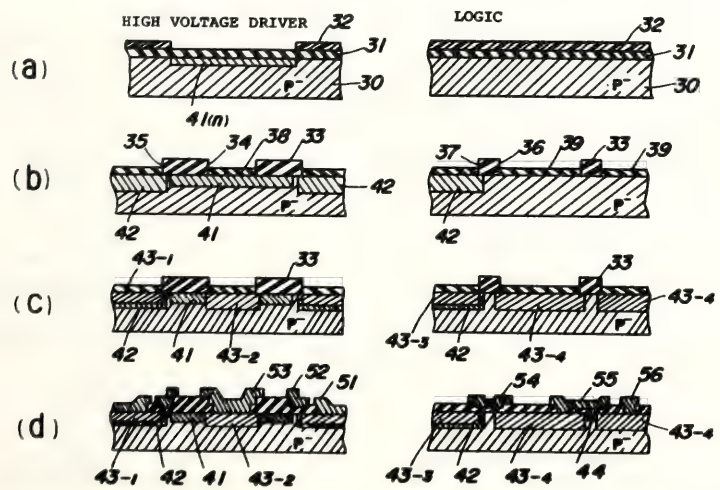
Blanchard et al., IEEE J. of Solid State Circuits, vol. SC9, No. 3, Jun. 1974, pp. 103, 108–109.
Saraswat et al., IEEE J. of Solid State Circuits, vol. SC-10, No. 3, Jun. 1975, pp. 136–137, 142.

Primary Examiner—William D. Larkins
Attorney, Agent, or Firm—Birch, Stewart, Kolasch & Birch

[57] **ABSTRACT**

High voltage diffusion-self-alignment metal oxide semiconductor devices and control logic circuitry therefor are integrated in a single semiconductor body. The integrated semiconductor device includes a considerably large number of output terminals compared to the number of input terminals. The output terminals develop signals of high voltages derived from the high voltage diffusion-self-alignment metal oxide semiconductor devices which are positioned at a peripheral zone of the semiconductor body.

3 Claims, 7 Drawing Figures



United States Patent [19]
Youmans et al.
[11] **4,193,836**
[45] **Mar. 18, 1980**

[54] **METHOD FOR MAKING SEMICONDUCTOR STRUCTURE**

[75] Inventors: **Albert P. Youmans**, Cupertino; **David F. Allison**, Los Altos; **David A. Maxwell**, San Jose, all of Calif.

[73] Assignee: **Signetics Corporation**, Sunnyvale, Calif.

[21] Appl. No.: **6,057**

[22] Filed: **Jan. 27, 1970**

Related U.S. Application Data

[60] Division of Ser. No. 569,368, Aug. 1, 1966, which is a division of Ser. No. 391,704, Aug. 24, 1964, Pat. No. 3,829,889, which is a continuation-in-part of Ser. No. 338,802, Jan. 20, 1964, abandoned, which is a continuation-in-part of Ser. No. 330,697, Dec. 16, 1963, abandoned.

[51] **Int. Cl.**[2] **H01L 21/306**
[52] **U.S. Cl.** **156/657**; 29/578; 29/580; 148/187; 156/648; 156/662
[58] **Field of Search** 156/3, 7, 17, 648, 649, 156/657, 662; 29/576, 580, 578; 427/82, 86, 87, 258, 259, 270, 271, 399, 93; 148/187

[56] **References Cited**

U.S. PATENT DOCUMENTS

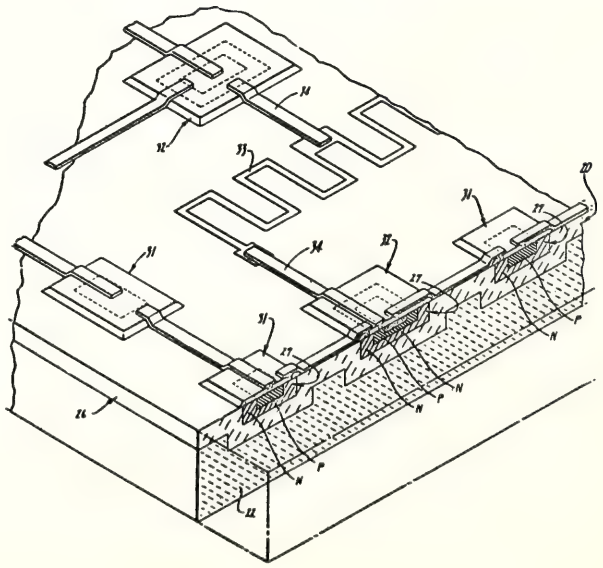
3,531,857	10/1970	Iwamatsu	156/657
4,139,401	2/1979	McWilliams et al.	148/175

Primary Examiner—Jerome W. Massie
Attorney, Agent, or Firm—Flehr, Hohbach, Test, Albritton & Herbert

[57] **ABSTRACT**

Method for making a semiconductor structure having isolated islands of semiconductor material from a semiconductor body by forming a first layer of insulating material on a surface of the body having a first support structure upon the layer of insulating material and then forming grooves in the semiconductor body which extend to the layer of insulating material formed from the semiconductor body. A second layer of insulating material is then formed on the exposed surfaces of the islands. A second support structure is then formed on the second layer of insulating material. Thereafter, the first support structure is removed and circuit devices are fabricated in the isolated islands.

11 Claims, 80 Drawing Figures



United States Patent [19]
Yim et al.
[11] **4,203,126**
[45] **May 13, 1980**

[54] **CMOS STRUCTURE AND METHOD UTILIZING RETARDED ELECTRIC FIELD FOR MINIMUM LATCH-UP**

[75] Inventors: **Ernest W. Yim**, Sunnyvale; **Paul G. G. VanLoon**, San Jose, both of Calif.

[73] Assignee: **Siliconix, Inc.**, Santa Clara, Calif.

[21] Appl. No.: **631,729**

[22] Filed: **Nov. 13, 1975**

[51] **Int. Cl.**[2] **H01L 27/02**
[52] **U.S. Cl.** **357/42**; 357/41; 357/44; 357/88; 357/89; 357/90
[58] **Field of Search** 357/40, 41, 42, 43, 357/44, 88, 89, 90

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,340,598	9/1967	Hatcher	357/42
3,440,503	4/1969	Gallagher	357/42
3,712,995	1/1973	Steudel	357/42
3,748,545	7/1973	Beale	357/42
3,920,481	11/1975	Hu	357/42
3,925,120	12/1975	Saida et al.	357/42
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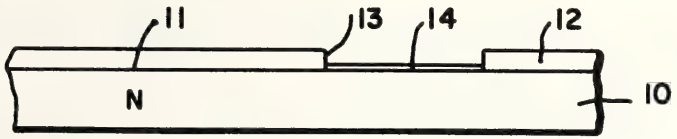
Electronics; Getting the Most Out of CMOS Devices for Analog Switching Jobs; by E. Thibodeaux; Dec. 1975, pp. 69–74.
IBM Technical Disclosure Bulletin; by James, vol. 16 No. 6 Nov. 1973, p. 1998.
IBM Technical Disclosure Bulletin; by Antipon, vol. 16 No. 8 Jan. 1974.

Primary Examiner—Andrew J. James
Attorney, Agent, or Firm—Flehr, Hohbach, Test, Albritton & Herbert

[57] **ABSTRACT**

CMOS device and method utilizing a retarded electric field for reducing the current gain in the base region of parasitic transistors in the device. A buried layer is utilized in the base region of the parasitic transistor, and the resistivities of the buried layer and substrate are chosen to reduce both NPN and PNP betas and also to reduce the distributed resistance shunting the P+N and N+P junctions, thereby increasing the level of current required to produce latch-up in the device.

6 Claims, 8 Drawing Figures



United States Patent [19]
Miles et al.
[11] **4,225,877**
[45] **Sep. 30, 1980**

[54] **INTEGRATED CIRCUIT WITH C-MOS LOGIC, AND A BIPOLAR DRIVER WITH POLYSILICON RESISTORS**

[75] Inventors: **Steven W. Miles**, Dudley; **Paul R. Emerald**, Sterling, both of Mass.

[73] Assignee: **Sprague Electric Company**, North Adams, Mass.

[21] Appl. No.: **939,506**

[22] Filed: **Sep. 5, 1978**

[51] **Int. Cl.**[2] **H01L 27/02**
[52] **U.S. Cl.** **357/41**; 357/42; 357/43; 357/48; 357/51; 357/59
[58] **Field of Search** 357/41, 42, 43, 48, 357/51, 59

[56] **References Cited**

U.S. PATENT DOCUMENTS

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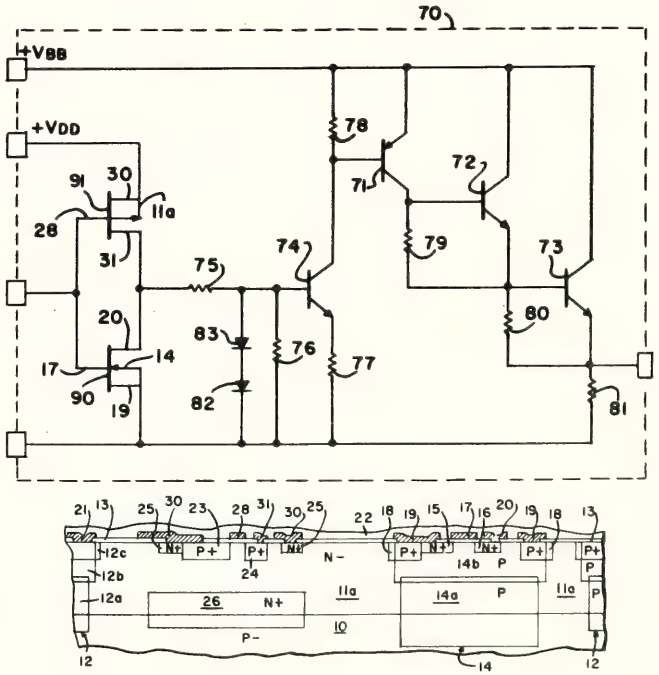
Primary Examiner—Edward J. Wojciechowicz
Attorney, Agent, or Firm—Connolly and Hutz

[57] **ABSTRACT**

An integrated circuit includes MOS transistors and bipolar transistors, each of both polarity types, in a silicon wafer. High value polysilicon resistors are formed over an outer protective silicon dioxide layer of the silicon wafer, which resistors are rendered conductive by having ion implanted impurities concentrated near the outer surface of the polysilicon body, permitting achievement of close tolerance resistors. The process for making the integrated circuit includes forming a sheet of polysilicon over the entire wafer surface, performing the ion implantation and etching away all but the desired resistor portions of the polysilicon. It also includes heating the wafer to simultaneously anneal the ion implanted polysilicon, form the gate oxide, thicken the oxide over the emitters, and cover the resistor body with a thin protective oxide film.

7 Claims, 6 Drawing Figures



United States Patent [19]
Plummer
[11] **4,199,774**
[45] **Apr. 22, 1980**

[54] **MONOLITHIC SEMICONDUCTOR SWITCHING DEVICE**

[75] Inventor: **James D. Plummer**, Mountain View, Calif.

[73] Assignee: **The Board of Trustees of the Leland Stanford Junior University**, Stanford, Calif.

[21] Appl. No.: **943,200**

[22] Filed: **Sep. 18, 1978**

[51] **Int. Cl.**[2] **H01L 7/02**
[52] **U.S. Cl.** **357/41**; 357/23; 357/55; 357/48; 307/304
[58] **Field of Search** 357/41, 48, 55, 23; 307/304

[56] **References Cited**

U.S. PATENT DOCUMENTS

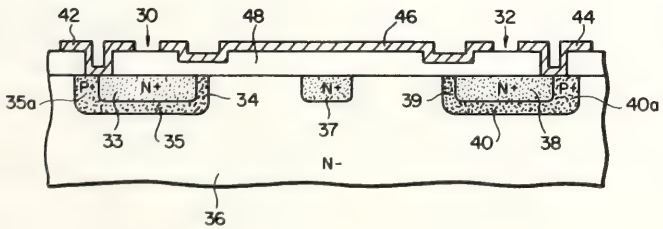
3,926,694	12/1975	Cauge	148/187
3,974,486	8/1976	Curtis	340/173 R
3,996,655	12/1976	Cunningham	29/571
4,119,996	10/1978	Jhabrola	357/23
4,145,703	3/1979	Blanchard	357/55

Primary Examiner—Martin H. Edlow
Attorney, Agent, or Firm—Flehr, Hohbach, Test, Albritton & Herbert

[57] **ABSTRACT**

An electrical circuit device made in integrated monolithic form has low level operating characteristics of a MOS device and high level operating characteristics of a Triac. The structure includes two double diffused MOS transistors which have merged drain regions. At higher voltage and current levels a lateral Triac structure is triggered by the MOS devices. Alternatively, separate terminal contacts can be made to the P and N regions comprising the MOS transistor source and channel regions with the Triac triggered conventionally by an externally applied control voltage.

25 Claims, 20 Drawing Figures



United States Patent [19]
Sanders
[11] **4,202,005**
[45] **May 6, 1980**

[54] **DISTRIBUTED COLLECTOR BALLAST RESISTOR STRUCTURE**

[75] Inventor: **Paul W. Sanders**, Manhattan Beach, Calif.

[73] Assignee: **TRW Inc.**, Los Angeles, Calif.

[21] Appl. No.: **962,122**

[22] Filed: **Nov. 20, 1978**

[51] **Int. Cl.**[2] **H01L 27/02**
[52] **U.S. Cl.** **357/51**; 357/13; 357/20; 357/36; 357/89
[58] **Field of Search** 357/51, 13, 20, 89, 357/36

[56] **References Cited**

U.S. PATENT DOCUMENTS

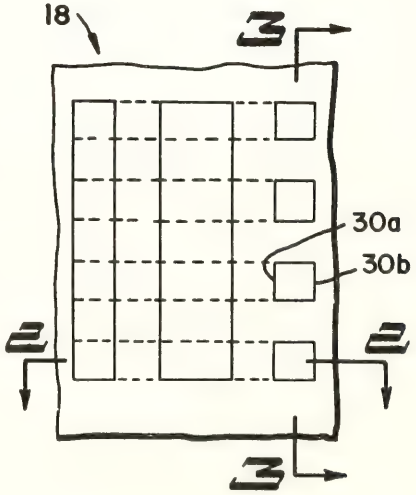
4,123,672	10/1978	Kasperkoritz	307/303

Primary Examiner—Martin H. Edlow
Attorney, Agent, or Firm—Martin R. Horn

[57] **ABSTRACT**

A distributed collector ballast resistor structure for use in a distributed collector contacted transistor comprises a diffusion geometry which is designed to employ a number of distributed collector ballast resistors in parallel as opposed to a single bulk resistor in series with the collector circuit thereby generating a lower current for a given voltage during avalanche while allowing lower saturation voltage, better RF gain and higher saturated output power.

7 Claims, 5 Drawing Figures



United States Patent [19]
Oehler et al.
[11] **4,183,134**
[45] **Jan. 15, 1980**

[54] **HIGH YIELD PROCESSING FOR SILICON-ON-SAPPHIRE CMOS INTEGRATED CIRCUITS**

[75] Inventors: **Harry G. Oehler**, Glen Burnie; **David S. Herman**, Columbia; **James R. Cricchi**, Catonsville, all of Md.

[73] Assignee: **Westinghouse Electric Corp.**, Pittsburgh, Pa.

[21] Appl. No.: **968,529**

[22] Filed: **Dec. 11, 1978**

Related U.S. Application Data

[63] Continuation of Ser. No. 769,138, Feb. 15, 1977, abandoned.

[51] **Int. Cl.**[2] **H01L 21/22**; H01L 21/26
[52] **U.S. Cl.** **29/571**; 148/1.5; 148/187; 148/188; 357/42
[58] **Field of Search** ..... 148/1.5, 187, 188; 29/571, 577 R; 357/42

[56] **References Cited**

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3,566,518	3/1971	Brown et al.	29/571
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3,837,071	9/1974	Ronen	29/571
3,865,653	2/1975	Goser	148/187
3,909,307	8/1975	Stein	148/1.5
4,023,195	5/1977	Richman	357/23

OTHER PUBLICATIONS

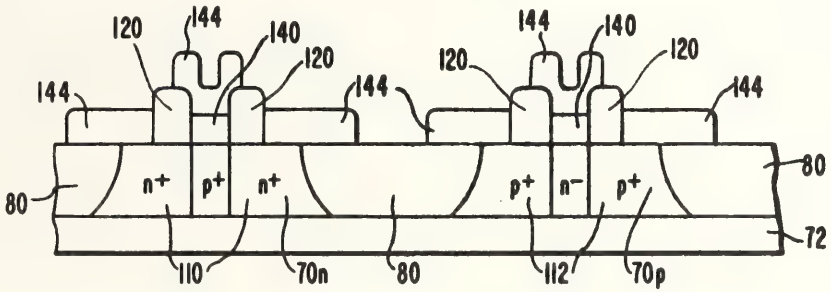
Dataquest Inc., "Silicon on Sapphire", Palo Alto, Calif., Feb. 21, 1975, pp. 37–59.

Primary Examiner—G. Ozaki
Attorney, Agent, or Firm—R. M. Trepp

[57] **ABSTRACT**

Described herein a technique for constructing a complementary MOS device on a sapphire substrate so that the surface of the device is planarized, the P-channel and N-channel devices are in substantially correct registration, the threshold voltage for the back-channel leakage effect inherent in sapphire substrate device to occur is increased, and the areas of gate oxidation are pseudo self-aligned so as to minimize overlap of the gate oxide with the source and drain regions.

11 Claims, 17 Drawing Figures



United States Patent [19]
Thornburg
[11] **4,181,913**
[45] **Jan. 1, 1980**

[54] **RESISTIVE ELECTRODE AMORPHOUS SEMICONDUCTOR NEGATIVE RESISTANCE DEVICE**

[75] Inventor: **David D. Thornburg**, Los Altos, Calif.

[73] Assignee: **Xerox Corporation**, Stamford, Conn.

[21] Appl. No.: **801,959**

[22] Filed: **May 31, 1977**

[51] **Int. Cl.**[2] **H01L 45/00**
[52] **U.S. Cl.** **357/2**; 357/4; 357/51; 357/67; 357/71
[58] **Field of Search** ..... 357/2, 57; 307/238, 307/252 E, 324, 299 R; 365/163

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,382,418	5/1968	Jensen	357/2
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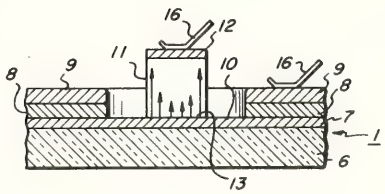
3,546,491	12/1970	Berglund	357/57
3,629,863	12/1971	Neale	357/2
3,864,719	2/1975	Uematsu et al.	357/57
3,906,537	9/1975	Thornburg et al.	357/2
3,975,755	8/1976	Thornburg	357/2

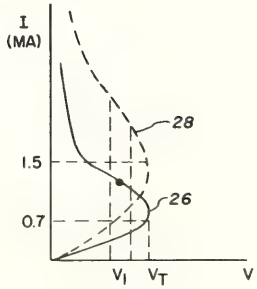
Primary Examiner—William D. arkins
Attorney, Agent, or Firm—Irving Keschner; W. Douglas Carothers, Jr.

[57] **ABSTRACT**

Semiconductor devices which exhibit negative differential resistance and comprise a semiconductor material in contact with an electrode and a resistive film layer, preferably comprising an alloy of nickel and chrome is disclosed. The slope of the negative resistance region and the current filament area can be varied by altering the sheet resistivity of the resistive film layer. This allows the semiconductor device to be incorporated in a single monolithic thin film integrated circuit in which the thickness of the semiconductor layer utilized in the integrated circuit is constant. A method for fabricating the aforementioned semiconductor device is also disclosed.

7 Claims, 7 Drawing Figures





United States Patent [19]

Nishizawa

[11] **4,198,648**

[45] **Apr. 15, 1980**

[54] **INTEGRATED SEMICONDUCTOR DEVICE**

[75] Inventor: **Jun-ichi Nishizawa**, Sendai, Japan

[73] Assignee: **Zaidan Hojin Handotai Kenkyu Shinkokai**, Sendai, Japan

[21] Appl. No.: **902,965**

[22] Filed: **May 4, 1978**

[30] **Foreign Application Priority Data**

May 15, 1977 [JP] Japan 52/55778

[51] **Int. Cl.**[2] **H01L 27/02**

[52] **U.S. Cl.** **357/43**; 357/22; 357/41; 357/46; 357/50; 357/55

[58] **Field of Search** 357/22, 41, 43, 46, 357/50, 55

[56] **References Cited**

PUBLICATIONS

IEEE Trans. on Electron Devices, vol. ED-22, pp. 185-197, Apr. 1975.

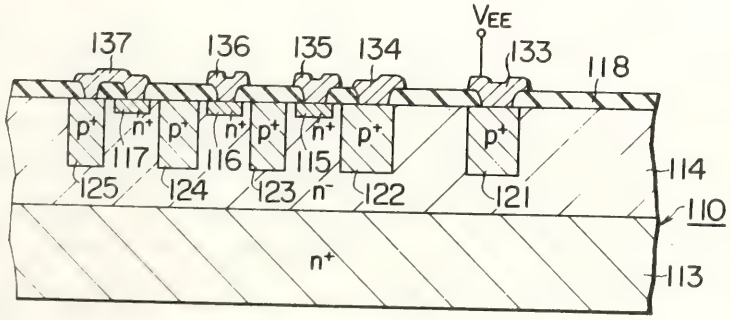
Primary Examiner—Edward J. Wojciechowicz

Attorney, Agent, or Firm—Cushman, Darby & Cushman

[57] **ABSTRACT**

An integrated semiconductor device comprising: a first and a second static induction transistor each including a drain and a source, each having a first conductivity type, a current channel having the first conductivity type and located between the drain and the source, and a gate having a second conductivity type opposite to the first conductivity type and located adjacent to the current channel; and a third bipolar transistor including a collector and an emitter each having the second conductivity type, and a base having the first conductivity type and located between the collector and the emitter, the collector being connected to the gates of the first and second transistors and also to the drain of the second transistor, the source of the second transistor being connected to the source of the first transistor. The second transistor is operative for suppressing the occurrence of an unrequired excessive minority carrier injection in the first transistor.

25 Claims, 9 Drawing Figures



United States Patent [19]

Kruzhanov et al.

[11] **4,195,354**

[45] **Mar. 25, 1980**

[54] **SEMICONDUCTOR MATRIX FOR INTEGRATED READ-ONLY STORAGE**

[76] Inventors: **Jury V. Kruzhanov**, 103498, korpus 431, kv. 112; **Viktor P. Dubinin**, 103498, korpus 445, kv. 120; **Viktor S. Ovchinnikov**, 103527, korpus 839, kv. 11; **Vladimir E. Safronov**, 103527, korpus 811, kv. 146, all of Moscow, U.S.S.R.

[21] Appl. No.: **931,422**

[22] Filed: **Aug. 7, 1978**

[30] **Foreign Application Priority Data**

Aug. 16, 1977 [SU] U.S.S.R. ..... 2517209[1]

[51] **Int. Cl.**[2] **G11C 11/36**

[52] **U.S. Cl.** **365/105**; 357/20

[58] **Field of Search** 365/94, 103, 104, 105; 357/20, 45

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,717,852 2/1973 Abbas et al. 365/103

OTHER PUBLICATIONS

Abbas, Electronically Encodable Read-only Store, IBM Technical Disclosure Bulletin, vol. 13, No. 6, 11/70, pp. 1426-1427.

Gaesslen, Schottky Barrier Read-only Memory, IBM Technical Disclosure Bulletin, vol. 14, No. 1, 6/71, p. 252.

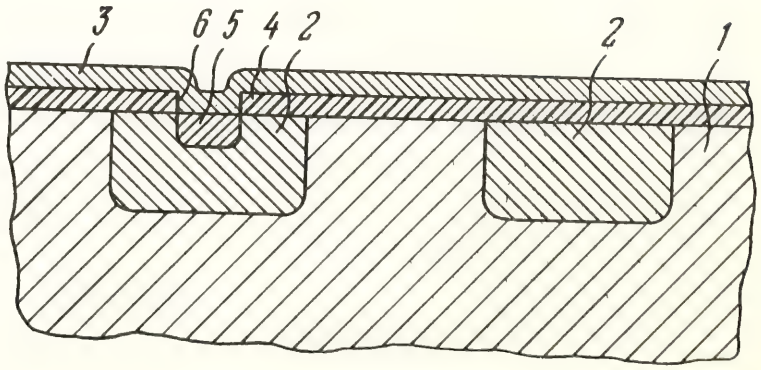
Primary Examiner—Stuart N. Hecker

Attorney, Agent, or Firm—Steinberg & Blake

[57] **ABSTRACT**

A semiconductor matrix for an integrated read-only storage is disclosed which comprises a plurality of components each of which is provided with a semiconductor region of a first type conductivity, at least some components of said components each having a semiconductor region of a second type conductivity disposed in said first type conductivity semiconductor region. Said components are formed at the locations where semiconductor buses of said first type conductivity, made in a substrate, intersect metallic buses disposed on a dielectric layer which is adapted to isolate the semiconductor buses from the metallic ones. There are windows comprising openings which register with them and are adapted to provide for electric contact between the second type conductivity semiconductor regions and the metallic buses, said windows are formed in the dielectric layer above said second type conductivity semiconductor regions of respective components.

1 Claim, 1 Drawing Figure



United States Patent [19]
Lardy et al.
[11] **4,219,828**
[45] **Aug. 26, 1980**

[54] **MULTIDRAIN METAL-OXIDE-SEMICONDUCTOR FIELD-EFFECT DEVICE**

[76] Inventors: **Jean-Louis Lardy**, Lotissement les Iris no. 23, Le Versoud-Domène, France, 38420; **Jacques Majos**, 4, Rue du Dauphine, Lannion, France, 22300

[21] Appl. No.: **966,502**

[22] Filed: **Dec. 4, 1978**

[30] **Foreign Application Priority Data**

Dec. 6, 1977 [FR] France 77 36720

[51] **Int. Cl.**[2] **H01L 29/80**
[52] **U.S. Cl.** **357/22**; 357/23; 357/41; 357/36
[58] **Field of Search** 357/22, 23, 41, 36

[56] **References Cited**

U.S. PATENT DOCUMENTS

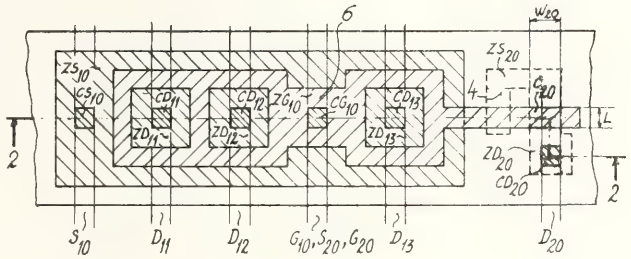
4,015,278 3/1977 Fukuta 357/55

Primary Examiner—E. Wojciechowicz
Attorney, Agent, or Firm—Abraham A. Saffitz

[57] **ABSTRACT**

A metal-oxide-semiconductor field-effect device for constituting a single logic inverter stage. It includes a multidrain transistor operating in enhancement mode and a load transistor, both of monochannel metal-oxide-semiconductor structure. The inverter transistor comprises a single gate region and several drain regions. The single gate region and the single channel region of the inverter multidrain transistor are superimposed on both implantation planes separated by a thin insulating layer, entirely surround each drain region of the inverter multidrain transistor and are entirely surrounded by the single source region of the inverter multidrain transistor.

6 Claims, 20 Drawing Figures



United States Patent [19]
Warner, Jr.
[11] **4,190,852**
[45] **Feb. 26, 1980**

[54] **PHOTOVOLTAIC SEMICONDUCTOR DEVICE AND METHOD OF MAKING SAME**

[76] Inventor: **Raymond M. Warner, Jr.**, 5001 Arden Ave., Minneapolis, Minn. 55424

[21] Appl. No.: **942,152**

[22] Filed: **Sep. 14, 1978**

[51] **Int. Cl.**[2] **H01L 27/14**
[52] **U.S. Cl.** **357/30**; 357/48; 357/86; 148/186; 148/189
[58] **Field of Search** 357/30, 48, 86; 148/186, 189

[56] **References Cited**

U.S. PATENT DOCUMENTS

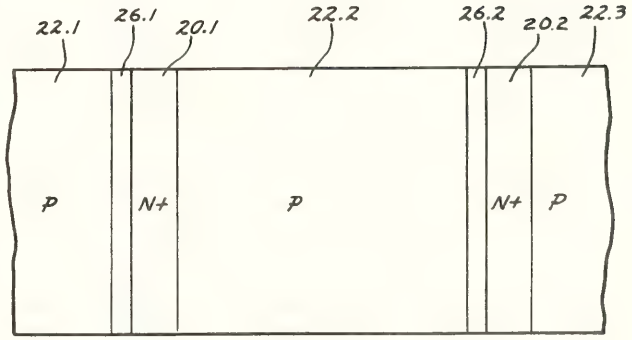
3,994,012 11/1976 Warner 357/30

Primary Examiner—Martin H. Edlow
Attorney, Agent, or Firm—Peterson, Palmatier, Sturm & Sjoquist, Ltd.

[57] **ABSTRACT**

A photovoltaic semiconductor device which is a horizontal multijunction series-array solar battery with a monocrystalline body and having elongate zones of aluminum doped silicon passed entirely through N-type silicon layers by Thermomigration process to connect together epitaxially grown buried P layers. Masked elongate N diffusion zones which are parallel and substantially contiguous to each elongated P zone penetrates at least through the lowest P layer thereby forming an inactive pn junction. A thin shallow layer of P-type material is diffused across the top N-type layer. Topologically continuous photovoltaic junctions exist in each cell of the photovoltaic semiconductor device between the shallow layer of P-type material, the buried layer or layers of P-type material, the elongate zone of aluminum doped silicon, and the N-type silicon thereby forming active pn junctions. Metallic strips, at the other pn junctions formed by the thermomigrated aluminum which are inactive, electrically connect the cells together. A method is disclosed for manufacturing the photovoltaic semiconductor device.

22 Claims, 2 Drawing Figures



REFERENCE CITATION INFORMATION

INTEGRATED CIRCUIT STRUCTURE

During the examination of an application for a patent in the United States, references may be cited by the examiner and applicant to show the state of the art or to indicate the prior art most closely related to the invention which is claimed in the application. The information presented below is based on the references made of record during the examination of U.S. Patents granted in the subject technology from 1975-1979. A more detailed explanation of these data appears in Appendix A.

TOTAL PATENTS ISSUED (1975-1979)	1036
TOTAL REFERENCES CITED	6046
U.S. Patent References Cited	5119
Foreign Patent References Cited	147
Other References Cited	780

COUNTRY OF ORIGIN OF U.S. PATENT REFERENCES CITED	NUMBER OF CITATIONS
United States	3694
Japan	605
West Germany	259
Netherlands	220
United Kingdom	150
France	91
Canada	31
Switzerland	24
Italy	13
Sweden	12
Denmark	8
USSR	5
Others	7

MOST FREQUENTLY CITED PATENTS	NUMBER OF CITATIONS
3,648,125	34
3,823,353	20
3,736,477	19
3,386,865	19

MOST FREQUENTLY CITED ASSIGNEES	NUMBER OF CITATIONS
International Business Machines Corporation	333
U.S. Phillips Corporation	193
Texas Instruments, Incorporated	182
RCA Corporation	137

United States Patent

Peltzer

[15] 3,648,125

[45] Mar. 7, 1972

[54] **METHOD OF FABRICATING INTEGRATED CIRCUITS WITH OXIDIZED ISOLATION AND THE RESULTING STRUCTURE**

[72] Inventor: **Douglas L. Peltzer**, Cupertino, Calif.

[73] Assignee: **Fairchild Camera and Instrument Corporation**, Mountain View, Calif.

[22] Filed: **Feb. 2, 1971**

[21] Appl. No.: **111,956**

[52] **U.S. Cl.** **317/235**, 317/101, 317/234

[51] **Int. Cl.** **H01l 19/00**

[58] **Field of Search** 317/234, 235, 101; 29/576

[56] **References Cited**

UNITED STATES PATENTS

3,136,897	6/1964	Kaufman	317/235 X
3,189,798	6/1965	Benjamin	317/234
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3,210,677	10/1965	Lin et al	330/17
3,474,308	10/1969	Kronlage	317/235
3,575,740	4/1971	Castrucci et al	148/175
3,575,741	4/1971	Murphy	148/175

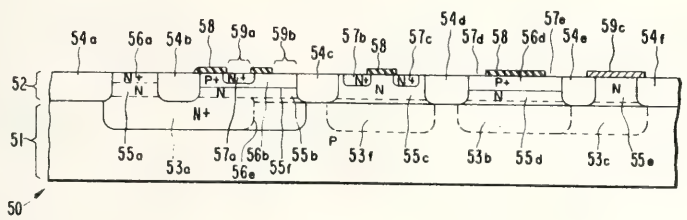
Primary Examiner—James D. Kallam

Attorney—Roger S. Borovoy, Alan MacPherson and Charles L. Botsford

[57] **ABSTRACT**

A thin silicon epitaxial layer, formed on a silicon substrate, is subdivided into electrically isolated pockets by a grid of oxidized regions of epitaxial silicon material which extend through the epitaxial layer to a laterally extending PN junction.

24 Claims, 19 Drawing Figures



United States Patent [19]

Berger et al.

[11] 3,823,353

[45] July 9, 1974

[54] **MULTI LAYERED VERTICAL TRANSISTOR HAVING REACH-THROUGH ISOLATING CONTACTS**

[75] Inventors: **Horst H. Berger**, Sindelfingen; **Siegfried K. Wiedmann**, Stuttgart, both of Germany

[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[22] Filed: **Mar. 2, 1973**

[21] Appl. No.: **337,510**

[30] **Foreign Application Priority Data**

Mar. 14, 1972 Germany 22121682

[52] **U.S. Cl.** **357/40**, 307/215, 357/48, 357/51, 357/89

[51] **Int. Cl.** **H01l 11/00**, H01l 15/00

[58] **Field of Search** 317/235, 22.1, 31, 482, 317/48.4; 307/215

[56] **References Cited**

UNITED STATES PATENTS

3,506,893	4/1970	Dhaka	317/235 E
3,524,113	8/1970	Agusta et al.	317/235 E
3,576,682	4/1971	Frouin et al.	317/235 E
3,622,382	11/1971	Karl	317/235 E
3,643,235	2/1972	Berger et al.	317/235 E
3,697,337	10/1972	Stehlin	317/235 E
3,717,564	2/1973	Bhatt	317/235 E
3,736,477	5/1973	Berger et al.	317/235 R

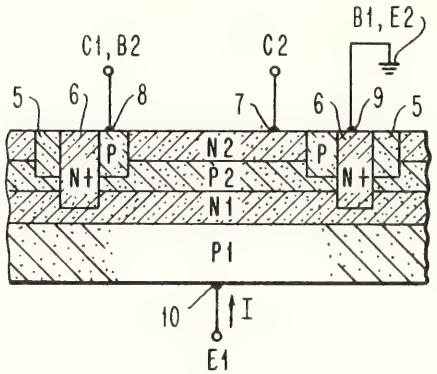
Primary Examiner—Andrew J. James

Attorney, Agent, or Firm—Martin G. Reiffin

[57] **ABSTRACT**

Logic circuits for performing the INVERTER and NOR functions, and monolithic integrated structures for realizing the circuits. The basic circuit comprises PNP transistor and an NPN transistor. The emitter of the PNP transistor has its base grounded and its collector connected to the base of the NPN transistor having its emitter grounded. The logic signal input is at the base of the NPN transistor. The output is taken at the collector of the NPN transistor and is the inverse of the input. Two such basic circuits are interconnected to provide the NOR function.

6 Claims, 8 Drawing Figures



United States Patent [19]

Berger et al.

[11] **3,736,477**

[45] **May 29, 1973**

[54] **MONOLITHIC SEMICONDUCTOR CIRCUIT FOR A LOGIC CIRCUIT CONCEPT OF HIGH PACKING DENSITY**

[75] Inventors: **Horst H. Berger**, Sindelfingen, Germany; **Siegfried K. Wiedmann**, Poughkeepsie, N.Y.

[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[22] Filed: **Apr. 14, 1971**

[21] Appl. No.: **134,008**

[30] **Foreign Application Priority Data**

May 5, 1970 Germany ..... P 20 21 824.0

[52] **U.S. Cl.** ..... **317/235 R**, 307/303, 317/235, 317/235 Z

[51] **Int. Cl.** **H01l 19/00**

[58] **Field of Search** ..... 317/235 D, 235 E, 317/235 Y; 307/303; 213

[56] **References Cited**

UNITED STATES PATENTS

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3,238,384	3/1966	Lewis	317/235
3,401,319	9/1968	Watkins	317/235

FOREIGN PATENTS OR APPLICATIONS

2,007,263	1/1970	France	307/303

OTHER PUBLICATIONS

IBM Tech. Discl. Bul., "Backdropped Array Technology" by Tsui, Vol. 13, No. 10, March, 1971, page 2,953.

IBM Tech. Disel Bul. "Memory Cell" by Berger et al., Vol. 11, No. 11, April, 1969, page 1,601.

Electronics, "Hard Cell" April 3, 1967, page 44.

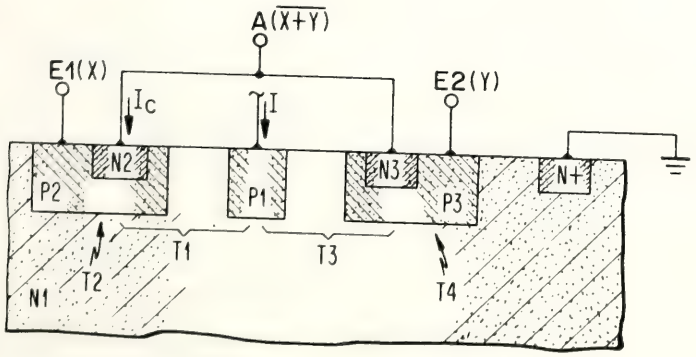
Primary Examiner—Jerry D. Craig

Attorney—Hanifin & Jancin and Martin G. Reiffin

[57] **ABSTRACT**

A monolithic semiconductor circuit comprises a lateral PNP transistor and an inversely operated vertical NPN transistor. The lateral transistor is formed by a pair of mutually spaced P-type regions diffused in an N-type semiconductor body. The collector region has diffused therein a region of N-type and constituting the collector of the vertical transistor. The semiconductor body constitutes the base region of the lateral transistor and the emitter region of the vertical transistor.

14 Claims, 9 Drawing Figures



United States Patent Office

3,386,865

Patented June 4, 1968

PROCESS OF MAKING PLANAR SEMICONDUCTOR DEVICES ISOLATED BY ENCAPSULATING OXIDE FILLED CHANNELS

Ven Y. Doo, Poughkeepsie, N.Y., assignor to International Business Machines Corporation, Armonk, N.Y., a corporation of New York

Filed May 10, 1965, Ser. No. 454,374

4 Claims. (Cl. 148—175)

References Cited

UNITED STATES PATENTS

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3,206,339	9/1965	Thornton	148—174 XR
3,234,058	2/1966	Marinace	148—175
3,260,902	7/1966	Porter	148—175 XR
3,265,542	8/1966	Hirshon	148—175
3,296,040	1/1967	Wigton	148—175
3,343,255	9/1967	Donovan	148—1.5 XR
3,354,360	11/1967	Campagna et al.	29—578 XR

HYLAND BIZOT, *Primary Examiner.*

P. WEINSTEIN, *Assistant Examiner.*

This invention relates to semiconductor devices and in particular to planar type isolated semiconductor devices.

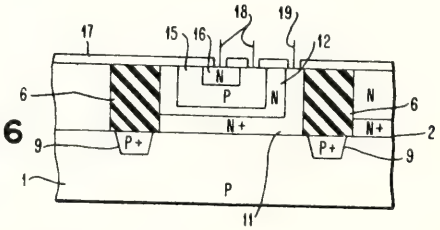
In the planar type of fabrication, a plurality of individual semiconductor elements are formed in a substrate of semiconductor material by steps which are all conducted through a single major surface. Such fabrication of planar type devices on a single substrate has as a goal the fabrication of the maximum number of devices on the major surface, while at the same time electrically isolating each device and its contacts and accomplishing this with a minimum of critical spacing restrictions on the electrodes which provide circuit connections to the individual devices. The technique involves the use of an encapsulating material which serves to protect the PN junctions of the finished product and to serve as a shape delineating member in the formation of portions of the devices. Previous approaches in the art to provide isolation between individual devices require added difficult processing, critical inter-device spacing, or unreliability in providing high resistance paths between devices.

The preferable isolating medium should provide a minimum of deleterious electrical effects to the device and yet provide good heat transfer.

The encapsulating material has good electrical properties and it would be desirable to use the encapsulating material in a channel for isolation but encapsulating material has been found to provide an undesirable low resistance current path where it contacts the substrate.

What has been discovered is a combination of structural features and processing steps in the fabrication of a planar device which provide a semiconductor device that is isolated by a channel of an encapsulating material and a region of higher conductivity type in the substrate where the encapsulating material contacts the surface of the substrate.

FIG. 6



CPU'S AND OTHER SYSTEMS

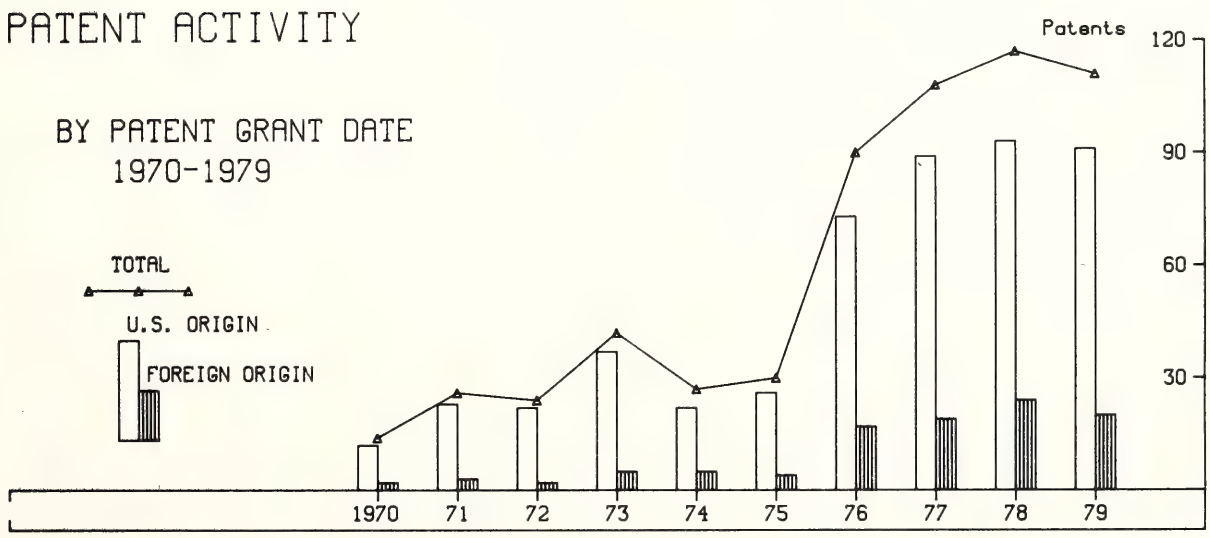
This profile is drawn to systems in which the inventive thrust involves the use of microelectronic processing devices, e.g., CPU's.

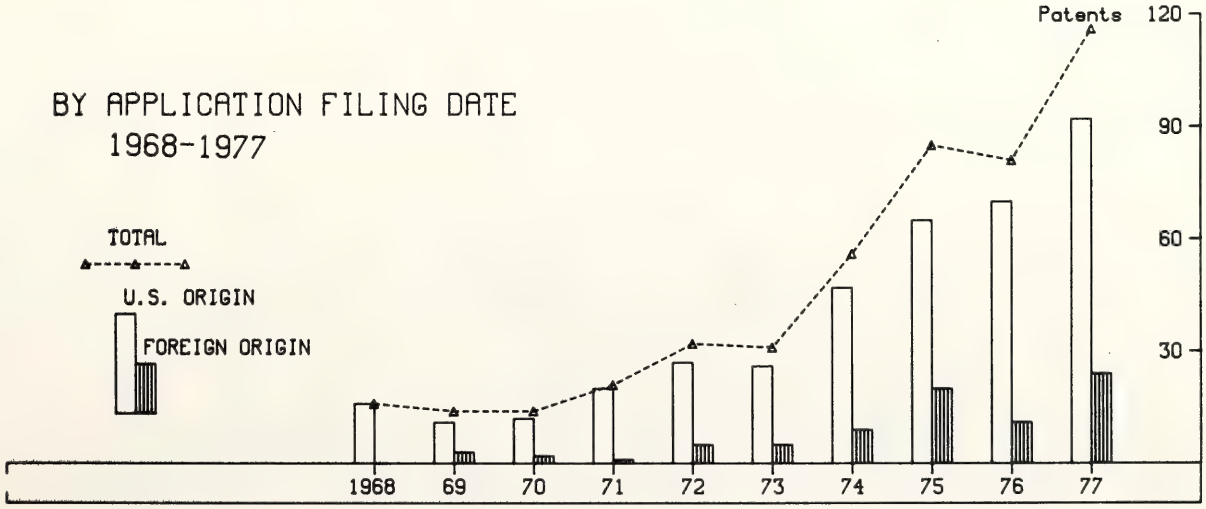
INCLUDED IN THIS PROFILE ARE SELECTED PATENTS FROM:

Class 364, Subclasses 200 and 900

ACTIVITY INDICES (1977-1979)

GROWTH	57.0%
FOREIGN SHARE	18.8%
CORPORATE OWNED	91.7%
GOVERNMENT OWNED	1.8%
U.S. OWNED OF FOREIGN	12.7%





MICROELECTRONICS - CPUS AND OTHER SYSTEMS

PATENT ACTIVITY (1963-1979) BY DATE OF PATENT GRANT

	NUMBER OF PATENTS															
	63-65	1966	1967	1968	1969	1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	TOTAL
TOTAL	1	2	3	6	10	14	26	24	42	27	30	90	108	117	111	611
U.S. ORIGIN	1	1	3	6	10	12	23	22	37	22	26	73	89	93	91	509
FOREIGN ORIGIN		1				2	3	2	5	5	4	17	19	24	20	102
JAPAN							2	1		1		3	7	13	9	36
GERMANY		1						1	1	1	3	3	5	1	3	19
UNITED KINGDOM						2	1		1		1	2	3	5	3	18
FRANCE									1	1		3	2	3	1	11
ITALY												1	1	1	2	5
NETHERLANDS									2			1				3
BELGIUM												3				3
CANADA										2					1	3
ISRAEL												1			1	2
SWITZERLAND													1			1
U.S.S.R.														1		1
U.S. ORIGIN	1	1	3	6	10	12	23	22	37	22	26	73	89	93	91	509
U.S. CORP. OWNED	1	1	3	6	10	12	22	19	36	21	25	65	80	87	80	468
U.S. GOVT. OWNED								3	1	1		2	2	1	1	11
U.S. INDIV. OWNED							1				1	6	7	5	8	28
FOREIGN OWNED															2	2
FOREIGN ORIGIN		1				2	3	2	5	5	4	17	19	24	20	102
U.S. OWNED									3	2		5	4	2	2	18
FOREIGN OWNED		1				2	3	2	2	3	4	12	15	22	18	84
FOREIGN CORP.		1				2	3	2	1	3	3	11	13	21	17	77
FOREIGN GOVT.													1		1	2
FOREIGN INDIV.									1		1	1	1	1		5

PATENT ACTIVITY (PATENTS GRANTED 1/67-12/79) BY DATE OF PATENT APPLICATION

	NUMBER OF PATENTED APPLICATIONS															
	PRE 66	1966	1967	1968	1969	1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	TOTAL
TOTAL	6	4	9	16	14	14	21	32	31	56	85	81	116	104	19	608
U.S. ORIGIN	6	4	9	16	11	12	20	27	26	47	65	70	92	84	18	507
FOREIGN ORIGIN					3	2	1	5	5	9	20	11	24	20	1	101
JAPAN					1	1	1		1	2	4	3	12	10	1	36
GERMANY								2	2	1	6	3	1	3		18
UNITED KINGDOM					2	1			1	1	3	1	7	2		18
FRANCE								2		1	4	1	1	2		11
ITALY										1		1	2	1		5
NETHERLANDS								1	1			1				3
BELGIUM											2	1				3
CANADA										2	1					3
ISRAEL										1				1		2
SWITZERLAND													1			1
U.S.S.R.														1		1
U.S. ORIGIN	6	4	9	16	11	12	20	27	26	47	65	70	92	84	18	507
U.S. CORP. OWNED	6	4	9	16	11	11	16	27	25	41	60	61	88	75	16	466
U.S. GOVT. OWNED							4			1	1	2	2	1		11
U.S. INDIV. OWNED						1			1	5	4	7	2	7	1	28
FOREIGN OWNED														1	1	2
FOREIGN ORIGIN					3	2	1	5	5	9	20	11	24	20	1	101
U.S. OWNED								1	2	3	2	5	1	4		18
FOREIGN OWNED					3	2	1	4	3	6	18	6	23	16	1	83
FOREIGN CORP.					3	2	1	3	3	5	16	5	23	14	1	76
FOREIGN GOVT.												1		1		2
FOREIGN INDIV.								1		1	2			1		5

CPU'S AND OTHER SYSTEMS

ASSIGNEES WITH 3 OR MORE PATENTS (1/69-12/79)

INTERNATIONAL BUSINESS MACHINES CORPORATION	73
TEXAS INSTRUMENTS, INCORPORATED	72
BURROUGHS CORPORATION	34
MOTOROLA INC.	28
HONEYWELL INFORMATION SYSTEMS INC.	26
HEWLETT-PACKARD COMPANY	17
BELL TELEPHONE LABORATORIES INCORPORATED	15
SPERRY RAND CORPORATION	15
XEROX CORPORATION	14
DATA GENERAL CORPORATION	13
TOKYO SHIBAURA ELECTRIC CO., LTD.	10
HITACHI, LTD.	9
NCR CORPORATION	9
HONEYWELL INC.	9
UNITED STATES OF AMERICA, NAVY	9
RCA CORPORATION	8
INTEL CORPORATION	6
U.S. PHILIPS CORPORATION	6
ALLEN-BRADLEY COMPANY	6*
OLYMPIA WERKE AG	5
COGAR CORPORATION	5
FAIRCHILD CAMERA AND INSTRUMENT CORPORATION	5
GULF & WESTERN INDUSTRIES, INC.	4
GTE AUTOMATIC ELECTRIC LABORATORIES INC.	4
GENERAL ELECTRIC COMPANY	4
NIPPON ELECTRIC CO., LTD.	4
SIEMENS AKTIENGESELLSCHAFT	4
COMPUTER AUTOMATION, INC.	4
OLIVETTI, ING. C., + C. S.P.A.	4*
SHARP KABUSHIKI KAISHA	3
BUNKER RAMO CORPORATION	3
ROCKWELL INTERNATIONAL CORPORATION	3
PLESSEY HANDEL UND INVESTMENTS AG	3
PITNEY-BOWES, INC.	3
RAYTHEON COMPANY	3*

*COMPOSITE TOTAL, SEE APPENDIX A

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

ACTION COMMUNICATION SYSTEMS, INC.
3825905 - BINARY SYNCHRONOUS COMMUNICATIONS PROCESSOR SYSTEM AND METHOD

AGENCE NATIONALE DE VALORISATION DE LA RECHERCHE (ANVAR)
4053871 - METHOD AND SYSTEM FOR THE ITERATIVE AND SIMULTANEOUS COMPARISON OF DATA WITH A GROUP OF REFERENCE DATA ITEMS

AGFA-GEVAERT, AG
3688661 - PHOTOGRAPHIC APPARATUS WITH AUTOMATICALLY AND MANUALLY ADJUSTABLE SHUTTER MEANS

ALLAN-BRADLEY COMPANY
4070702 - CONTACT HISTOGRAM FOR PROGRAMMABLE CONTROLLER

ALLEN-BRADLEY COMPANY
3753246 - PRINTER ADAPTED FOR OPERATION WITH A PROGRAMMABLE CONTROLLER
4118789 - PROGRAM PROTECTION MODULE FOR PROGRAMMABLE CONTROLLER
4122519 - DATA HANDLING MODULE FOR PROGRAMMABLE CONTROLLER
4158226 - PROGRAMMABLE CONTROLLER WITH LIMIT DETECTION
4172289 - PROGRAMMABLE CONTROLLER WITH PROGRAMMABLE I/O SCAN RATE

AMDAHL CORPORATION
3858183 - DATA PROCESSING SYSTEM AND METHOD THEREFOR
3866180 - HAVING AN INSTRUCTION PIPELINE FOR CONCURRENTLY PROCESSING A PLURALITY OF INSTRUCTIONS

AMF INCORPORATED
4092727 - BOWLING SCORER

AMSCO/MEDICAL ELECTRONICS, INC.
4053951 - DATA ACQUISITION, STORAGE AND DISPLAY SYSTEM

ARTHUR D. LITTLE INC.
4125871 - PORTABLE DATA ENTRY DEVICE

AUTOMATIC REVENUE CONTROLS (EUROPA) LTD.
4150437 - ATTENDANCE RECORDING SYSTEM

BELL + HOWELL COMPANY
4174890 - ELECTRONICALLY CONTROLLED MICROFILM PHOTOGRAPHIC IMAGE UTILIZATION DEVICE

BELL PUNCH COMPANY LIMITED
3585604 - CALCULATING MACHINES

BELL TELEPHONE LABORATORIES INCORPORATED
3543243 - DATA RECEIVING ARRANGEMENT
3568162 - DATA PROCESSING WITH DUAL FUNCTION LOGIC
3594730 - INFORMATION PROCESSING SYSTEM INCLUDING MULTIPLE FUNCTION TRANSLATORS
3747070 - DATA FIELD TRANSFER AND MODIFICATION APPARATUS
3748649 - TRANSLATOR MEMORY DECODING ARRANGEMENT FOR A MICROPROGRAM CONTROLLED PROCESSOR
3749845 - DIGITAL DATA COMMUNICATION SYSTEM
3867579 - SYNCHRONIZATION APPARATUS FOR A TIME DIVISION SWITCHING SYSTEM
4028678 - MEMORY PATCHING CIRCUIT
4028679 - MEMORY PATCHING CIRCUIT WITH INCREASED CAPABILITY
4028683 - MEMORY PATCHING CIRCUIT WITH COUNTER
4028684 - MEMORY PATCHING CIRCUIT WITH REPATCHING CAPABILITY
4034347 - METHOD AND APPARATUS FOR CONTROLLING A MULTIPROCESSOR SYSTEM
4071888 - TELEPHONE MULTILINE AUTOMATIC VOICE ANSWER SYSTEM
4103327 - INTERRUPT CONTROL CIRCUIT

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

BELL TELEPHONE LABORATORIES INCORPORATED (CONTINUED)
4164787 - MULTIPLE MICROPROCESSOR INTERCOMMUNICATION ARRANGEMENT

BENDIX CORPORATION
4164786 - APPARATUS FOR EXPANDING MEMORY SIZE AND DIRECT MEMORY ADDRESSING CAPABILITIES OF DIGITAL COMPUTER MEANS

BOLT BERANEK AND NEWMAN INC.
4130865 - MULTIPROCESSOR COMPUTER APPARATUS EMPLOYING DISTRIBUTED COMMUNICATIONS PATHS AND A PASSIVE TASK REGISTER

BUNKER RAMO CORPORATION
3602901 - CIRCUIT FOR CONTROLLING THE LOADING AND EDITING OF INFORMATION IN A RECIRCULATING MEMORY
4085442 - DATA DISPLAY SYSTEM DESIGNED AS A MICROCONTROLLER
4127896 - BIDIRECTIONAL INTERFACE UTILIZING READ-ONLY MEMORY, DECODER AND MULTIPLEXER

BURROUGHS CORPORATION
3482213 - DIGITAL DATA TRANSPARENT TRANSMISSION MEANS
3510843 - DIGITAL DATA TRANSMISSION SYSTEM HAVING MEANS FOR AUTOMATICALLY DETERMINING THE TYPES OF PERIPHERAL UNITS COMMUNICATING WITH THE SYSTEM
3512133 - DIGITAL DATA TRANSMISSION SYSTEM HAVING MEANS FOR AUTOMATICALLY SWITCHING THE STATUS OF INPUT-OUTPUT CONTROL UNITS
3514758 - DIGITAL COMPUTER SYSTEM HAVING MULTI-LINE CONTROL UNIT
3526878 - DIGITAL COMPUTER SYSTEM
3555513 - MULTI-PROCESSOR DIGITAL COMPUTER SYSTEM WITH ADDRESS MODIFICATION DURING PROGRAM EXECUTION
3609665 - APPARATUS FOR EXCHANGING INFORMATION BETWEEN A HIGH-SPEED MEMORY AND A LOW-SPEED MEMORY
3610903 - ELECTRONIC BARREL SWITCH FOR DATA SHIFTING
3665421 - INFORMATION PROCESSING SYSTEM IMPLEMENTING PROGRAM STRUCTURES COMMON TO HIGHER LEVEL PROGRAM LANGUAGES
3668644 - FAILSAFE MEMORY SYSTEM
3742459 - DATA PROCESSING METHOD AND APPARATUS ADAPTED TO SEQUENTIALLY PACK ERROR CORRECTING CHARACTERS INTO MEMORY LOCATIONS
3781812 - ADDRESSING SYSTEM RESPONSIVE TO A TRANSFER VECTOR FOR ACCESSING A MEMORY
3878514 - LSI PROGRAMMABLE PROCESSOR
3905023 - LARGE SCALE MULTI-LEVEL INFORMATION PROCESSING SYSTEM EMPLOYING IMPROVED FAILSAFT TECHNIQUES
3942163 - CCD STACK MEMORY ORGANIZATION
3952289 - CONTROLLER FOR LINKING A TYPEWRITER CONSOLE TO A PROCESSOR UNIT
3972024 - PROGRAMMABLE MICROPROCESSOR
3972025 - EXPANDED MEMORY PAGING FOR A PROGRAMMABLE MICROPROCESSOR
3978452 - SYSTEM AND METHOD FOR CONCURRENT AND PIPELINE PROCESSING EMPLOYING A DATA DRIVEN NETWORK
3980992 - MULTI-MICROPROCESSING UNIT ON A SINGLE SEMICONDUCTOR CHIP
3980993 - HIGH-SPEED/LOW-SPEED INTERFACE FOR DATA PROCESSING SYSTEMS
4007441 - METHOD OF DATA COMMUNICATIONS IN A HETEROGENOUS ENVIRONMENT
4051551 - MULTIDIMENSIONAL PARALLEL ACCESS COMPUTER MEMORY SYSTEM
4084154 - CHARGE COUPLED DEVICE MEMORY SYSTEM WITH BURST MODE
4101960 - SCIENTIFIC PROCESSOR
4128873 - STRUCTURE FOR AN EASILY TESTABLE SINGLE CHIP CALCULATOR/CONTROLLER
4139899 - SHIFT NETWORK HAVING A MASK GENERATOR AND A ROTATOR
4155118 - ORGANIZATION FOR AN INTEGRATED CIRCUIT CALCULATOR/CONTROLLER
4156277 - ACCESS REQUEST MECHANISM FOR A SERIAL DATA INPUT/OUTPUT SYSTEM
4156903 - DATA DRIVEN DIGITAL DATA PROCESSOR
4156908 - CURSIVE MECHANISM IN A DATA DRIVEN DIGITAL DATA PROCESSOR
4156909 - STRUCTURED DATA FILES IN A DATA DRIVEN DIGITAL DATA PROCESSOR
4156910 - NESTED DATA STRUCTURES IN A DATA DRIVEN DIGITAL DATA PROCESSOR
4177511 - PORT SELECT UNIT FOR A PROGRAMMABLE SERIAL-BIT MICROPROCESSOR

CALIFORNIA INSTITUTE OF TECHNOLOGY
3959774 - PROCESSOR WHICH SEQUENCES EXTERNALLY OF A CENTRAL PROCESSOR

CANON KABUSHIKI KAISHA
3815098 - ZERO SUPPRESSOR CIRCUIT

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

CANON KABUSHIKI KAISHA (CONTINUED)
4137563 - CIRCUITRY FOR REDUCING POWER DISSIPATION IN EQUIPMENT WHICH OPERATES IN SYNCHRONISM WITH CLOCK PULSES

CATERPILLAR TRACTOR CO.
4082224 - FUEL INJECTION NOZZLE

CENTRONICS DATA COMPUTER CORP.
3833891 - HIGH SPEED MATRIX PRINTER
4026402 - INCREMENTAL LINE PRINTER

CHARLES STARK DRAPER LABORATORY, INC.
4112488 - FAULT-TOLERANT NETWORK WITH NODE BRANCHING

CII HONEYWELL BULL (COMPAGNIE INTERNATIONALE POUR L INFORM
4125891 - ARRANGEMENT FOR PROTECTING DATA STORED IN A DIGITAL COMPUTER

CLEVELAND SPENCER
3976840 - PORTABLE SECURITIES SELECTOR SYSTEM

COGAR CORPORATION
3644899 - METHOD FOR DETERMINING PARTIAL MEMORY CHIP CATEGORIES
3659275 - MEMORY CORRECTION REDUNDANCY SYSTEM
3681757 - SYSTEM FOR UTILIZING DATA STORAGE CHIPS WHICH CONTAIN OPERATING AND NON-OPERATING STORAGE CELLS
3758759 - APPARATUS FOR DETERMINING PARTIAL MEMORY CHIP CATEGORIES
3805243 - APPARATUS AND METHOD FOR DETERMINING PARTIAL MEMORY CHIP CATAGORIES

COMPAGNIE HONEYWELL BULL
4084228 - PROCESS MANAGEMENT STRUCTURES AND HARDWARE/FIRMWARE CONTROL

COMPAGNIE INDUSTRIELLE DES TELECOMMUNICATIONS CIT-ALCATEL
3988718 - LOGIC CONTROL SYSTEM
4011544 - CONTROL SYSTEM HAVING A PROGRAMMED LOGIC UNIT

COMPTEURS-SCHLUMBERGER MONTROAGE
3852722 - STATIC REMOTE-CONTROL RELAY SELECTION SYSTEM

COMPUTER AUTOMATION, INC.
4025903 - AUTOMATIC MODULAR MEMORY ADDRESS ALLOCATION SYSTEM
4100601 - MULTIPLEXER FOR A DISTRIBUTED INPUT/OUT CONTROLLER SYSTEM
4124888 - PERIPHERAL-UNIT CONTROLLER APPARATUS
4124889 - DISTRIBUTED INPUT/OUTPUT CONTROLLER SYSTEM

CRAY RESEARCH, INC.
4128880 - COMPUTER VECTOR REGISTER PROCESSING

DATA GENERAL CORPORATION
3737866 - DATA STORAGE AND RETRIEVAL SYSTEM
3931613 - DATA PROCESSING SYSTEM
3990052 - CENTRAL PROCESSING UNIT EMPLOYING MICROPROGRAMMABLE CONTROL FOR USE IN A DATA PROCESSING SYSTEM
4014006 - DATA PROCESSING SYSTEM HAVING A UNIQUE CPU AND MEMORY TUNING RELATIONSHIP AND DATA PATH CONFIGURATION
4040032 - PERIPHERAL DEVICE CONTROLLER FOR A DATA PROCESSING SYSTEM
4047201 - I/O BUS TRANSCEIVER FOR A DATA PROCESSING SYSTEM
4047246 - I/O BUS TRANSCEIVER FOR A DATA PROCESSING SYSTEM
4048623 - DATA PROCESSING SYSTEM
4048673 - CPU - I/O BUS INTERFACE FOR A DATA PROCESSING SYSTEM
4056845 - MEMORY ACCESS TECHNIQUE

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

DATA GENERAL CORPORATION (CONTINUED)
4071890 - CPU-SYNCHRONOUS PARALLEL DATA PROCESSOR APPARATUS
4089052 - DATA PROCESSING SYSTEM
4104720 - CPU/PARALLEL PROCESSOR INTERFACE WITH MICROCODE EXTENSION

D.D.I. COMMUNICATIONS, INC.
3825695 - DIGITAL DATA INTERFACE SCANNING SYSTEM
3825696 - DIGITAL DATA INTERFACE SYSTEM

DELAWARE SDS, INC., MESNE
3702462 - COMPUTER INPUT-OUTPUT SYSTEM

DIGITAL COMPUTER CONTROLS, INC.
3934227 - MEMORY CORRECTION SYSTEM

DIGITAL EQUIPMENT CORPORATION
4045781 - MEMORY MODULE WITH SELECTABLE BYTE ADDRESSING FOR DIGITAL DATA PROCESSING SYSTEM
4156931 - DIGITAL DATA COMMUNICATIONS DEVICE WITH STANDARD OPTION CONNECTION

DIRKS ELECTRONICS CORPORATION
3815083 - METHOD AND ARRANGEMENT FOR SORTING RECORD UNITS HAVING KEYFIELD BITS ARRANGED IN DESCENDING ORDER OF SIGNIFICANCE WITHOU
T COMPARATOR

EDITEXT WORD PROCESSING, INC.
4051459 - STORED PROGRAM CONTROLLED TYPEWRITING/EDITING SYSTEM

ENGLISH ELECTRIC COMPUTERS LIMITED
3525985 - DATA HANDLING ARRANGEMENTS
3535697 - RESILIENT RAILWAY VEHICLE TRUCK SUSPENSION

ENVIRONMENTAL RESEARCH INSTITUTE OF MICHIGAN
4174514 - PARALLEL PARTITIONED SERIAL NEIGHBORHOOD PROCESSORS

EXCELLO CORPORATION
3832694 - PROCESSOR UNIT FOR DATA RETRIEVAL AND PROCESSING

FAIRCHILD CAMERA AND INSTRUMENT CORPORATION
3984670 - EXPANDABLE DIGITAL ARITHMETIC LOGIC REGISTER STACK
3984813 - MICROPROCESSOR SYSTEM
4086626 - MICROPROCESSOR SYSTEM
4106090 - MONOLITHIC MICROCOMPUTER CENTRAL PROCESSOR
4167781 - MICROPROCESSOR SYSTEM HAVING A SINGLE CENTRAL PROCESSING UNIT SHARED BY A PLURALITY OF SUBSYSTEMS EACH HAVING A MEMORY

FERRANTI LIMITED
4112487 - APPARATUS FOR WRITING DATA IN UNIQUE ORDER INTO AND RETRIEVING SAME FROM MEMORY

FLOATING POINT SYSTEMS, INC.
4075704 - FLOATING POINT DATA PROCESSOR FOR HIGH SPEECH OPERATION
4179734 - FLOATING POINT DATA PROCESSOR HAVING FAST ACCESS MEMORY MEANS

FOXBORO COMPANY
3761889 - COMPUTER DIRECTED PROCESS CONTROL SYSTEM WITH ANALOG INPUT MULTIPLEXER

FREEDMAN ARTCRAFT ENGINEERING CORPORATION
3788717 - DISPLAY FIXTURE

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

FUJITSU LIMITED
4145749 - LOG IN-OUT SYSTEM FOR LOGIC APPARATUS
4167780 - DATA PROCESSING UNIT HAVING SCAN-IN AND SCAN-OUT MEANS

GENERAL ATOMIC COMPANY
4143283 - BATTERY BACKUP SYSTEM

GENERAL ELECTRIC COMPANY
3470537 - INFORMATION PROCESSING SYSTEM USING RELATIVE ADDRESSING
3500336 - MEANS FOR EXTRACTING SYNCHRONIZING SIGNALS FROM TELEVISION VIDEO SIGNALS
3569940 - REMOTE ALARM FOR VISUAL DISPLAY TERMINALS
4168531 - REAL-TIME CLOCK HAVING PROGRAMMABLE TIME INITIALIZATION AND READ-OUT

GTE AUTOMATIC ELECTRIC LABORATORIES INCORPORATED
3750111 - MODULAR DIGITAL DETECTOR CIRCUIT ARRANGEMENT
3786436 - MEMORY EXPANSION ARRANGEMENT IN A CENTRAL PROCESSOR
3978455 - I/O STRUCTURE FOR MICROPROCESSOR IMPLEMENTED SYSTEMS
3986170 - MODULAR CONTROL SYSTEM DESIGN WITH MICROPROCESSORS

GULF + WESTERN INDUSTRIES, INC.
4078259 - PROGRAMMABLE CONTROLLER HAVING A SYSTEM FOR MONITORING THE LOGIC CONDITIONS AT EXTERNAL LOCATIONS
4093998 - PROGRAMMING MODULE FOR PROGRAMMABLE CONTROLLER USING A MICROPROCESSOR
4107785 - PROGRAMMABLE CONTROLLER USING MICROPROCESSOR

HALLIBURTON COMPANY
3760362 - OIL FIELD PRODUCTION AUTOMATION METHOD AND APPARATUS

HARRIS CORPORATION
4014004 - AUTOMATIC REPORT REGISTER
4016545 - PLURAL MEMORY CONTROLLER APPARATUS

HARRIS DATA COMMUNICATIONS, INC.
4115852 - MICROPROGRAMMED CONTROLLER

HAWKER SIDDELEY DYNAMICS LIMITED
3983537 - RELIABILITY OF RANDOM ACCESS MEMORY SYSTEMS

HEWLETT-PACKARD COMPANY
3855461 - CALCULATOR WITH KEY CODE ASSOCIATION AND DISPLAY FEATURES
3891972 - SYNCHRONOUS SEQUENTIAL CONTROLLER FOR LOGIC OUTPUTS
3971925 - ADAPTABLE PROGRAMMED CALCULATOR HAVING PROVISION FOR PLUG-IN KEYBOARD AND MEMORY MODULES
4028538 - PROGRAMMABLE CALCULATOR EMPLOYING ALGEBRAIC LANGUAGE
4028675 - METHOD AND APPARATUS FOR REFRESHING SEMICONDUCTOR MEMORIES IN MULTI-PORT AND MULTI-MODULE MEMORY SYSTEM
4152769 - PROGRAMMABLE CALCULATOR INCLUDING MEANS FOR PERMITTING DATA ENTRY DURING PROGRAM EXECUTION
4152770 - PROGRAMMABLE CALCULATOR INCLUDING MEANS FOR PROGRAMMABLY CONTROLLING MAGNETIC STORAGE UNITS
4152771 - PROGRAMMABLE CALCULATOR INCLUDING DISPLAY MEANS FOR SIGNALLING THE USER TO INDICATE THE EXHAUSTION OF A PRINTER PAPER SUPPLY
4156282 - PROGRAMMABLE CALCULATOR INCLUDING RELATIONAL OPERATOR MEANS
4156917 - PROGRAMMABLE CALCULATOR INCLUDING SEPARATE USER PROGRAM AND DATA MEMORY AREAS
4156918 - PROGRAMMABLE CALCULATOR INCLUDING MEANS FOR PERFORMING COMPUTED JUMPS DURING PROGRAM EXECUTION
4158228 - PROGRAMMABLE CALCULATOR INCLUDING ALPHANUMERIC ERROR DISPLAY MEANS
4158231 - PROGRAMMABLE CALCULATOR INCLUDING PROGRAM LISTING MEANS
4159525 - PROGRAMMABLE CALCULATOR EMPLOYING COMPUTED MEMORY ADDRESSES
4161031 - PROGRAMMABLE CALCULATOR INCLUDING BOOLEAN FLAG VARIABLE MEANS
4162532 - PROGRAMMABLE CALCULATOR INCLUDING DATA FORMAT DISPLAY CONTROL MEANS
4164019 - PROGRAMMABLE CALCULATOR INCLUDING ALPHANUMERIC DISPLAY MEANS

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

HITACHI, LTD.
3618040 - MEMORY CONTROL APPARATUS IN MULTI-PROCESSOR SYSTEM
3947822 - PROCESSOR OF MICRO-COMPUTER WITH DIVISION OF MICRO-INSTRUCTION
3999165 - INTERRUPT INFORMATION INTERFACE SYSTEM
4037212 - INFORMATION PROCESSING SYSTEM
4057845 - GROUP CONTROL SYSTEM FOR VISUAL INFORMATION PROCESSING
4096564 - DATA PROCESSING SYSTEM WITH INTERRUPT FUNCTIONS
4149264 - CRT DISPLAY APPARATUS OF RASTER SCANNING TYPE
4156904 - COMPUTER SYSTEMS HAVING A COMMON MEMORY SHARED BETWEEN A CENTRAL PROCESSOR AND A CRT DISPLAY
4156928 - PROGRAMMABLE TELEVISION GAME AND TRAINING SYSTEM WITH ADAPTABLE OPERATOR CONTROL

HOHNER MATTH AG
3914746 - ELECTRONIC DATA-PROCESSING SYSTEM AND METHOD OF OPERATING SAME

HONEYWELL INC.
3582902 - DATA PROCESSING SYSTEM HAVING AUXILIARY REGISTER STORAGE
3618026 - CHARACTER GENERATOR
3633175 - DEFECT-TOLERANT DIGITAL MEMORY SYSTEM
3651472 - MULTI STATE FLIP-FLOP ELEMENT INCLUDING A LOCAL MEMORY FOR USE IN CONSTRUCTING A DATA PROCESSING SYSTEM
4017841 - BUS ALLOCATION CONTROL APPARATUS
4028669 - PRINTER CONTROL SYSTEM
4153943 - HIGH SPEED I/O FOR CONTENT ADDRESSABLE TYPE MEMORIES
4155115 - PROCESS CONTROL SYSTEM WITH ANALOG OUTPUT CONTROL CIRCUIT
4172280 - DIGITAL OUTPUT CONTROL CIRCUIT

HONEYWELL INFORMATION SYSTEMS INC.
3728688 - LINE PRINTER TIME SHARED ELECTRONICS
3753236 - MICROPROGRAMMABLE PERIPHERAL CONTROLLER
3755788 - DATA RECIRCULATOR
3757310 - MEMORY ADDRESS SELECTION APPARATUS INCLUDING ISOLATION CIRCUITS
3813650 - METHOD FOR FABRICATING AND ASSEMBLING A BLOCK-ADDRESSABLE SEMICONDUCTOR MASS MEMORY
3840862 - STATUS INDICATOR APPARATUS FOR TAG DIRECTORY IN ASSOCIATIVE STORES
3866183 - COMMUNICATIONS CONTROL APPARATUS FOR THE USE WITH A CACHE STORE
3882470 - MULTIPLE REGISTER VARIABLY ADDRESSABLE SEMICONDUCTOR MASS MEMORY
3896419 - CACHE MEMORY STORE IN A PROCESSOR OF A DATA PROCESSING SYSTEM
3909800 - IMPROVED MICROPROGRAMMED PERIPHERAL PROCESSING SYSTEM
3916385 - RING CHECKING HARDWARE
3986172 - CCD REGISTER INTERFACE WITH PARTIAL-WRITE MODE
4024508 - DATABASE INSTRUCTION FIND SERIAL
4024509 - CCD REGISTER ARRAY ADDRESSING SYSTEM INCLUDING APPARATUS FOR BY-PASSING SELECTED ARRAYS
4025901 - DATABASE INSTRUCTION FIND OWNER
4042914 - MICROPROGRAMMED CONTROL OF FOREIGN PROCESSOR CONTROL FUNCTIONS
4044334 - DATABASE INSTRUCTION UNLOAD
4060794 - APPARATUS AND METHOD FOR GENERATING TIMING SIGNALS FOR LATCHED TYPE MEMORIES
4068299 - DATA PROCESSING SYSTEM INCORPORATING A LOGICAL COMPARE INSTRUCTION
4068300 - DATA PROCESSING SYSTEM UTILIZING DATA FIELD DESCRIPTORS FOR PROCESSING DATA FILES
4118773 - MICROPROGRAM MEMORY BANK ADDRESSING SYSTEM
4130867 - DATABASE INSTRUCTION APPARATUS FOR DETERMINING A DATABASE RECORD TYPE
4157587 - HIGH SPEED BUFFER MEMORY SYSTEM WITH WORD PREFETCH
4159532 - FIFO LOOK-AHEAD SYSTEM
4161784 - MICROPROGRAMMABLE FLOATING POINT ARITHMETIC UNIT CAPABLE OF PERFORMING ARITHMETIC OPERATIONS ON LONG AND SHORT OPERANDS
4167782 - CONTINUOUS UPDATING OF CACHE STORE

HONEYWELL INFORMATION SYSTEMS ITALIA
4041473 - COMPUTER INPUT/OUTPUT CONTROL APPARATUS

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

HUGHES AIRCRAFT COMPANY
3745532 - MODULAR DIGITAL PROCESSING EQUIPMENT
4075688 - SYSTEM FOR ADDRESSING AND ADDRESS INCREMENTING OF ARITHMETIC UNIT SEQUENCE CONTROL SYSTEM

ING. C. OLIVETTI & C., S.P.A.
4114026 - ELECTRONIC DESK-TOP ACCOUNTING MACHINE AND CALCULATOR
4156290 - SPEEDUP ADDRESSING DEVICE BY DETECTING REPETITIVE ADDRESSING
4179735 - COMPUTER WITH AN ARRANGEMENT FOR CHANGING ITS WORKING ENVIRONMENT

INTEL CORPORATION
3821715 - MEMORY SYSTEM FOR A MULTI-CHIP DIGITAL COMPUTER
4010449 - MOS COMPUTER EMPLOYING A PLURALITY OF SEPARATE CHIPS
4099236 - SLAVE MICROPROCESSOR FOR OPERATION WITH A MASTER MICROPROCESSOR AND A DIRECT MEMORY ACCESS CONTROLLER
4112490 - DATA TRANSFER CONTROL APPARATUS AND METHOD
4152761 - MULTI-TASK DIGITAL PROCESSOR EMPLOYING A PRIORITY
4153933 - SINGLE CHIP MOS COMPUTER WITH EXPANDABLE MEMORY

INTERNATIONAL BUSINESS MACHINES CORPORATION
3432812 - MEMORY SYSTEM
3449723 - CONTROL SYSTEM FOR INTERLEAVE MEMORY
3449724 - CONTROL SYSTEM FOR INTERLEAVE
3462744 - EXECUTION UNIT WITH A COMMON OPERAND AND RESULT BUSSING SYSTEM
3466611 - MULTI-WORD MULTI-DIRECTIONAL RANDOM ACCESS MEMORY SYSTEM
3500337 - DATA HANDLING SYSTEM EMPLOYING A FULL WORD MAIN MEMORY TRANSFER WITH INDIVIDUAL INDIRECT BYTE ADDRESSING AND PROCESSING
3533077 - ADDRESS MODIFICATION
3541518 - DATA HANDLING APPARATUS EMPLOYING AN ACTIVE STORAGE DEVICE WITH PLURAL SELECTIVE READ AND WRITE PATHS
3566363 - PROCESSOR TO PROCESSOR COMMUNICATION IN A MULTI- PROCESSOR COMPUTER SYSTEM
3585599 - UNIVERSAL SYSTEM SERVICE ADAPTER
3588830 - SYSTEM FOR USING A MEMORY HAVING IRREMEDIABLE BAD BITS
3593299 - INPUT-OUTPUT CONTROL SYSTEM FOR DATA PROCESSING APPARATUS
3623016 - ELECTRONIC KEYBOARD
3631229 - MONOLITHIC MEMORY ARRAY TESTER
3648246 - DECIMAL ADDITION EMPLOYING TWO SEQUENTIAL PASSES THROUGH A BINARY ADDER IN ONE BASIC MACHINE CYCLE
3648254 - HIGH SPEED ASSOCIATIVE MEMORY
3648255 - AUXILIARY STORAGE APPARATUS
3651475 - ADDRESS MODIFICATION BY MAIN/CONTROL STORE BOUNDRY REGISTER IN A MICROPROGRAMMED PROCESSOR
3651476 - PROCESSOR WITH IMPROVED CONTROLS FOR SELECTING AN OPERAND FROM A LOCAL STORAGE UNIT, AN ALU OUTPUT REGISTER OR BOTH
3654622 - AUXILIARY STORAGE APPARATUS WITH CONTINUOUS DATA TRANSFER
3700873 - STRUCTURED COMPUTER NOTATION AND SYSTEM ARCHITECTURE UTILIZING SAME
3735368 - FULL CAPACITY MONOLITHIC MEMORY UTILIZING DEFECTIVE STORAGE CELLS
3736574 - PSEUDO-HIERARCHY MEMORY SYSTEM
3737870 - STATUS SWITCHING ARRANGEMENT
3740723 - INTEGRAL HIERARCHICAL BINARY STORAGE ELEMENT
3753244 - YIELD ENHANCEMENT REDUNDANCY TECHNIQUE
3755791 - MEMORY SYSTEM WITH TEMPORARY OR PERMANENT SUBSTITUTION OF CELLS FOR DEFECTIVE CELLS
3760368 - VECTOR INFORMATION SHIFTING ARRAY
3760369 - DISTRIBUTED MICROPROGRAM CONTROL IN AN INFORMATION HANDLING SYSTEM
3764742 - CRYPTOGRAPHIC IDENTIFICATION SYSTEM
3765001 - ADDRESS TRANSLATION LOGIC WHICH PERMITS A MONOLITHIC MEMORY TO UTILIZE DEFECTIVE STORAGE CELLS
3766534 - SHIFT REGISTER STORAGE UNIT WITH MULTI-DIMENSIONAL DYNAMIC ORDERING
3781826 - MONOLITHIC MEMORY UTILIZING DEFECTIVE STORAGE CELLS
3798606 - BIT PARTITIONED MONOLITHIC CIRCUIT COMPUTER SYSTEM
3806888 - HIERACHICAL MEMORY SYSTEM
3806891 - LOGIC CIRCUIT FOR SCAN-IN/SCAN-OUT
3811117 - TIME ORDERED MEMORY SYSTEM AND OPERATION
3840863 - DYNAMIC STORAGE HIERARCHY SYSTEM

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

INTERNATIONAL BUSINESS MACHINES CORPORATION (CONTINUED)
3905025 - DATA ACQUISITION AND CONTROL SYSTEM INCLUDING DYNAMIC INTERRUPT CAPABILITY
3919695 - ASYNCHRONOUS CLOCKING APPARATUS
3943494 - DISTRIBUTED EXECUTION PROCESSOR
3967263 - TEXT EDITING SYSTEM
3983538 - UNIVERSAL LSI ARRAY LOGIC MODULES WITH INTEGRAL STORAGE ARRAY AND VARIABLE AUTONOMOUS SEQUENCING
3991408 - SELF-SEQUENCING MEMORY
4008460 - CIRCUIT FOR IMPLEMENTING A MODIFIED LRU REPLACEMENT ALGORITHM FOR A CACHE
4020470 - SIMULTANEOUS ADDRESSING OF DIFFERENT LOCATIONS IN A STORAGE UNIT
4024510 - FUNCTION MULTIPLEXER
4032899 - APPARATUS AND METHOD FOR SWITCHING OF DATA
4038641 - COMMON POLLING LOGIC FOR INPUT/OUTPUT INTERRUPT OR CYCLE STEAL DATA TRANSFER REQUESTS
4051353 - ACCORDION SHIFT REGISTER AND ITS APPLICATION IN THE IMPLEMENTATION OF LEVEL SENSITIVE LOGIC SYSTEM
4052699 - HIGH SPEED REAL TIME IMAGE TRANSFORMATION
4057846 - BUS STEERING STRUCTURE FOR LOW COST PIPELINED PROCESSOR SYSTEM
4063078 - CLOCK GENERATION NETWORK FOR LEVEL SENSITIVE LOGIC SYSTEM
4063308 - AUTOMATIC CLOCK TUNING AND MEASURING SYSTEM FOR LSI COMPUTERS
4071902 - REDUCED OVERHEAD FOR CLOCK TESTING IN A LEVEL SYSTEM SCAN DESIGN (LSSD) SYSTEM
4078254 - HIERARCHICAL MEMORY WITH DEDICATED HIGH SPEED BUFFERS
4084230 - HYBRID SEMICONDUCTOR MEMORY WITH ON-CHIP ASSOCIATIVE PAGE ADDRESSING, PAGE REPLACEMENT AND CONTROL
4086658 - INPUT/OUTPUT AND DIAGNOSTIC ARRANGEMENTS FOR PROGRAMMABLE MACHINE CONTROLLERS HAVING MULTIPROGRAMMING CAPABILITIES
4090249 - APPARATUS FOR SORTING RECORDS IN OVERLAP RELATION WITH RECORD LOADING AND EXTRACTION
4093982 - MICROPROCESSOR SYSTEM
4095265 - MEMORY CONTROL STRUCTURE FOR A PIPELINED MINI-PROCESSOR SYSTEM
4095270 - METHOD OF IMPLEMENTING MANUAL OPERATIONS
4096578 - DATA SYSTEM WITH MICROPROCESSOR FEATURING MULTIPLEXED DATA TRANSFER AND REPEAT CYCLE DRIVING ARRANGEMENT
4100597 - COMPUTER CONTROLLED DISTRIBUTION APPARATUS FOR DISTRIBUTING TRANSACTIONS TO AND FROM CONTROLLED MACHINE TOOLS HAVING MEA
NS INDEPENDENT OF THE COMPUTER FOR COMPLETING OR STOPPING A TOOL FUNCTION INITIATED BY A COMPUTER TRANSACTION
4110830 - CHANNEL STORAGE ADAPTER
4110837 - APPARATUS FOR THE SORTING OF RECORDS OVERLAPPED WITH LOADING AND UNLOADING OF RECORDS INTO A STORAGE APPARATUS
4128876 - SYNCHRONOUS MICROCODE GENERATED INTERFACE FOR SYSTEM OF MICROCODED DATA PROCESSORS
4128891 - MAGNETIC BUBBLE DOMAIN RELATIONAL DATA BASE SYSTEM
4141005 - DATA FORMAT CONVERTING APPARATUS FOR USE IN A DIGITAL DATA PROCESSOR
4144563 - MICROPROCESSOR SYSTEM
4157454 - METHOD AND SYSTEM FOR MACHINE ENCIPHERING AND DECIPHERING
4171536 - MICROPROCESSOR SYSTEM

INTERNATIONAL COMPUTERS LIMITED
3993980 - SYSTEM FOR HARD WIRING INFORMATION INTO INTEGRATED CIRCUIT ELEMENTS
4112489 - DATA PROCESSING SYSTEMS

INTERNATIONAL TELEPHONE AND TELEGRAPH CORPORATION
4001789 - MICROPROCESSOR BOOLEAN PROCESSOR

ISRAEL ELECTRO-OPTICAL INDUSTRY LTD.
4161035 - CIRCUITRY FOR DISPLAYING A CONSTANTLY CHANGING M-MODE OUTPUT ON A RASTER SCAN DISPLAY

KANEBO LTD.
4078253 - PATTERN GENERATING SYSTEM

KEARNEY + TRECKER CORPORATION
4120030 - COMPUTER SOFTWARE SECURITY SYSTEM

KENWAY INCORPORATED
4052702 - CIRCUIT FOR INTERFACING MICROCOMPUTER TO PERIPHERAL DEVICES

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

LEXICON CORPORATION
4158236 - ELECTRONIC DICTIONARY AND LANGUAGE INTERPRETER

LICENTIA PATENT-VERWALTUNGS-GMBH
3772652 - DATA STORAGE SYSTEM WITH MEANS FOR ELIMINATING DEFECTIVE STORAGE LOCATIONS

LITTON SYSTEMS INC.
3988717 - GENERAL PURPOSE COMPUTER OR LOGIC CHIP AND SYSTEM

MANGOOD CORPORATION
3959636 - BATCHING SYSTEM

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
4130885 - PACKET MEMORY SYSTEM FOR PROCESSING MANY INDEPENDENT MEMORY TRANSACTIONS CONCURRENTLY
4174536 - DIGITAL COMMUNICATIONS CONTROLLER WITH FIRMWARE CONTROL

MATSUSHITA ELECTRIC WORKS, LTD.
4023152 - IONIZATION TYPE SMOKE SENSING DEVICE

MCDONNELL DOUGLAS CORPORATION
4149235 - COMPUTER NUMERICAL CONTROL SYSTEM FOR MACHINE TOOL

MITSUBISHI DENKI KABUSHIKI KAISHA
4071889 - CENTRAL PROCESSING APPARATUS FOR GENERATING AND RECEIVING TIME DIVISION MULTIPLEX SIGNALS

MODICON CORPORATION
3944984 - COMPUTER CONTROLLER SYSTEM WITH A REPROGRAMMABLE READ ONLY MEMORY
3959776 - PROGRAMMABLE PRINTER

MONARCH MARKING SYSTEMS, INC.
4019174 - DATA COLLECTING AND TRANSMITTING SYSTEM

MOS TECHNOLOGY, INC.
3941989 - REDUCING POWER CONSUMPTION IN CALCULATORS
4099232 - INTERVAL TIMER ARRANGEMENT IN A MICROPROCESSOR SYSTEM

MOTOROLA INC.
3962682 - SPLIT LOW ORDER INTERNAL ADDRESS BUS FOR MICROPROCESSOR
3968478 - CHIP TOPOGRAPHY FOR MOS INTERFACE CIRCUIT
3975712 - ASYNCHRONOUS COMMUNICATION INTERFACE ADAPTOR
3979732 - ASYNCHRONOUS STATUS INTERLOCK CIRCUIT FOR INTERFACE ADAPTOR
3987418 - CHIP TOPOGRAPHY FOR MOS INTEGRATED CIRCUITRY MICROPROCESSOR CHIP
4003028 - INTERRUPT CIRCUITRY FOR MICROPROCESSOR CHIP
4004281 - MICROPROCESSOR CHIP REGISTER BUS STRUCTURE
4004283 - MULTIPLE INTERRUPT MICROPROCESSOR SYSTEM
4010448 - INTERRUPT CIRCUITRY FOR MICROPROCESSOR CHIP
4016546 - BUS SWITCH COUPLING FOR SERIES-COUPLED ADDRESS BUS SECTIONS IN A MICROPROCESSOR
4020472 - MASTER SLAVE REGISTERS FOR INTERFACE ADAPTOR
4030079 - PROCESSOR INCLUDING INCREMENTOR AND PROGRAM REGISTER STRUCTURE
4032896 - MICROPROCESSOR HAVING INDEX REGISTER COUPLED TO SERIAL-COUPLED ADDRESS BUS SECTIONS AND TO DATA BUS
4037204 - MICROPROCESSOR INTERRUPT LOGIC
4040035 - MICROPROCESSOR HAVING INDEX REGISTER COUPLED TO SERIAL-COUPLED ADDRESS BUS SECTIONS AND TO DATA BUS
4050096 - PULSE EXPANDING SYSTEM FOR MICROPROCESSOR SYSTEMS WITH SLOW MEMORY
4069510 - INTERRUPT STATUS REGISTER FOR INTERFACE ADAPTOR CHIP
4071887 - SYNCHRONOUS SERIAL DATA ADAPTOR
4086627 - INTERRUPT SYSTEM FOR MICROPROCESSOR SYSTEM

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

MOTOROLA INC. (CONTINUED)
4087855 - VALID MEMORY ADDRESS ENABLE SYSTEM FOR A MICROPROCESSOR SYSTEM
4090236 - N-CHANNEL FIELD EFFECT TRANSISTOR INTEGRATED CIRCUIT MICROPROCESSOR REQUIRING ONLY ONE EXTERNAL POWER SUPPLY
4106091 - INTERRUPT STATUS INDICATION LOGIC FOR POLLED INTERRUPT DIGITAL SYSTEM
4122304 - CONTROL CIRCUITRY FOR A RADIO TELEPHONE
4128872 - HIGH SPEED DATA SHIFTER ARRAY
4145751 - DATA DIRECTION REGISTER FOR INTERFACE ADAPTOR CHIP
4149263 - PROGRAMMABLE MULTI-BIT SHIFTER
4153942 - INDUSTRIAL CONTROL PROCESSOR
4159520 - MEMORY ADDRESS CONTROL DEVICE WITH EXTENDER BUS

NATIONAL SEMICONDUCTOR CORPORATION
3978328 - POCKET CALCULATOR
4171537 - NUMBER ORIENTED PROCESSOR

NCR CORPORATION
3631402 - INPUT AND OUTPUT CIRCUITRY
3668661 - CHARACTER CODING, MEMORY, AND DISPLAY SYSTEM
3702988 - DIGITAL PROCESSOR
3713107 - FIRMWARE SORT PROCESSOR SYSTEM
4144562 - SYSTEM AND METHOD FOR INCREASING MICROPROCESSOR OUTPUT DATA RATE
4146922 - CONSTANT VELOCITY DRIVING MEANS
4156905 - METHOD AND APPARATUS FOR IMPROVING ACCESS SPEED IN A RANDOM ACCESS MEMORY
4159526 - DIGITALLY CONTROLLED VARIABLE FREQUENCY OSCILLATOR
4177515 - INTERRUPT ADAPTER FOR DATA PROCESSING SYSTEMS

NESTOR ASSOCIATES
3950733 - INFORMATION PROCESSING SYSTEM

NIPPON ELECTRIC CO., LTD.
3689895 - MICRO-PROGRAM CONTROL SYSTEM
3932844 - COMMON CONTROL SWITCHING SYSTEM
4027292 - SYNCHRONOUS DATA PROCESSING SYSTEM HAVING ARITHMETIC AND CONTROL UNITS CONTROLLED BY SINGLE-PHASE CLOCK PULSES
4157457 - FREQUENCY ANALYZER COMPRISING A DIGITAL BAND-PASS AND A DIGITAL LOW-PASS FILTER SECTION BOTH OPERABLE IN A TIME-DIVISION FASHION

NIPPON TELEGRAPH AND TELEPHONE PUBLIC CORPORATION
4051460 - APPARATUS FOR ACCESSING AN INFORMATION STORAGE DEVICE HAVING DEFECTIVE MEMORY CELLS

NIXDORF COMPUTER AG
4162519 - DATA PROCESSOR WITH ADDRESS ALLOCATION TO OPERATIONS

NORLIN MUSIC, INC.
4118791 - MULTI-LEVEL ENCODING SYSTEM

NORTH ELECTRIC COMPANY
3727192 - CENTRAL PROCESSING SYSTEM HAVING PRELOADER AND DATA HANDLING UNITS EXTERNAL TO THE PROCESSOR CONTROL UNIT

NORTHERN ELECTRIC COMPANY LIMITED
4150428 - METHOD FOR PROVIDING A SUBSTITUTE MEMORY IN A DATA PROCESSING SYSTEM

NUGRAPHICS, INC.
4070710 - RASTER SCAN DISPLAY APPARATUS FOR DYNAMICALLY VIEWING IMAGE ELEMENTS STORED IN A RANDOM ACCESS MEMORY ARRAY

OLIVETTI, ING. C., + C. S.P.A.
3939452 - DESK-TOP ELECTRONIC COMPUTER WITH MOS CIRCUIT LOGIC

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

OLYMPIA WERKE AG
3879713 - TRANSMISSION OF SIGNALS BETWEEN A DATA PROCESSING SYSTEM AND INPUT AND OUTPUT UNITS
3972028 - DATA PROCESSING SYSTEM INCLUDING A PLURALITY OF MEMORY CHIPS EACH PROVIDED WITH ITS OWN ADDRESS REGISTER
3975714 - DATA PROCESSING SYSTEM INCLUDING AN LSI CHIP CONTAINING A MEMORY AND ITS OWN ADDRESS REGISTER
4004282 - CIRCUIT ARRANGEMENT FOR AN INTEGRATED DATA PROCESSING SYSTEM COMPOSED OF A SMALL NUMBER OF DIFFERENT CHIP TYPES WITH ALL CHIPS DIRECTLY CONNECTABLE TO A COMMON COLLECTING BUS
4028682 - CIRCUIT ARRANGEMENT FOR SELECTING THE FUNCTION OF CONNECTION CONTACTS ON CIRCUIT CHIPS

PANAFACOM LIMITED
4128881 - SHARED MEMORY ACCESS CONTROL SYSTEM FOR A MULTIPROCESSOR SYSTEM

PITNEY-BOWES, INC.
3978457 - MICROCOMPUTERIZED ELECTRONIC POSTAGE METER SYSTEM
4135662 - OPERATOR PROMPTING SYSTEM
4168533 - MICROCOMPUTERIZED MINIATURE POSTAGE METER

PLESSEY HANDEL UND INVESTMENTS AG
4068305 - ASSOCIATIVE PROCESSORS
4121286 - DATA PROCESSING MEMORY SPACE ALLOCATION AND DEALLOCATION ARRANGEMENTS
4167040 - TAXIMETER INDICATING DEVICES

POST OFFICE
4146929 - INPUT/OUTPUT SECURITY SYSTEM FOR DATA PROCESSING EQUIPMENT

PYE LIMITED
4063310 - SAMPLER CONTROL SYSTEM FOR CHROMATOGRAPH ANALYTICAL APPARATUS

RAYTHEON COMPANY
4069511 - DIGITAL BIT IMAGE MEMORY SYSTEM

RAYTHEON CORPORATION
3579201 - METHOD OF PERFORMING DIGITAL COMPUTATIONS USING MULTIPURPOSE INTEGRATED CIRCUITS AND APPARATUS THEREFOR
3699535 - MEMORY LOOK AHEAD CONNECTION ARRANGEMENT FOR WRITING INTO AN UNOCCUPIED ADDRESS AND PREVENTION OF READING OUT FROM AN EMPTY ADDRESS

RCA CORPORATION
3460094 - INTEGRATED MEMORY SYSTEM
3462742 - COMPUTER SYSTEM ADAPTED TO BE CONSTRUCTED OF LARGE INTEGRATED CIRCUIT ARRAYS
3798615 - COMPUTER SYSTEM WITH PROGRAM-CONTROLLED PROGRAM COUNTERS
3943347 - DATA PROCESSOR REORDER RANDOM ACCESS MEMORY
3970998 - MICROPROCESSOR ARCHITECTURE
4040029 - MEMORY SYSTEM WITH REDUCED BLOCK DECODING
4087626 - SCRAMBLER AND UNSCRAMBLER FOR SERIAL DATA
4092728 - PARALLEL ACCESS MEMORY SYSTEM

R. C. SANDERS TECHNOLOGY SYSTEMS, INC.
4159882 - HIGH QUALITY PRINTER

RELIANCE ELECTRIC COMPANY
4021783 - PROGRAMMABLE CONTROLLER

ROCKWELL INTERNATIONAL CORPORATION
3965459 - SELECTABLE EIGHT OR TWELVE DIGIT INTEGRATED CIRCUIT CALCULATOR AND CONDITIONAL GATE OUTPUT SIGNAL MODIFICATION CIRCUIT THEREFOR
4136400 - MICRO-PROGRAMMABLE DATA TERMINAL
4159535 - FRAMING AND ELASTIC STORE CIRCUIT APPARATUS

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

SANDERS ASSOCIATES INC.
3613054 - SCANNING ENCODER
3932842 - COMPUTER TERMINAL

SEEBURG CORPORATION
4058316 - ELECTRONIC CONTROL AND TEST CIRCUIT FOR PINBALL TYPE GAMES

SHARP KABUSHIKI KAISHA
3571808 - DECIMAL POINT PROCESSING APPARATUS
4020467 - MINIATURIZED KEY ENTRY AND TRANSLATION CIRCUITRY ARRANGEMENT FOR A DATA PROCESSING UNIT
4090245 - EFFECTIVE DIGIT CAPACITY MODIFICATION MEANS FOR INTEGRATED CIRCUIT CALCULATORS

SIEMENS AKTIENGESELLSCHAFT
3974366 - INTEGRATED, PROGRAMMABLE LOGIC ARRANGEMENT
4005389 - ARRANGEMENT FOR REDUCING THE ACCESS TIME IN A STORAGE SYSTEM
4037089 - INTEGRATED PROGRAMMABLE LOGIC ARRAY
4133029 - DATA PROCESSING SYSTEM WITH TWO OR MORE SUBSYSTEMS HAVING COMBINATIONAL LOGIC UNITS FOR FORMING DATA PATHS BETWEEN PORTI
ONS OF THE SUBSYSTEMS

SINGER COMPANY
4106105 - ZERO DETECTOR
4143417 - PORTABLE DATA-GATHERING APPARATUS FORMED BY MODULAR COMPONENTS HAVING OPERATE-STANDBY MODES

SMITHKLINE CORPORATION
3945379 - INJECTION DEVICE

SOCIETE LANNIONNAISE D ELECTRONIQUE SLE-CITEREL
3999162 - TIME-DIVISION MULTIPLEX SWITCHING CIRCUITRY

SPECIALIZED ELECTRONICS INC.
3979058 - OPERATOR PROMPTING SYSTEM FOR STORED PROGRAM CALCULATOR

SPERRY RAND CORPORATION
3530438 - TASK CONTROL
3567914 - AUTOMATED MANUFACTURING SYSTEM
3739349 - DIGITAL EQUIPMENT INTERFACE UNIT
3848234 - MULTI-PROCESSOR SYSTEM WITH MULTIPLE CACHE MEMORIES
3889237 - COMMON STORAGE CONTROLLER FOR DUAL PROCESSOR SYSTEM
3906461 - INTEGRATED MNOS MEMORY WITH DECODER
4001786 - AUTOMATIC CONFIGURATION OF MAIN STORAGE ADDRESSING RANGES
4003032 - AUTOMATIC TERMINAL AND LINE SPEED DETECTOR
4034349 - APPARATUS FOR PROCESSING INTERRUPTS IN MICROPROCESSING SYSTEMS
4057847 - REMOTE CONTROLLED TEST INTERFACE UNIT
4058851 - CONDITIONAL BYPASS OF ERROR CORRECTION FOR DUAL MEMORY ACCESS TIME SELECTION
4064556 - PACKED LOOP MEMORY WITH DATA MANIPULATION CAPABILITIES
4067059 - SHARED DIRECT MEMORY ACCESS CONTROLLER
4112502 - CONDITIONAL BYPASS OF ERROR CORRECTION FOR DUAL MEMORY ACCESS TIME SELECTION
4160124 - MULTIPLE DIAL ADAPTER

SQUARE D COMPANY
3950736 - PROGRAMMABLE SOLID STATE CONTROL FOR MACHINE TOOL OR PROCESS CONTROL SYSTEMS

STAMFORD RESEARCH INSTITUTE
3514760 - SORTING ARRAY II

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

STANDARD OIL COMPANY (INDIANA)
4054947 - COMPUTER TO TAPE DECK INTERFACE

STANDARD OIL COMPANY
4005387 - COMPUTER CONTROL SYSTEM

STANFORD RESEARCH INSTITUTE
3505653 - SORTING ARRAY

STROLL, H., AND COMPANY
3820082 - DATA STORAGE MEANS FOR ELECTRICAL CONTROL SYSTEMS PARTICULARLY FOR KNITTING MACHINES

TELECOMMUNICATIONS TECHNOLOGY, INC.
4076970 - SWITCHING SYSTEM HAVING A CENTRAL CONTROLLER FOR ACCESSING INDIVIDUAL TELEPHONE CIRCUITS FOR TESTING

TELE RESOURCES, INC.
3862372 - BRANCH EXCHANGE INCLUDING ELECTRONIC TIMER

TENDY ELECTRONICS CO.
4101967 - SINGLE BIT LOGIC MICROPROCESSOR

TESDATA SYSTEMS CORPORATION
4166290 - COMPUTER MONITORING SYSTEM

TEXAS INSTRUMENTS, INCORPORATED
3430203 - TRAINABLE DECISION SYSTEM UTILIZING METAL-OXIDE- SEMICONDUCTOR FIELD EFFECT TRANSISTORS
3573851 - MEMORY BUFFER FOR VECTOR STREAMING
3573852 - VARIABLE TIME SLOT ASSIGNMENT OF VIRTUAL PROCESSORS
3638197 - ELECTRONIC PRINTING INPUT-OUTPUT STATION
3757306 - COMPUTING SYSTEMS CPU
3757308 - DATA PROCESSOR
3758761 - SELF-INTERCONNECTING/SELF-REPAIRABLE ELECTRONIC SYSTEMS ON A SLICE
3855577 - POWER SAVING CIRCUIT FOR CALCULATOR SYSTEM
3892957 - DIGIT MASK LOGIC COMBINED WITH SEQUENTIALLY ADDRESSED MEMORY IN ELECTRONIC CALCULATOR CHIP
3896418 - SYNCHRONOUS MULTI-PROCESSOR SYSTEM UTILIZING A SINGLE EXTERNAL MEMORY UNIT
3904863 - CALCULATOR SYSTEM USING INSTRUCTION WORDS AS DATA
3909626 - CONTROL OF AXB MATRIX THERMAL PRINTHEAD
3919532 - CALCULATOR SYSTEM HAVING AN EXCHANGE DATA MEMORY REGISTER
3921142 - ELECTRONIC CALCULATOR CHIP HAVING TEST INPUT AND OUTPUT
3922538 - CALCULATOR SYSTEM FEATURING RELATIVE PROGRAM MEMORY
3924110 - CALCULATOR SYSTEM FEATURING A SUBROUTINE REGISTER
3931507 - POWER-UP CLEAR IN AN ELECTRONIC DIGITAL CALCULATOR
3932846 - ELECTRONIC CALCULATOR HAVING INTERNAL MEANS FOR TURNING OFF DISPLAY
3934229 - EXTERNAL REGISTER MEMORY CHIP IN A CALCULATOR SYSTEM
3937940 - DIRECT COMPARE IN AN ELECTRONIC DIGITAL CALCULATOR
3938094 - COMPUTING SYSTEM BUS
3939335 - UNIVERSAL CONDITION LATCH IN AN ELECTRONIC DIGITAL CALCULATOR
3944983 - EXPANDABLE DATA STORAGE FOR A CALCULATOR SYSTEM
3944985 - WORKSPACE ADDRESSING SYSTEM
3946216 - ELECTRONIC CALCULATOR SYSTEM HAVING SERIAL TRANSFER OF INSTRUCTION WORD FIELDS TO DECODE ARRAYS
3949367 - DRUM PRINTER CONTROL
3953719 - LATCHED DECODER FOR DIGIT OUTPUTS TO AN ELECTRONIC DIGITAL CALCULATOR DISPLAY
3953834 - PROGRAMMABLE LOGIC CONTROLLER WITH PUSH DOWN STACK
3958223 - EXPANDABLE DATA STORAGE IN A CALCULATOR SYSTEM
3962571 - LOW POWER DIGIT BLANKING CIRCUIT
3962684 - COMPUTING SYSTEM INTERFACE USING COMMON PARALLEL BUS AND SEGMENTED ADDRESSING

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

TEXAS INSTRUMENTS, INCORPORATED (CONTINUED)
3967104 - DIRECT AND INDIRECT ADDRESSING IN AN ELECTRONIC DIGITAL CALCULATOR
3968443 - SOLID STATE TELEVISION CHANNEL SELECTION SYSTEM
3970995 - SLAVING CALCULATOR CHIPS
3976975 - PROMPTING CALCULATOR
3984816 - EXPANDABLE FUNCTION ELECTRONIC CALCULATOR
3986016 - SINGLE CHIP MAGNETIC BUBBLE PROCESSOR
3991306 - ELECTRONIC CALCULATOR OR DIGITAL PROCESSOR CHIP WITH SEPARATELY CONTROLLABLE DIGIT AND SEGMENT OUTPUTS
4004280 - CALCULATOR DATA STORAGE SYSTEM
4020465 - THERMAL LINE PRINTER
4021656 - DATA INPUT FOR ELECTRONIC CALCULATOR OR DIGITAL PROCESSOR CHIP
4021781 - VIRTUAL GROUND READ-ONLY-MEMORY FOR ELECTRONIC CALCULATOR OR DIGITAL PROCESSOR
4024386 - ELECTRONIC CALCULATOR OR DIGITAL PROCESSOR CHIP HAVING TEST MODE OF OPERATION
4025904 - PROGRAMMED ALLOCATION OF COMPUTER MEMORY WORKSPACE
4030080 - VARIABLE MODULE MEMORY
4037090 - MULTIPHASE CLOCKING FOR MOS
4038535 - CALCULATOR-PRINT CRADLE SYSTEM
4048624 - CALCULATOR SYSTEM HAVING MULTI-FUNCTION MEMORY INSTRUCTION REGISTER
4064554 - MICROCOMPUTER WITH CODE CONVERSION
4067058 - WORKSPACE ADDRESSING SYSTEM
4073006 - DIGITAL PROCESSOR SYSTEM WITH SIMULTANEOUS BRANCH AND OP CODE FUNCTION
4074351 - VARIABLE FUNCTION PROGRAMMED CALCULATOR
4074355 - DIGITAL MICROPROCESSOR SYSTEM WITH SHARED DECODE
4078251 - ELECTRONIC CALCULATOR OR MICROPROCESSOR WITH MASK LOGIC EFFECTIVE DURING DATA EXCHANGE OPERATION
4079459 - TWO SPEED SHIFT REGISTER FOR ELECTRONIC CALCULATOR OR MICROPROCESSOR SYSTEM
4089062 - SWITCHING CONTROL CIRCUITS FOR ELECTRONIC CALCULATOR WITH PUSH-BUTTON ON-OFF SYSTEM
4092730 - DATA PROCESSOR WITH READ-ONLY-MEMORY PROCESSOR AND PARTIAL SOLUTION PUSH-DOWN STACK
4100606 - KEY DEBOUNCE SYSTEM FOR ELECTRONIC CALCULATOR OR MICROPROCESSOR
4107781 - ELECTRONIC CALCULATOR OR MICROPROCESSOR WITH INDIRECT ADDRESSING
4107782 - PROMPTING PROGRAMMABLE CALCULATOR
4112495 - ELECTRONIC CALCULATOR OR MICROPROCESSOR HAVING A SELECTIVELY LOADABLE INSTRUCTION REGISTER
4139893 - CALCULATOR PROGRAM SECURITY SYSTEM
4145756 - THERMAL LINE PRINTER
4146928 - POWER UP CLEAR SYSTEM FOR AN ELECTRONIC CALCULATOR OR MICROPROCESSOR
4153937 - MICROPROCESSOR SYSTEM HAVING HIGH ORDER CAPABILITY
4156927 - DIGITAL PROCESSOR SYSTEM WITH DIRECT ACCESS MEMORY
4158431 - SELF-TEST FEATURE FOR APPLIANCES OR ELECTRONIC SYSTEMS OPERATED BY MICROPROCESSOR
4158432 - CONTROL OF SELF-TEST FEATURE FOR APPLIANCES OR ELECTRONIC EQUIPMENT OPERATED BY MICROPROCESSOR
4159516 - INPUT/OUTPUT CONTROLLER HAVING SELECTABLE TIMING AND MASKABLE INTERRUPT GENERATION
4164037 - ELECTRONIC CALCULATOR OR MICROPROCESSOR SYSTEM HAVING COMBINED DATA AND FLAG BIT STORAGE SYSTEM
4175286 - BURN-IN TEST SYSTEM FOR ELECTRONIC APPARATUS

TOKYO ELECTRIC CO., LTD.
4095267 - CLOCK PULSE CONTROL SYSTEM FOR MICROCOMPUTER SYSTEMS

TOKYO SHIBAURA ELECTRIC CO., LTD.
4087854 - MINICOMPUTER SYSTEM WITH AN ARITHMETIC CONTROL UNIT INTEGRATED ON A ONE-CHIP SEMICONDUCTOR DEVICE
4093984 - DATA PROCESSING SYSTEM HAVING A CYCLE CONTROL FUNCTION
4093993 - BIT-SLICE TYPE LARGE SCALE INTEGRATED CIRCUIT WITH MULTIPLE FUNCTIONS ON A ONE-CHIP SEMICONDUCTOR DEVICE
4096572 - COMPUTER SYSTEM WITH A MEMORY ACCESS ARBITRATOR
4126896 - MICROPROGRAMMED LARGE-SCALE INTEGRATION (LSI) MICROPROCESSOR
4130866 - DATA PROCESSOR HAVING A CIRCUIT STRUCTURE SUITABLE FOR FABRICATION IN LSI FORM
4130869 - MICROPROGRAM CONTROLLED SYSTEM
4142233 - REFRESHING SYSTEM FOR DYNAMIC MEMORY
4151611 - POWER SUPPLY CONTROL SYSTEM FOR MEMORY SYSTEMS
4164666 - ELECTRONIC APPARATUS USING COMPLEMENTARY MOS TRANSISTOR DYNAMIC CLOCKED LOGIC CIRCUITS

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

TOYODA KOKI KABUSHIKI KAISHA
4019175 - PROGRAM CHANGEABLE SEQUENCE CONTROLLER

TRANSACTRON, INC.
3946220 - POINT-OF-SALE SYSTEM AND APPARATUS

UNION CARBIDE CORPORATION
4091447 - INTERRUPT CONTROL SYSTEM FOR A MICROCOMPUTER

UNITED STATES OF AMERICA, AIR FORCE
4021785 - INTERFACE SYSTEM FOR A COMPUTER TERMINAL AND RANDOM ACCESS SLIDE PROJECTOR
4168532 - MULTIMODE DATA DISTRIBUTION AND CONTROL APPARATUS

UNITED STATES OF AMERICA, NAVY
3641485 - ECHO SIMULATION MEANS
3678468 - DIGITAL DATA STORAGE SYSTEM
3699534 - CELLULAR ARITHMETIC ARRAY
3757312 - GENERAL PURPOSE ASSOCIATIVE PROCESSOR
3824562 - HIGH SPEED RANDOM ACCESS MEMORY SHIFT REGISTER
3935563 - COMPUTER FOOTPRINT FILE
3949378 - COMPUTER MEMORY ADDRESSING EMPLOYING BASE AND INDEX REGISTERS
4016547 - MOS SHIFT REGISTER COMPENSATION SYSTEM FOR DEFECTIVE TRACKS OF DRUM STORAGE SYSTEM
4104719 - MULTI-ACCESS MEMORY MODULE FOR DATA PROCESSING SYSTEMS

UNIVERSITY OF PENNSYLVANIA
3601809 - ADDRESSABLE LIST MEMORY SYSTEMS

UNIVERSITY OF ROCHESTER
3953732 - DYNAMIC MASS SPECTROMETER

U.S. PHILIPS CORPORATION
3747073 - ELECTRICAL DISPLAY DEVICES
3761885 - COMPUTER SYSTEM COMPRISING A STORAGE CONFIGURATION WITH ACCESS PRIOR TO ULTIMATE ADDRESS CALCULATION
3764991 - DEVICE COMPRISING A PLURALITY OF SERIES ARRANGED STORAGE ELEMENTS
3965338 - APPARATUS FOR ACHIEVING A PREDETERMINED TRANSFER CHARACTERISTIC
3984811 - MEMORY SYSTEM WITH BYTEWISE DATA TRANSFER CONTROL
4034345 - MICROPROGRAMMABLE COMPUTER DATA TRANSFER ARCHITECTURE

VICKERS LIMITED
4093999 - ELECTRONIC FRANKING MACHINES

VICTOR COMPTOMETER CORPORATION
3906453 - CARE MEMORY CONTROL CIRCUIT
3906457 - DISPLAY SYSTEM FOR AN ELECTRONIC BUSINESS MACHINE

WALTER BUHMANN ELEKTRO APPARATEBAU GMBH
3864669 - CORRECTION ARRANGEMENT FOR ELECTRONIC TYPEWRITERS

WANG LABORATORIES, INC.
3760171 - PROGRAMMABLE CALCULATORS HAVING DISPLAY MEANS AND MULTIPLE MEMORIES
4145739 - DISTRIBUTED DATA PROCESSING SYSTEM

WARNER + SWASEY COMPANY
3969724 - CENTRAL PROCESSING UNIT FOR USE IN A MICROPROCESSOR

ASSIGNED PATENTING(1/69-12/79) - - ALPHA LISTING

WESTINGHOUSE ELECTRIC CORP.
3978454 - SYSTEM AND METHOD FOR PROGRAMMABLE SEQUENCE CONTROL

XEROX CORPORATION
3810105 - COMPUTER INPUT-OUTPUT SYSTEM
3967251 - USER VARIABLE COMPUTER MEMORY MODULE
4016549 - SCANNING AND SELECTION METHODS AND APPARATUS THEREFOR
4021650 - VELOCITY COMMAND SIGNAL GENERATING APPARATUS
4045779 - SELF-CORRECTING MEMORY CIRCUIT
4058195 - INCREMENT-DECREMENT LOGIC FOR SERIAL PRINTER
4075707 - PROGRAMMED DEVICE CONTROLLER
4084680 - ENHANCED UNDERSCORING METHODS AND MEANS FOR AUTOMATIC TYPEWRITER AND THE LIKE EMPLOYING HAMMER-TYPE IMPACT PRINTING MECH ANISM
4087852 - MICROPROCESSOR FOR AN AUTOMATIC WORD-PROCESSING SYSTEM
4103326 - TIME-SLICING METHOD AND APPARATUS FOR DISK DRIVE
4109310 - VARIABLE FIELD LENGTH ADDRESSING SYSTEM HAVING DATA BYTE INTERCHANGE
4144561 - CHIP TOPOGRAPHY FOR MOS INTEGRATED CIRCUITRY MICROPROCESSOR CHIP
4156291 - CIRCUITRY FOR ELIMINATING DOUBLE RAM ROW ADDRESSING
4170791 - SERIAL DATA COMMUNICATION SYSTEM FOR A REPRODUCTION MACHINE

UNASSIGNED PATENTS(1/75-12/79) INVENTORS(ALPHA LISTING)

INVENTOR NAME			STREET	CITY	ST	ZIP/CNTRY
BEST	ROBERT	M.	16016 9TH AVE. NE.	SEATTLE	WA	98155
4168396 - MICROPROCESSOR FOR EXECUTING ENCIPHERED PROGRAMS						
BOONE	GARY		6319 OAKHAM	HOUSTON	TX	77045
3962683 - CPU PROGRAMMABLE CONTROL SYSTEM						
BRUNSON	RAYMOND	D.	5404 BRIXHAM COURT	BURKE	VA	22015
3987417 - ADDRESS MEMORY SYSTEM						
CATT	IVOR		CROUCH HALL	REDBOURN, HERTFORDSH		EN
3913072 - DIGITAL INTEGRATED CIRCUITS						
CAUDEL	EDWARD	R.	P.O. BOX 394	BELLAIRE	TX	77401
3991305 - ELECTRONIC CALCULATOR OR DIGITAL PROCESSOR CHIP WITH MULTIPLE CODE COMBINATIONS OF DISPLAY AND KEYBOARD SCAN OUTPUTS						
CHESLEY	GILMAN	D.	22431 STARLING DRIVE	LOS ALTOS	CA	94022
4038648 - SELF-CONFIGURABLE CIRCUIT STRUCTURE FOR ACHIEVING WAFER SCALE INTEGRATION						
CHICHERIN	JURY	E.	103460, KORPUS 161, KV. 31	MOSCOW		SU
4124890 - MICROPROCESSOR COMPUTING SYSTEM						
CONE	GAIL	P.	2276 EDSEL DRIVE	MILPITAS	CA	95035
4015243 - MULTI-PROCESSING COMPUTER SYSTEM						
CONSTANT	JAMES	N.	1603 DANBURY DR.	CLAREMONT	CA	90027
4107458 - CIPHER COMPUTER AND CRYPTOGRAPHIC SYSTEM						
DSHKHUNIAN	VALERY	L.	K-482, KORPUS 338-A, KV. 78	MOSCOW		SU
4124890 - MICROPROCESSOR COMPUTING SYSTEM						
FISHER	ROGER	J.	2601 MARILEE	HOUSTON	TX	77002
3987416 - ELECTRONIC CALCULATOR WITH DISPLAY AND KEYBOARD SCANNING SIGNAL GENERATOR IN DATA MEMORY						
GERNELLE	FRANCOIS		18 AVENUE DU BOIS	92290-CHATENAY MALAB		FR
3974480 - DATA PROCESSING SYSTEM, SPECIALLY FOR REAL-TIME APPLICATIONS						
GILBERT	ELI		545 W. END AVE.	NEW YORK	NY	10024
4164024 - INFORMATION RETRIEVAL SYSTEM FOR PROVIDING RETRIEVABLE UPDATEABLE DISPLAY OF A PERMANENT MICROFILM RECORD						
GITTINS	MARVIN	W.	RTE. 1	COUNCIL BLUFFS	IA	51501
4128226 - EXTENSION LIGHT ASSEMBLY						
HARTSELL	GLENN	A.	7215 ROUNDROCK ROAD	DALLAS	TX	75240
3987416 - ELECTRONIC CALCULATOR WITH DISPLAY AND KEYBOARD SCANNING SIGNAL GENERATOR IN DATA MEMORY						
HARVEY	NORMAN	L.	127 BEVERLY DR., SE	WINTER HAVEN	FL	33880
4142232 - STUDENT+3 S COMPUTER						
HOTTO	ROBERT		41 E. 19TH ST.	NEW YORK	NY	10003
4117542 - ELECTRONIC POCKET DIRECTORY						
HYATT	GILBERT	P.	P.O. BOX 4584	ANAHEIM	CA	92803
4144582 - VOICE SIGNAL PROCESSING SYSTEM						

UNASSIGNED PATENTS(1/75-12/79) INVENTORS(ALPHA LISTING)

INVENTOR NAME				STREET	CITY	ST	ZIP/CNTRY
HYATT	GILBERT	P.		11101 AMIGO AVE.	NORTHRIDGE	CA	91324
4121284 - COMPUTERIZED SYSTEM FOR OPERATOR INTERACTION							
HYATT	GILBERT	PETER		P.O. BOX 4584	ANAHEIM	CA	92803
4016540 - APPARATUS AND METHOD FOR PROVIDING INTERACTIVE AUDIO COMMUNICATION							
4060848 - ELECTRONIC CALCULATOR SYSTEM HAVING AUDIO MESSAGES FOR OPERATOR INTERACTION							
JUDITSKY	DAVLET	I.		125475, ULITSA ZELENOGRADSKAYA	MOSCOW		SU
4124890 - MICROPROCESSOR COMPUTING SYSTEM							
KLAUSNER	JUDAH			18 E. 64TH ST.	NEW YORK	NY	10021
4117542 - ELECTRONIC POCKET DIRECTORY							
KURPANEK	HORST	G.		802 ALLISON WAY	SUNNYVALE	CA	94087
4015243 - MULTI-PROCESSING COMPUTER SYSTEM							
LAMAR	WILLIAM	PAUL		1024 17TH ST.	HERMOSA BEACH	CA	90254
4056711 - METHOD AND APPARATUS FOR PROGRAMMING MICROPROCESSORS							
LEVINE	MICHAEL	R.		3605 FREDERICK DR.	ANN ARBOR	MI	48105
4117469 - COMPUTER ASSISTED DISPLAY PROCESSOR HAVING MEMORY SHARING BY THE COMPUTER AND THE PROCESSOR							
MANNING	FRANK			APARTMENT 6, 30 LITTELL ROAD	BROOKLINE	MA	02146
4020469 - PROGRAMMABLE ARRAYS							
MASHEVICH	PAVEL	R.		K-482, KORPUS 338-A, KV. 139	MOSCOW		SU
4124890 - MICROPROCESSOR COMPUTING SYSTEM							
MORETON	DEREK	VIDION		15 CHURCH ROAD	ALSAGER, CHESHIRE		EN
4035777 - DATA PROCESSING SYSTEM INCLUDING PARALLEL BUS TRANSFER CONTROL PORT							
NESTEROV	PETR	V.		K-460, KORPUS 3, KV. 30	MOSCOW		SU
4124890 - MICROPROCESSOR COMPUTING SYSTEM							
RAYMOND	JOSEPH	H.	JR.	7618 EICHLER	HOUSTON	TX	77036
3991305 - ELECTRONIC CALCULATOR OR DIGITAL PROCESSOR CHIP WITH MULTIPLE CODE COMBINATIONS OF DISPLAY AND KEYBOARD SCAN OUTPUTS							
RAYMOND	JOSEPH	H.	JR.	7618 EICHLER	HOUSTON, HARRIS COUN	TX	77401
3989939 - ELECTRONIC CALCULATOR OR DIGITAL PROCESSOR CHIP WITH COMBINED FUNCTIONS FOR CONSTANT, KEYBOARD AND CONTROL BIT							
ROSS	MERVIN	L.		502 E. BURLINGTON	FAIRFIELD	IA	52556
4128226 - EXTENSION LIGHT ASSEMBLY							
TELENKOV	VYACHESLAV	V.		K-527, KORPUS 811, KV. 75	MOSCOW		SU
4124890 - MICROPROCESSOR COMPUTING SYSTEM							
TOMAN	DONALD	J.		24 OLD FARM ROAD	PLEASANTVILLE	NY	10570
4027289 - OPERATING CONDITION DATA SYSTEM							
UPTON	HOWARD	T.		2301 GLENALLEN AVE., APT. 810	SILVER SPRING	MD	20906
4153946 - EXPANDABLE SELECTION AND MEMORY NETWORK							

UNASSIGNED PATENTS(1/75-12/79) INVENTORS(ALPHA LISTING)

INVENTOR NAME			STREET	CITY	ST	ZIP/CNTRY
VANDIERENDONCK	JERRY	L.	645 GLENWOOD CUTOFF	SANTA CRUZ	CA	95060
3987416 - ELECTRONIC CALCULATOR WITH DISPLAY AND KEYBOARD SCANNING SIGNAL GENERATOR IN DATA MEMORY						
VASENKOV	ALEXANDR	A.	ZELENOGRAD 103460, KORPUS 3, K	MOSCOW		SU
4124890 - MICROPROCESSOR COMPUTING SYSTEM						
WALKER	RICHARD	L.	P.O. BOX 7344	SAN DIEGO	CA	92107
3918030 - GENERAL PURPOSE DIGITAL COMPUTER						
WINKLER	DEAN	A.	R.R. +190 4, BOX 268	LOOGOOTEE	IN	47553
4168527 - ANALOG AND DIGITAL CIRCUIT TESTER						

PATENTS (1/63-12/79) WITH NEITHER ASSIGNMENT NOR INVENTOR INFORMATION IN DATABASE

3597744 - DIGITAL COMPUTING AND INFORMATION PROCESSING MACHINE AND SYSTEM
3711837 - HEADLINE COUNTING AND PRINTING DESIGN DEVICE
3735361 - INFORMATION STORE SYSTEM HAVING DATA BLOCK SHIFT REGISTERS
4159536 - PORTABLE ELECTRONIC LANGUAGE TRANSLATION DEVICE
4179733 - COMPUTER FOR CONTROL OF COMMUNICATION SIGNALS
3167685 3268871 3292151 3332069 3340513 3350690 3372379 3374465 3389380 3401376 3403383 3416139

CPU'S AND OTHER SYSTEMS

PATENTING UPDATE

ASSIGNEES WITH 2 OR MORE PATENTS (1/80-10/80)

HONEYWELL INFORMATION SYSTEMS INC.	11
INTERNATIONAL BUSINESS MACHINES CORPORATION	11
TEXAS INSTRUMENTS, INCORPORATED	11
MOTOROLA INC.	8
SPERRY CORPORATION	7*
TOKYO SHIBAURA ELECTRIC CO., LTD.	5
XEROX CORPORATION	4
GENERAL ELECTRIC COMPANY	3
HEWLETT-PACKARD COMPANY	3
CII HONEYWELL BULL	3
HONEYWELL INC.	3
SIEMENS AKTIENGESELLSCHAFT	3
ALLEN-BRADLEY COMPANY	2
BELL TELEPHONE LABORATORIES INCORPORATED	2
BURROUGHS CORPORATION	2
DATA GENERAL CORPORATION	2
EATON CORPORATION	2
GIDDINGS & LEWIS, INC.	2
GULF & WESTERN INDUSTRIES, INC.	2
HARRIS CORPORATION	2
HITACHI, LTD.	2
NCR CORPORATION	2
PHILLIPS PETROLEUM COMPANY	2

*COMPOSITE TOTAL, SEE APPENDIX A

United States Patent [19]

Joyce et al.

[11] **4,190,885**

[45] **Feb. 26, 1980**

[54] **OUT OF STORE INDICATOR FOR A CACHE STORE IN TEST MODE**

[75] Inventors: **Thomas F. Joyce**, Burlington; **William Panepinto, Jr.**, Tewksbury, both of Mass.

[73] Assignee: **Honeywell Information Systems Inc.**, Waltham, Mass.

[21] Appl. No.: **863,096**

[22] Filed: **Dec. 22, 1977**

[51] **Int. Cl.**[2] **G06F 11/00; G06F 13/00**

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** ..... 364/200 MS File

[56] **References Cited**

U.S. PATENT DOCUMENTS

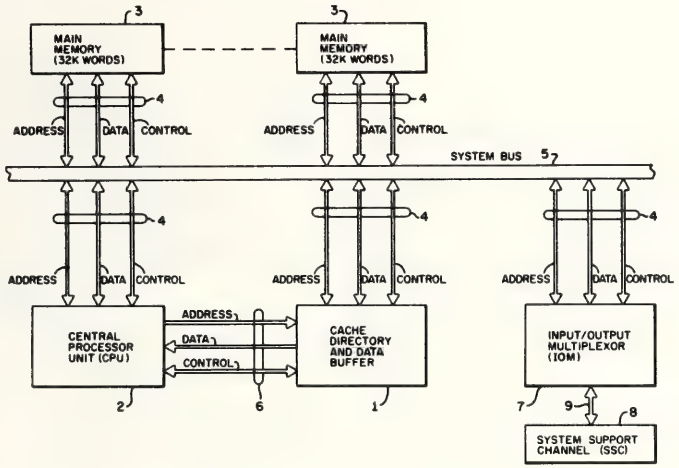
3,611,315	10/1971	Murano et al.	364/200
3,840,862	10/1974	Ready	364/200
3,896,419	7/1975	Lange et al.	364/200
4,042,912	8/1977	Bachman et al.	364/200

Primary Examiner—Harvey E. Springborn
Attorney, Agent, or Firm—George Grayson; Nicholas Prasinos; Ronald T. Reiling

[57] **ABSTRACT**

A Data Processing System comprises a central processor unit, a main memory and a cache, all coupled in common to a system bus. The central processor unit is also separately coupled to the cache. Apparatus in cache is responsive to signals received from the central processor unit to initiate a test and verification mode of operation in cache. This mode enables the cache to exercise various logic areas of cache and to indicate to the central processor unit hardware faults.

9 Claims, 29 Drawing Figures



United States Patent [19]

Joyce

[11] **4,195,343**

[45] **Mar. 25, 1980**

[54] **ROUND ROBIN REPLACEMENT FOR A CACHE STORE**

[75] Inventor: **Thomas F. Joyce**, Burlington, Mass.

[73] Assignee: **Honeywell Information Systems Inc.**, Waltham, Mass.

[21] Appl. No.: **863,102**

[22] Filed: **Dec. 22, 1977**

[51] **Int. Cl.**[2] **G06F 13/00; G11C 9/06**

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** ... 364/200 MS File, 900 MS File

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,820,078	6/1974	Curley et al.	364/200
3,840,862	10/1974	Ready	364/200
3,896,419	7/1975	Lange et al.	364/200

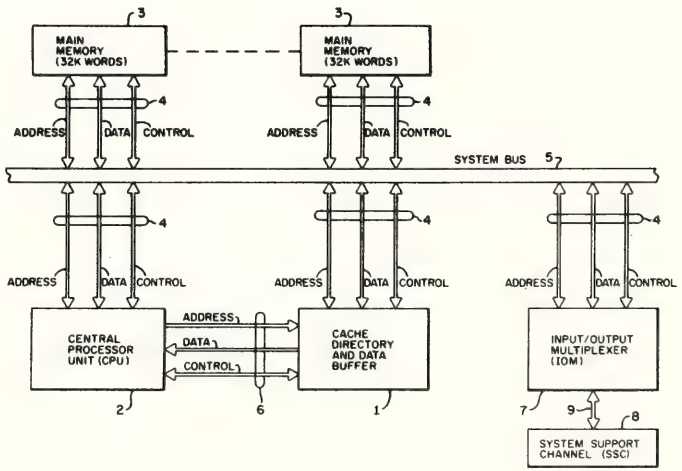
Primary Examiner—Melvin B. Chapnick

Attorney, Agent, or Firm—George Grayson; Nicholas Prasinos; Ronald T. Reiling

[57] **ABSTRACT**

During system initialization, a cache is completely loaded with valid information from main memory. The directory and data buffer are organized in levels of memory locations. Each level of the directory and data buffer is loaded in turn from main memory. Round Robin apparatus, which is preset during system initialization, identifies the next level into which a replacement data word is written on a first in-first out basis. The round robin count for each address location of cache indentifying the next level to be written is stored in a random access memory (RAM). The contents of a particular address location of RAM is incremented each time replacement information is written into that address location in cache.

10 Claims, 24 Drawing Figures



United States Patent [19]

Getson, Jr. et al.

[11] **4,204,250**

[45] **May 20, 1980**

[54] **RANGE COUNT AND MAIN MEMORY ADDRESS ACCOUNTING SYSTEM**

[75] Inventors: **Edward F. Getson, Jr.**, Lynn, Mass.; **John H. Kelley**, Nashua; **Albert T. McLaughlin**, both of Hudson, N.J.; **Donald J. Rathbun**, Andover, Mass.

[73] Assignee: **Honeywell Information Systems Inc.**, Waltham, Mass.

[21] Appl. No.: **821,900**

[22] Filed: **Aug. 4, 1977**

[51] **Int. Cl.**[2] **G06F 13/00**

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** ... 364/200 MS File, 900 MS File

[56] **References Cited**

U.S. PATENT DOCUMENTS

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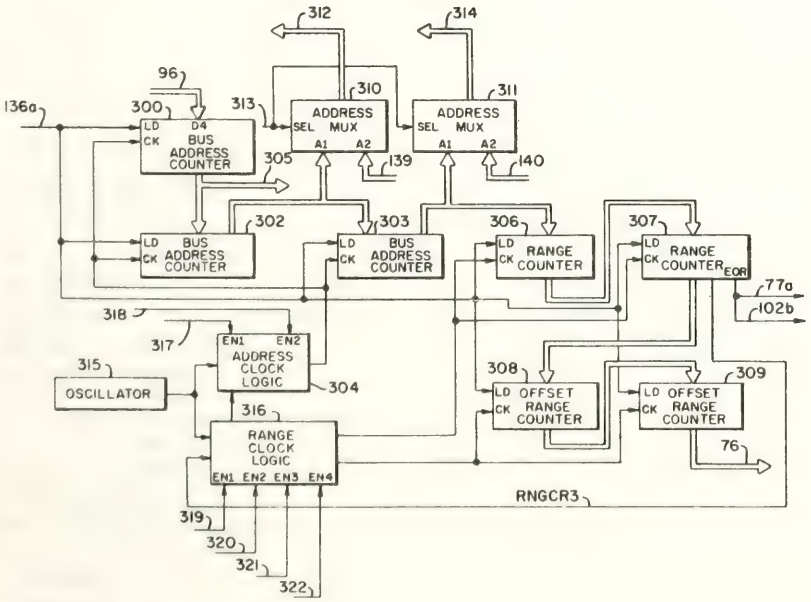
3,950,735	4/1976	Patel	364/200
3,993,981	11/1976	Cassarino, Jr. et al.	364/200
3,997,878	12/1976	Hirvela et al.	364/900

Primary Examiner—Joseph M. Thesz
Attorney, Agent, or Firm—Ronald T. Reiling; Nicholas Prasinos; Gerald E. Lester

[57] **ABSTRACT**

In a peripheral controller of a data processing system having a plurality of system units electrically coupled to a common communication bus for asynchronous intercommunication, an array of counters responsive to both hardware and firmware are connected in a manner to form a serial control data path. Prior to a data transfer, a serial data stream including an offset range count, a range count and a main memory address is shifted through the counters under firmware control. During a data transfer, the firmware enables the hardware control to increment the memory address and decrement the range count to accommodate the higher data transfer rates characteristic of hardware control.

4 Claims, 13 Drawing Figures



United States Patent [19]

Woods et al.

[11] **4,206,503**

[45] **Jun. 3, 1980**

[54] **MULTIPLE LENGTH ADDRESS FORMATION IN A MICROPROGRAMMED DATA PROCESSING SYSTEM**

[75] Inventors: **William E. Woods**, Natick; **Philip E. Stanley**, Westboro; **Richard A. Lemay**, Bolton, all of Mass.

[73] Assignee: **Honeywell Information Systems Inc.**, Waltham, Mass.

[21] Appl. No.: **868,251**

[22] Filed: **Jan. 10, 1978**

[51] **Int. Cl.**[2] **G06F 9/20**

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** ... 364/200 MS File, 900 MS File

[56] **References Cited**

U.S. PATENT DOCUMENTS

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3,344,404	9/1967	Curewitz	364/200
3,522,589	8/1970	Thron	364/200
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4,047,247	9/1977	Stanley et al.	

OTHER PUBLICATIONS

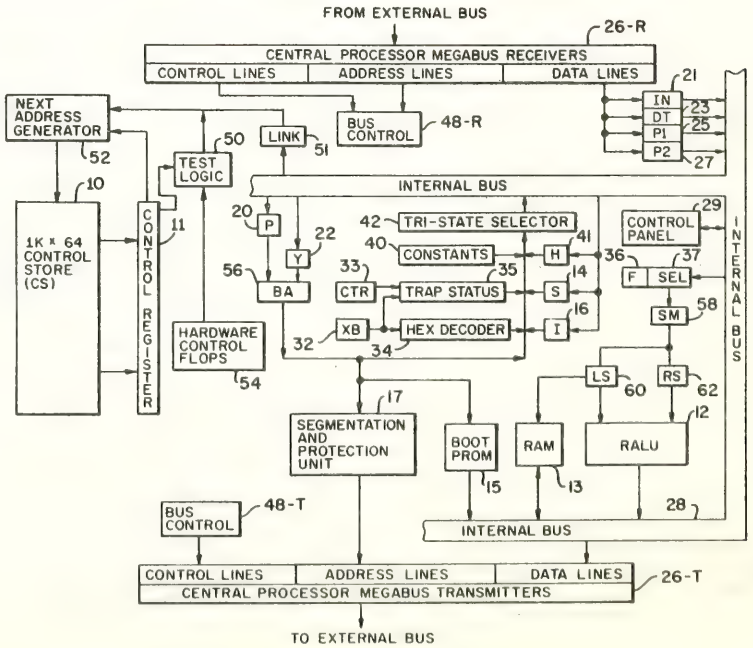
Brown, W. W. et al., "Instructions for Byte Addressing Capability", IBM TDB, vol. 16, No. 3, Aug. 1973, pp. 812–815.

Primary Examiner—Mark E. Nusbaum
Assistant Examiner—Thomas M. Heckler
Attorney, Agent, or Firm—William A. Linnell; Nicholas Prasinos; Ronald T. Reiling

[57] **ABSTRACT**

A final effective address of an operand is generated in a microprogrammed data processing system by use of a base address register which may include an unindexed address, an index register which may include an indexed address value, an instruction register which may include an instruction word, which instruction word provides control over the addressing of a control store dependent upon the state of a selected one of a plurality of test conditions. One of the test conditions indicating whether some of the addressing values used in the generation of the effective address are in a short address format or in a long address format. The address control store word provides signals for controlling the operation of the system, including the branch in between such major operations as instruction fetching, addressing, reading, writing, and execution as well as branching between minor operations which are included in the major operations.

4 Claims, 20 Drawing Figures



United States Patent [19]

Porter et al.

[11] **4,208,716**

[45] **Jun. 17, 1980**

[54] **CACHE ARRANGEMENT FOR PERFORMING SIMULTANEOUS READ/WRITE OPERATIONS**

[75] Inventors: **Marion G. Porter; William A. Shelly,** both of Phoenix; **Robert W. Norman, Jr.,** Glendale, all of Ariz.

[73] Assignee: **Honeywell Information Systems Inc.,** Waltham, Mass.

[21] Appl. No.: **968,521**

[22] Filed: **Dec. 11, 1978**

[51] **Int. Cl.**[2] **G06F 13/00**

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** ... 364/200 MS File, 900 MS File

[56] **References Cited**

U.S. PATENT DOCUMENTS

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3,974,479	8/1976	Kotok et al.	364/200
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4,070,706	1/1978	Schueneman	364/200
4,075,686	2/1978	Calle et al.	364/200
4,156,906	5/1979	Ryan	364/200

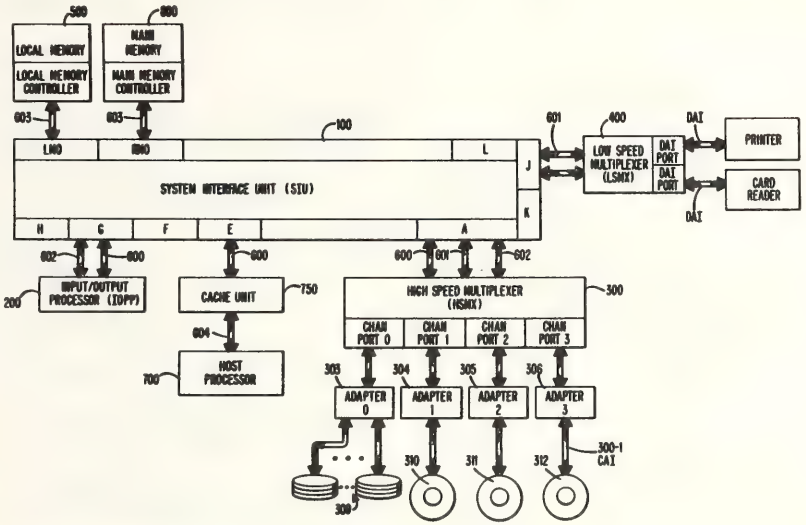
Primary Examiner—Harvey E. Springborn

Attorney, Agent, or Firm—Faith F. Driscoll; Nicholas Prasinos; Ronald T. Reiling

[57] **ABSTRACT**

A cache system includes a storage unit organized into a plurality of levels, each including a number of multi-word blocks and a corresponding number of address selection switches and address registers. Each address selection switch has a plurality of different positions connected to receive address signals from a plurality of address sources. A decoder circuit generates output signals for controlling the operation of the address selection switches. In response to previously defined level signals, the decoder circuit conditions a specified one of the number of switches to switch from a first position to a second position. An address specifying the location into which memory data is to be written is clocked into one address register while the address specifying the location from which an instruction is to be fetched is clocked into the remaining address registers. A comparator circuit compares signals indicating the level into which memory data is to be written with signals indicating the level from which a next instruction is to be fetched. The comparator circuit generates signals which cause the delay of instruction access when there is a conflict between writing memory data and accessing instructions.

39 Claims, 8 Drawing Figures



United States Patent [19]

Rathbun

[11] **4,212,038**

[45] **Jul. 8, 1980**

[54] **DOUBLE DENSITY READ RECOVERY**

[75] Inventor: **Donald J. Rathbun,** Andover, Mass.

[73] Assignee: **Honeywell Information Systems Inc.,** Waltham, Mass.

[21] Appl. No.: **866,441**

[22] Filed: **Jan. 3, 1978**

[51] **Int. Cl.**[2] **H03K 13/24;** G11B 5/09

[52] **U.S. Cl.** ..... **360/41;** 364/900; 340/347 DD

[58] **Field of Search** ... 364/200 MS File, 900 MS File; 360/41, 43, 44, 48; 340/347 DD

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,905,029	9/1975	McIntosh	360/41
3,976,996	7/1976	Wu	360/41
4,034,348	7/1977	Rathburn	364/900

Primary Examiner—Gareth D. Shaw

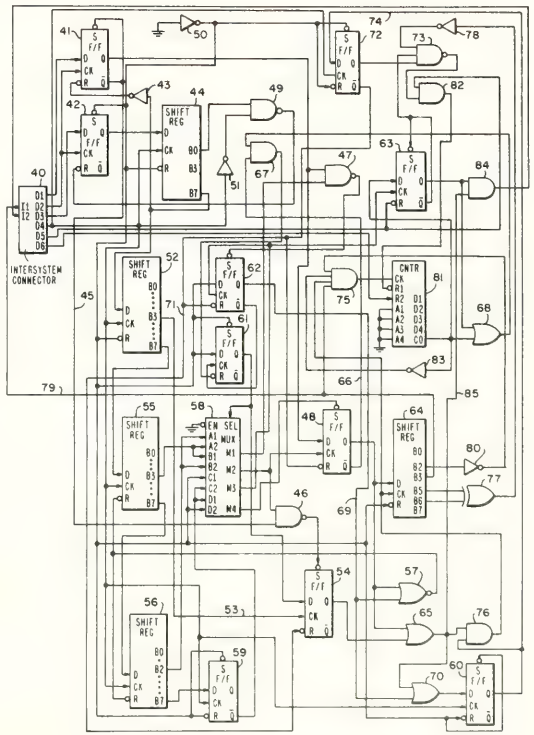
Assistant Examiner—C. T. Bartz

Attorney, Agent, or Firm—Ronald T. Reiling; Nicholas Prasinos; Gerald E. Lester

[57] **ABSTRACT**

A logic system requiring no tuning adjustments is provided for converting an MFM encoded information stream read from a mass storage medium to a non-return-to-zero (NRZ) information stream. The MFM encoded information stream is routed through an input shift register to provide plural information bit cells in parallel. Outputs of the shift register are sampled with a multiplexer to generate timing strobes for detecting an address mark, and for identifying clock bits, data bits and logic zero data appearing in the MFM encoded data field following the address mark. Clock bits are separated from the data, and both data bits and logic zero data are applied serially to an output shift register to form a serial NRZ data stream. Each time a data bit or logic zero data is loaded into the output shift register, a synchronization strobe is generated to transfer the NRZ data to succeeding systems.

3 Claims, 19 Drawing Figures



United States Patent [19]

Joyce et al.

[11] **4,214,303**

[45] **Jul. 22, 1980**

[54] **WORD ORIENTED HIGH SPEED BUFFER MEMORY SYSTEM CONNECTED TO A SYSTEM BUS**

[75] Inventors: **Thomas F. Joyce**, Burlington; **Thomas O. Holtey**, Newton Lower Falls; **William Panepinto, Jr.**, Tewksbury, all of Mass.

[73] Assignee: **Honeywell Information Systems Inc.**, Waltham, Mass.

[21] Appl. No.: **863,093**

[22] Filed: **Dec. 22, 1977**

[51] **Int. Cl.**[2] **G06F 13/00**

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** ... 364/200 MS File, 900 MS File

[56] **References Cited**

U.S. PATENT DOCUMENTS

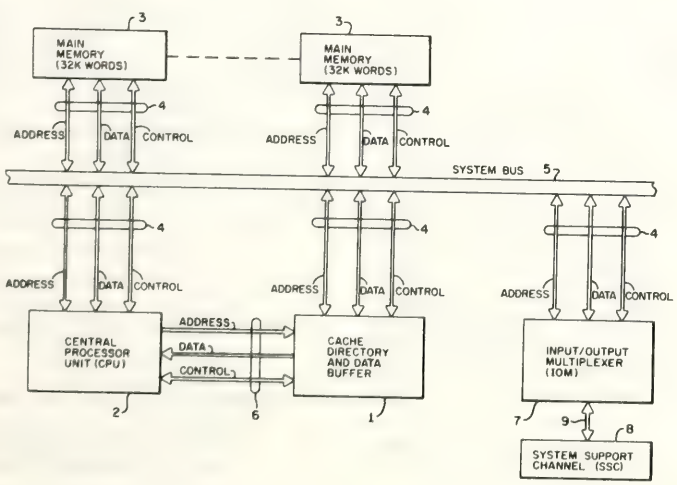
3,820,078	6/1974	Curley et al.	364/200
3,840,862	10/1974	Ready	364/200
3,840,863	10/1974	Fuqua et al.	364/200
3,866,183	2/1975	Lange	364/200
4,068,299	1/1978	Bachman	364/200

Primary Examiner—Melvin B. Chapnick
Attorney, Agent, or Firm—George Grayson; Nicholas Prasinos; Ronald T. Reiling

[57] **ABSTRACT**

A word oriented data processing system includes a plurality of system units all connected in common to a system bus. Included are a central processor unit (CPU), a memory system and a high speed buffer or cache system. The cache system is also coupled to the CPU. The cache includes an address directory and a data store with each address location of directory addressing its respective word in data store. The CPU requests a word of cache by sending a memory request to cache which includes a memory address location. If the requested word is stored in the data store, then it is sent to the CPU. If the word is not stored in cache, the cache requests the word of memory. When the cache receives the word from memory, the word is sent to the CPU and also stored in the data store.

11 Claims, 28 Drawing Figures



United States Patent [19]

Negi et al.

[11] **4,218,739**

[45] **Aug. 19, 1980**

[54] **DATA PROCESSING INTERRUPT APPARATUS HAVING SELECTIVE SUPPRESSION CONTROL**

[75] Inventors: **Virendra S. Negi**, Pepperell; **Ming T. Miu**, Chelmsford, both of Mass.

[73] Assignee: **Honeywell Information Systems Inc.**, Waltham, Mass.

[21] Appl. No.: **736,657**

[22] Filed: **Oct. 28, 1976**

[51] **Int. Cl.**[2] **G06F 9/18**

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** ..... 340/172.5; 445/1; 364/200 MS File, 900 MS File

[56] **References Cited**

U.S. PATENT DOCUMENTS

Re. 28,221	11/1974	Benghiat	340/172.5
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3,560,935	2/1971	Beers	340/172.5
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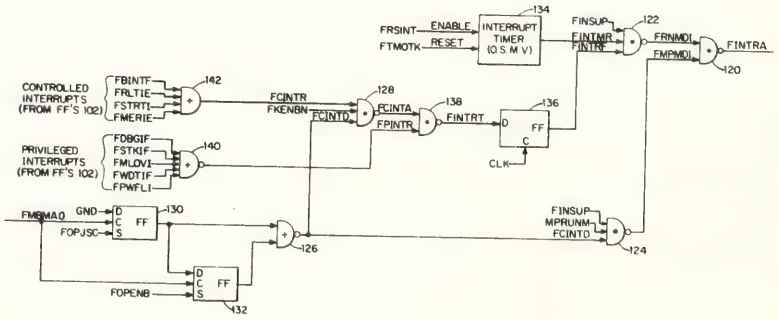
3,828,327	8/1974	Berglund et al.	340/172.5
3,866,181	2/1975	Gayman et al.	340/172.5
4,000,485	12/1976	Barlow et al.	340/172.5
4,001,784	1/1977	Bardotti	340/172.5

Primary Examiner—Melvin B. Chapnick
Attorney, Agent, or Firm—Finnegan, Henderson, Farabow, Garrett & Dunner

[57] **ABSTRACT**

Interrupts generated within a data processor (internal interrupts) and an interrupt received from a peripheral device (external interrupts) coupled with the processor are prioritized and, unless suppressed, are coupled to generate an interrupt signal for use in addressing a routine for servicing the particular highest priority requesting internal or external interrupt. All further interrupts are suppressed during the time required to service the interrupt and, depending upon the type of interrupt, either the internal or external interrupt may be suppressed for one or two instruction times for debug purposes or under computer program control as required for a particular operation.

12 Claims, 4 Drawing Figures



United States Patent [19]

Trinchieri

[11] **4,224,664**

[45] **Sep. 23, 1980**

[54] **APPARATUS FOR DETECTING WHEN THE ACTIVITY OF ONE PROCESS IN RELATION TO A COMMON PIECE OF INFORMATION INTERFERES WITH ANY OTHER PROCESS IN A MULTIPROGRAMMING/MULTIPROCESSING COMPUTER SYSTEM**

[75] Inventor: **Mario G. Trinchieri**, Weston, Mass.

[73] Assignee: **Honeywell Information Systems Inc.**, Waltham, Mass.

[21] Appl. No.: **684,345**

[22] Filed: **May 7, 1976**

[51] **Int. Cl.**[3] **G06F 9/46**

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** ..... 340/172.5; 445/1; 444/1; 364/200 MS File, 900 MS File, 300

[56] **References Cited**

U.S. PATENT DOCUMENTS

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3,530,438	9/1970	Mellen et al.	340/172.5
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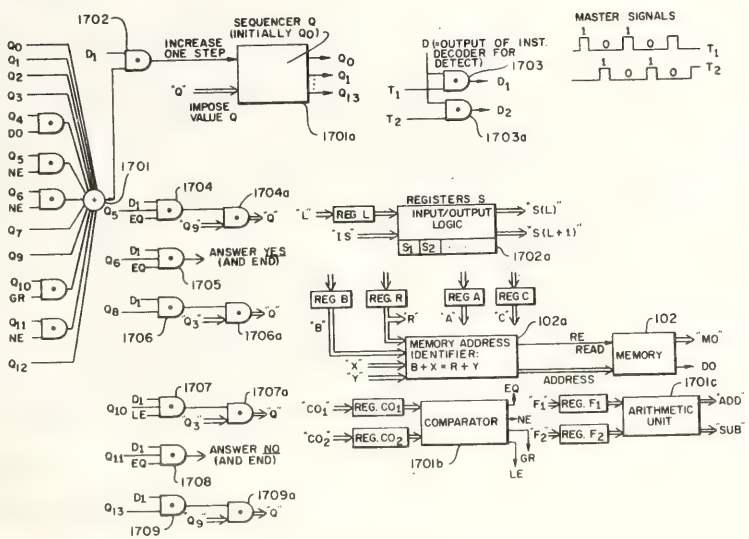
Primary Examiner—Melvin B. Chapnick
Attorney, Agent, or Firm—George Grayson; Nicholas Prasinos; Ronald T. Reiling

[57] **ABSTRACT**

A multiprogramming/multiprocessing computer system for executing a plurality of processes sharing common information in the form of records, pages or messages, employing an apparatus for avoiding an interference between two processes seeking access to elements of common information. The system operates to store in a first memory utilization data in table form identifying the processes which have accessed each individual element of common information. A second memory stores a matrix of precedence data representing the relative order in which processes must access the common information in accordance with a predetermined set of access rules. When a first process enters a request to access an element of common information, the system identifies from the utilization table any other process which, according to the access rules, must be given precedence to the common information over the first process. Thereafter, the system inspects the second memory and determines from the precedence data therein whether any inverse precedence relationships have been detected and, if so, rejects the access request entered by the first process and moves on to process the next access request.

10 Claims, 36 Drawing Figures



United States Patent [19]

Kobs et al.

[11] **4,225,942**

[45] **Sep. 30, 1980**

[54] **DAISY CHAINING OF DEVICE INTERRUPTS IN A CATHODE RAY TUBE DEVICE**

[75] Inventors: **Frederick E. Kobs**, Pepperell, Mass.; **Joseph L. Ryan**, Nashua, N.H.; **Minoru Inoshita**, Glendale, Ariz.; **Gerald N. Winfrey**, Billerica, Mass.

[73] Assignee: **Honeywell Information Systems Inc.**, Waltham, Mass.

[21] Appl. No.: **973,364**

[22] Filed: **Dec. 26, 1978**

[51] **Int. Cl.**[3] **G06F 9/46**

[52] **U.S. Cl.** **364/900**

[58] **Field of Search** ... 364/200 MS File, 900 MS File

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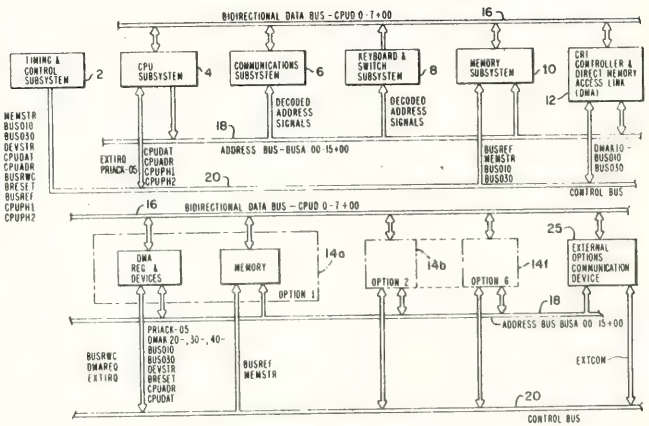
4,106,104	8/1978	Nitta et al.	364/900

Primary Examiner—Leo H. Boudreau
Attorney, Agent, or Firm—George Grayson; Nicholas Prasinos; Ronald T. Reiling

[57] **ABSTRACT**

A microprocessor controlled cathode ray tube display system has a plurality of peripheral devices all connected in common to a system bus. Apparatus in each peripheral device activates a single interrupt signal. A single acknowledge response signal to all the devices enables the interrupting device to place its address signals on the system bus thereby initiating a firmware routine for making the interrupting device operative with the system.

7 Claims, 15 Drawing Figures



United States Patent [19]

Tarbox et al.

[11] **4,231,086**

[45] **Oct. 28, 1980**

[54] **MULTIPLE CPU CONTROL SYSTEM**

[75] Inventors: **Bruce H. Tarbox**, Billerica, Mass.; **Kenneth E. Bruce**, Nashua, N.H.; **John W. Conway**, Waltham; **Ralph M. Lombardo, Jr.**, Lowell, both of Mass.

[73] Assignee: **Honeywell Information Systems, Inc.**, Waltham, Mass.

[21] Appl. No.: **956,382**

[22] Filed: **Oct. 31, 1978**

[51] **Int. Cl.**[3] **G06F 9/46**; G06F 3/04

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** 364/200, 900

[56] **References Cited**

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4,106,104	8/1978	Nitta et al.	364/900

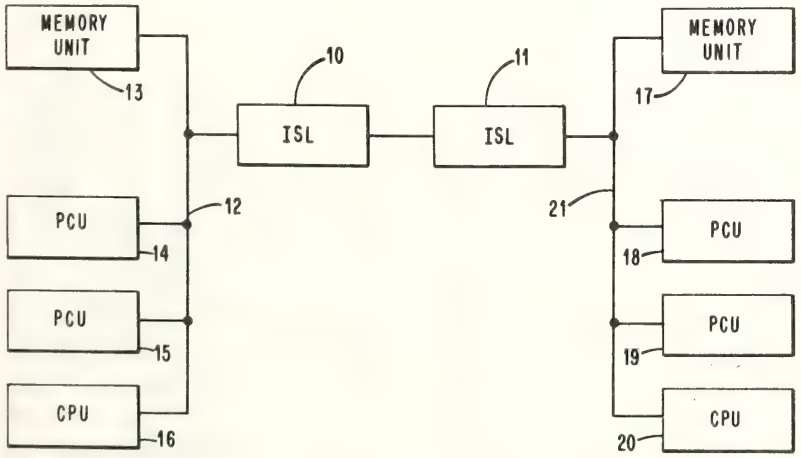
Primary Examiner—Jerry Smith
Attorney, Agent, or Firm—Gerald E. Lester; Nicholas Prasinos; Ronald T. Reiling

[57] **ABSTRACT**

A logic system in an intersystem link (ISL) unit is provided for avoiding deadlock conditions which may occur in a data processing system wherein multiple CPUs on one communication bus attempt to communicate with resources on remote communication busses.

The data processing system has plural communication busses, each providing a common information path to plural data processing units including memory units, peripheral control units, central processing units (CPUs) and ISL units, and each of the plural communication busses are in electrical communication with an ISL unit, and ISL units are electrically connected in pairs.

1 Claim, 42 Drawing Figures



United States Patent [19]

Marenin

[11] **4,181,934**

[45] **Jan. 1, 1980**

[54] **MICROPROCESSOR ARCHITECTURE WITH INTEGRATED INTERRUPTS AND CYCLE STEALS PRIORITIZED CHANNEL**

[75] Inventor: **George B. Marenin**, San Jose, Calif.

[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[21] Appl. No.: **754,193**

[22] Filed: **Dec. 27, 1976**

[51] **Int. Cl.**[2] **G06F 3/04**; G06F 13/00

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** ... 364/200 MS File, 900 MS File

[56] **References Cited**

U.S. PATENT DOCUMENTS

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IBM TDB, Shared Interrupt/Cycle Steal Priority, vol. 18, No. 3, Aug. 1975, pp. 901-904, Booner et al.

Primary Examiner—Gareth D. Shaw
Assistant Examiner—Thomas M. Heckler
Attorney, Agent, or Firm—Shelley M. Beckstrand

[57] **ABSTRACT**

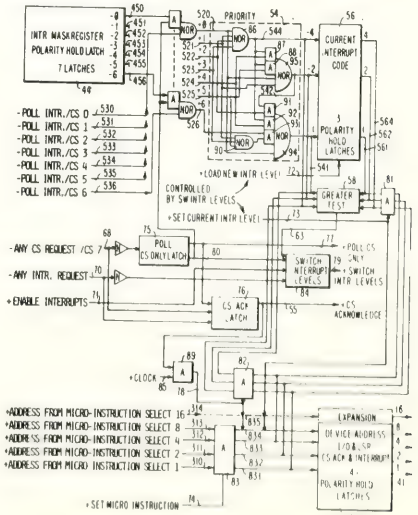
A computing system architecture includes a central processing unit having a channel, arithmetic and logic unit, a plurality of working registers, and control logic; a plurality of local storage registers; a main storage; an executable control store; one or more input/output devices; and a multiplexed cycle steal and interrupt request common poll bus.

The storage and input/output devices communicate with and are controlled by the central processing unit over a looped, or unidirectional bus and control channel including a bus in, a bus out, an address and control bus, and a plurality of control lines. Bus out is operated to address the executable control store and main storage, and to provide data to the input/output devices and the local storage registers. Bus in is shared by the input/output devices and all storage devices and registers for transferring data and control information to the central processing unit. Bus in is also used by main storage to receive data from the input/output devices and from the local storage registers. The address and control bus addresses the input/output devices and the local storage registers, thus enabling overlapping of device or local storage data transfers with the accessing of executable control storage and main storage, and with instruction execution.

The arithmetic and logic unit is time shared for data and input/output processing, register/register and storage/-register transfers, shift operations, byte manipulations, and address modification.

Both cycle steal and interrupt requests are received by the central processor on the common poll bus.

16 Claims, 16 Drawing Figures



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United States Patent [19]

Forster et al.

[11] **4,181,942**

[45] **Jan. 1, 1980**

[54] **PROGRAM BRANCHING METHOD AND APPARATUS**

[75] Inventors: **Richard G. Forster; John K. Howard,** both of San Jose, Calif.

[73] Assignee: **International Business Machines Corporation,** Armonk, N.Y.

[21] Appl. No.: **892,243**

[22] Filed: **Mar. 31, 1978**

[51] **Int. Cl.**[2] **G06F 9/12**

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** ... 364/200 MS File, 900 MS File

[56] **References Cited**

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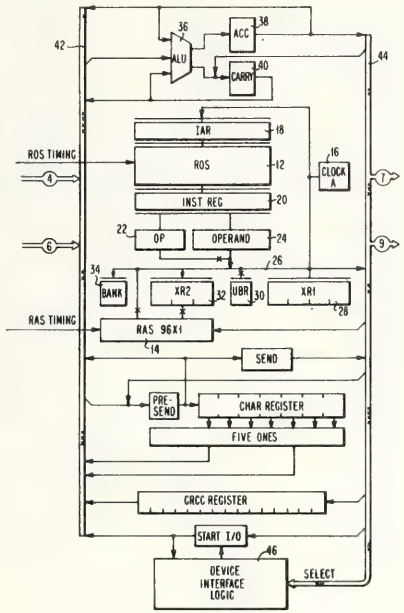
Primary Examiner—James D. Thomas
Attorney, Agent, or Firm—Otto Schmid, Jr.

[57] **ABSTRACT**

A special branch instruction used in a computing system serves as a conditional branch or as an unconditional branch as determined by the state of an internal register. This special branch instruction is used for conditional branching within or at the end of a program loop and for unconditional branching outside of such a loop.

7 Claims, 10 Drawing Figures



United States Patent [19]

Nagel et al.

[11] **4,188,665**

[45] **Feb. 12, 1980**

[54] **PROGRAMMABLE COMMUNICATIONS SUBSYSTEM**

[75] Inventors: **Dennis M. Nagel; Douglas O'Neal; Paul W. Petroskey; Jan W. van den Berg,** all of Boca Raton; **Donald V. Wildes,** North Lauderdale; **David C. Wu,** Delray Beach, all of Fla.

[73] Assignee: **International Business Machines Corporation,** Armonk, N.Y.

[21] Appl. No.: **855,572**

[22] Filed: **Nov. 29, 1977**

[51] **Int. Cl.**[2] **G06F 3/04**

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** ... 364/200 MS File, 900 MS File; 179/15 AL, 15 BV, 15 A

[56] **References Cited**

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Primary Examiner—Gareth D. Shaw
Assistant Examiner—Thomas M. Heckler
Attorney, Agent, or Firm—Richard E. Bee

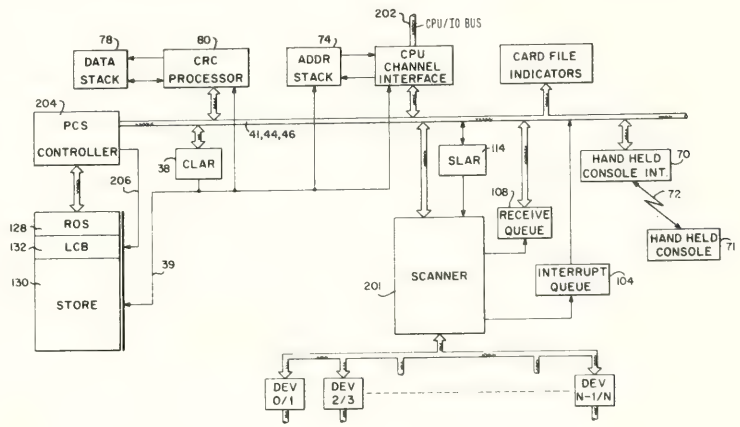
[57] **ABSTRACT**

A micro processor controlled user programmable communications multiplexer subsystem (herein referred to by the symbol PCS) capable of transmitting and receiving data on any one or more of 32 communications lines simultaneously. Each line may be dynamically assigned to a variety of communication characteristics, such as line speeds, character lengths, synchronous, or asynchronous operation, and code structures as well as protocol selections.

The system of the invention provides the capability for the user to write his communications programs using novel operations commands that provide code structure and protocol independence as well as communication line independence. Various hardware features and queuing techniques are employed in order to maintain high transmission rates.

Variable line scanning in the Teleprocessing Time Division Multiplexer of the PCS is programmably permissible; i.e., the time base for line scanning is fixed and is a multiple of the communication line rate, although the actual line to be scanned is programmably variable. The program ability is provided by a continuously scanned storage array which contains physical line addresses of the time division multiplexer. The scanning mechanism, while running, prioritizes the transmit buffer servicing of the individual lines.

3 Claims, 36 Drawing Figures



United States Patent [19]

Staiger

[11] **4,203,543**

[45] **May 20, 1980**

[54] **PATTERN GENERATION SYSTEM**

[75] Inventor: **Dieter Staiger**, Weil im Schonbuch, Fed. Rep. of Germany

[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[21] Appl. No.: **930,947**

[22] Filed: **Aug. 4, 1978**

[30] **Foreign Application Priority Data**

Oct. 18, 1977 [DE] Fed. Rep. of Germany 2746743

[51] **Int. Cl.**[2] **G06F 1/04**; G06F 11/00

[52] **U.S. Cl.** **371/24**; 364/200

[58] **Field of Search** 235/302; 364/200, 900; 307/106; 328/58

[56] **References Cited**

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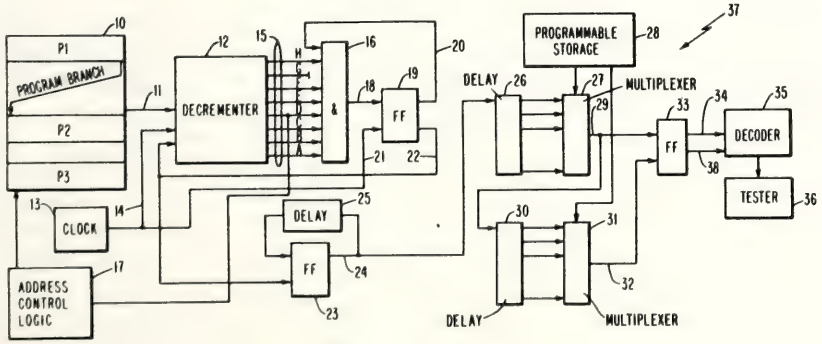
Primary Examiner—Jerry Smith
Attorney, Agent, or Firm—Francis J. Thornton

[57] **ABSTRACT**

This discloses a pattern generator having a programmable product cycle timer in which a pulse train, i.e., the pattern generated can be repeated or switched from a first pulse frequency to a second pulse frequency without the usual transient switching periods between pulses. The invention accomplishes this by providing the generator with a cycle timer using a clock operating in conjunction with a down counter so that at a preselected time interval, before the end of the pulse is achieved, a test is made to determine if a required condition needing a different pulse frequency exists. If such a condition does not exist the present pulse frequency is reinitiated so that at count 0 it is repeated without delay. If the required condition does exist loading of the needed pulse frequency is initiated so that upon termination of the presently existing pulse at count 0, the newly selected pulse will be introduced into the product being tested without delay.

9 Claims, 3 Drawing Figures



United States Patent [19]

Finlay et al.

[11] **4,213,190**

[45] **Jul. 15, 1980**

[54] **PROGRAMMED COPIER CONTROL**

[75] Inventors: **David E. Finlay**, Boulder; **Wayne E. Robbins**, Longmont; **Terence Travis**, Boulder, all of Colo.

[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[21] Appl. No.: **937,396**

[22] Filed: **Aug. 28, 1978**

[51] **Int. Cl.**[2] **G03G 15/00**

[52] **U.S. Cl.** **364/900**

[58] **Field of Search** ... 364/200 MS File, 900 MS File; 355/14

[56] **References Cited**

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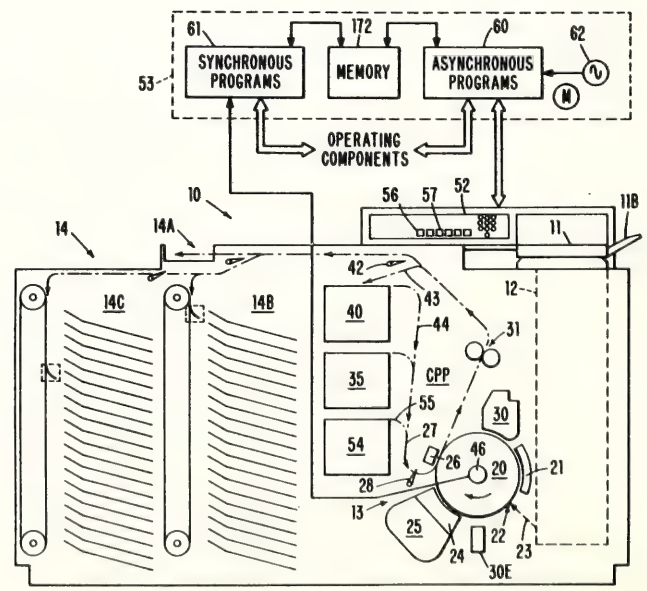
Primary Examiner—Raulfe B. Zache
Attorney, Agent, or Firm—Carl M. Wright

[57] **ABSTRACT**

A copy production machine controlled by a programmed computer in which the computer control programs include synchronous and asynchronous portions. The asynchronous portions are repetitively executed in loop form for checking operating components and servicing operator control panels. The synchronous portions are executed in timed relation to the operation of the machine. The execution of the programs is coordinated via a set of memory registers accessible by the computer during execution of both program portions.

9 Claims, 16 Drawing Figures



United States Patent [19]

McCray et al.

[11] **4,215,422**

[45] **Jul. 29, 1980**

[54] **SELECTIVELY MODIFIABLE PHRASE STORAGE FOR A TYPEWRITER**

[75] Inventors: **William R. McCray; Edward V. Rutkowski, Jr.,** both of Lexington, Ky.

[73] Assignee: **International Business Machines Corporation,** Armonk, N.Y.

[21] Appl. No.: **908,596**

[22] Filed: **May 22, 1978**

[51] **Int. Cl.**[2] **G06F 3/10; G06F 7/02**

[52] **U.S. Cl.** **364/900**

[58] **Field of Search** ... 364/200 MS File, 900 MS File

[56] **References Cited**

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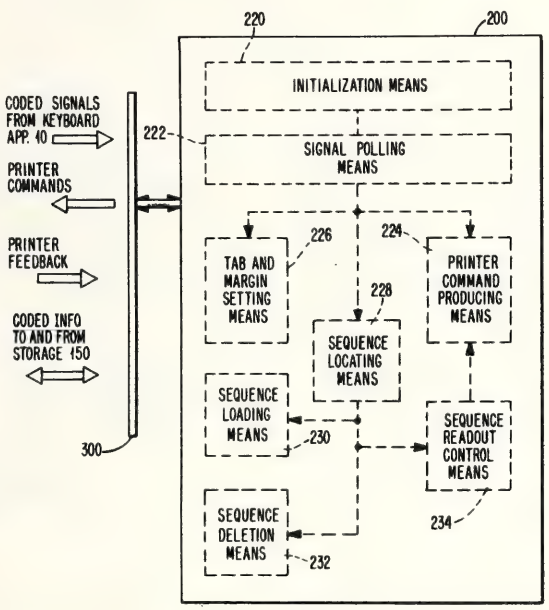
Primary Examiner—Gareth D. Shaw
Assistant Examiner—David Y. Eng
Attorney, Agent, or Firm—George E. Grosser

[57] **ABSTRACT**

Printing operation sequences (e.g. code sequences representing phases of text) entered along with identifier codes by means of typewriter keyboard are stored for selective individual retrieval and may be replaced on an individual basis as the needs of the typewriter operator may dictate. By using a special end loading procedure for adding new sequences, both storage overlapping and build-ups of unused storage locations between sequences are avoided so that storage integrity is maintained while storage usage remains, nonetheless, efficient.

In a preferred implementation, individual sequence retrieval capability is achieved by including in the respective sequences a common delimiter code along with a sequence identifier code. During bulk code transfers that occur when changes are made to the stored sequences, such delimiter and identifier codes are shifted routinely without being distinguished from the sequences they separate.

8 Claims, 6 Drawing Figures



United States Patent [19]

Dixon et al.

[11] **4,218,741**

[45] **Aug. 19, 1980**

[54] **PAGING MECHANISM**

[75] Inventors: **Jerry D. Dixon; Joel C. Leininger,** both of Boca Raton, Fla.

[73] Assignee: **International Business Machines Corporation,** Armonk, N.Y.

[21] Appl. No.: **918,221**

[22] Filed: **Jun. 23, 1978**

[51] **Int. Cl.**[2] **G06F 9/20**

[52] **U.S. Cl.** **364/200;** 364/900

[58] **Field of Search** ..... 364/200, 900 MS File

[56] **References Cited**

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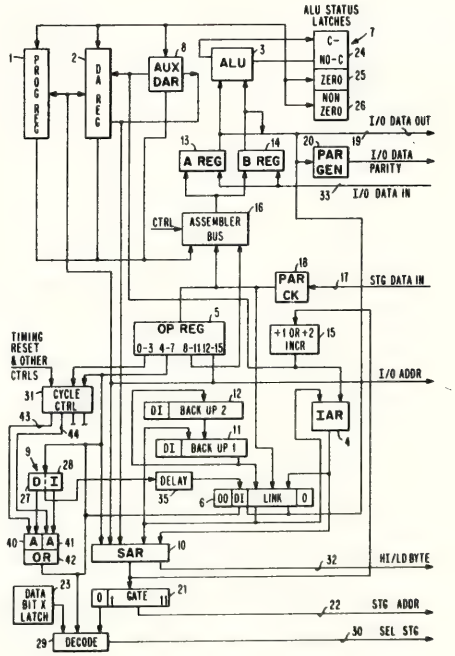
Primary Examiner—Gareth D. Shaw
Assistant Examiner—David Y. Eng
Attorney, Agent, or Firm—John C. Black

[57] **ABSTRACT**

In a data processing system, a mechanism provides independent assignment of page locations for a program's instructions and its data and better enables control to be transferred between programs, or portions thereof, that reside at different addresses in different pages of a multiple page instruction store. The initial linkage is established through the use of a Branch And Link instruction. Subsequent linkages are established through the use of Return and Link instructions, each of which transfers control to a previous program, or program segment, while simultaneously establishing the linkage for a subsequent return to this program or program segment.

9 Claims, 2 Drawing Figures



United States Patent [19]

Carlton et al.

[11] **4,218,742**

[45] **Aug. 19, 1980**

[54] **SYSTEM FOR CONTROLLING A SERIAL DATA CHANNEL WITH A MICROPROCESSOR**

[75] Inventors: **James E. Carlton; Werner J. Schaeuble**, both of San Jose, Calif.

[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[21] Appl. No.: **921,146**

[22] Filed: **Jun. 30, 1978**

[51] **Int. Cl.**[2] **G06F 13/00**

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** ... 364/200 MS File, 900 MS File; 360/48

[56] **References Cited**

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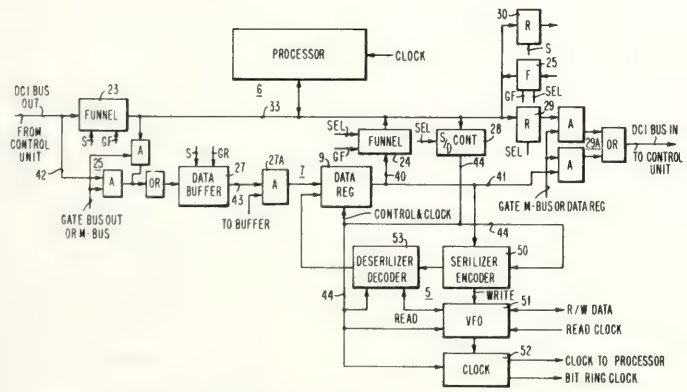
4,071,889	1/1978	Sumida et al.	364/900
4,155,117	5/1979	Mitchell et al.	364/200

Primary Examiner—Raulfe B. Zache
Attorney, Agent, or Firm—Richard E. Cummins

[57] **ABSTRACT**

A control system for a serial data channel for a disk file is disclosed in which a microcontroller is used as the control means. The microcontroller has an input port and an output port, while the serial data channel has a data register. The connections of the data register to the input and output port and the parallel by bit input and output busses on which write data and read data is sent provides a plurality of different data transfer loops through the data register which can be selected under the control of the microcontroller. The arrangement permits functions to be achieved by the microcontroller that heretofore were performed by another device connected to the controller or by special hardware.

13 Claims, 3 Drawing Figures



United States Patent [19]

Chang et al.

[11] **4,221,003**

[45] **Sep. 2, 1980**

[54] **BUBBLE DOMAIN RELATIONAL DATA BASE SYSTEM**

[75] Inventors: **Hsu Chang**, Yorktown Heights; **Anil Nigam**, Rochester, both of N.Y.

[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[21] Appl. No.: **902,641**

[22] Filed: **May 4, 1978**

[51] **Int. Cl.**[2] **G06F 7/00; G06F 13/00; G11G 11/14; G11G 19/08**

[52] **U.S. Cl.** **364/900; 365/15; 365/49**

[58] **Field of Search** ... 364/200 MS File, 900 MS File; 365/1, 5, 13, 15, 49, 50, 77, 78, 183; 340/146.2

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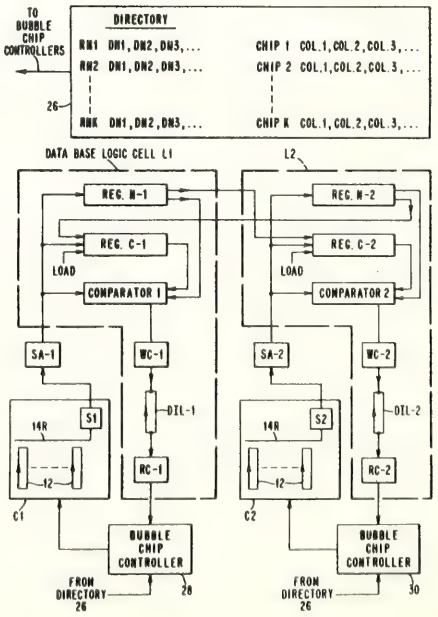
4,053,871	10/1977	Vidalin	364/900
4,128,891	12/1978	Lin	364/900

Primary Examiner—James D. Thomas
Attorney, Agent, or Firm—Jackson E. Stanland

[57] **ABSTRACT**

A relational data base system using magnetic bubble domain storage to eliminate data formatting, and dynamic indexing loops to facilitate convenient marking during data qualification and to eliminate redundant traversing of disqualified data during the search operation. A data base is stored in columnized storage tables which insure minimum input/output data traffic during search and retrieval. A suitable storage chip is organized in a major/minor loop organization, with several sections of transfer lines to provide selective access to individual groups of storage loops. Off-chip circuitry includes a comparator for comparing data read from a bubble storage chip with a given criterion in order to select appropriate data, and a dynamic indexing loop which keeps track of comparisons. This indexing loop provides an input to a bubble chip controller so that each subsequent search and compare is done only on already qualified data. This eliminates the need for repeated searching through the same data.

12 Claims, 9 Drawing Figures



United States Patent [19]
Lewis et al.
[11] **4,224,667**
[45] **Sep. 23, 1980**

[54] **COMMAND QUEUING FOR I/O ADAPTERS**

[75] Inventors: **David O. Lewis**, Rochester; **John W. Reed**, Pine Island; **Gary W. Wallin**, Mantorville, all of Minn.

[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[21] Appl. No.: **954,070**

[22] Filed: **Oct. 23, 1978**

[51] **Int. Cl.**[3] **G06F 3/00**
[52] **U.S. Cl.** **364/200**
[58] **Field of Search** 364/200, 900

[56] **References Cited**

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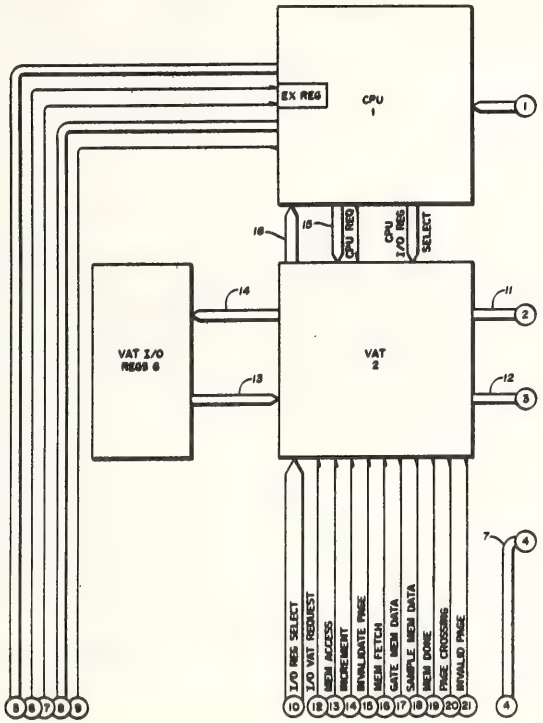
"Priority Interrupt Queuing" by Grant et al.; IBM Tech. Discl. Bulletin, vol. 15, No. 10, Mar. 1973, pp. 3046–3048.

Primary Examiner—Errol A. Krass
Attorney, Agent, or Firm—Dorsey, Windhorst, Hannaford, Whitney & Halladay

[57] **ABSTRACT**

In a computer system having: an addressable storage for storing instructions, data and input-output (I/O) commands; a central processing unit (CPU) which fetches and executes instructions; and channel means connecting I/O adapters to the storage and the CPU, an apparatus transfers I/O commands to the I/O adapters whereby the I/O command is either accepted immediately or is queued by the I/O adapter. A queued command is taken up by the I/O adapter when no other data transfer operation is pending. To take up a queued command, the I/O adapter initiates a fetch of the pending command by invoking a standard data-transfer-from-storage sequence. The channel means responds to the fetch initiated by the I/O adapter to send the pending command to the I/O adapter.

6 Claims, 35 Drawing Figures



United States Patent [19]
Bazlen et al.
[11] **4,231,085**
[45] **Oct. 28, 1980**

[54] **ARRANGEMENT FOR MICRO INSTRUCTION CONTROL**

[75] Inventors: **Dieter Bazlen**, Stuttgart; **Rolf Berger**, Schoenaich; **Arnold Blum**, Gechingen; **Dietrich W. Bock**; **Herbert Chilinski**, both of Schoenaich; **Hellmuth R. Geng**, Herrenberg; **Johann Hajdu**; **Fritz Irro**, both of Boeblingen; **Siegfried Neuber**, Sindelfingen, Udo Wille, Holzgerlingen, all of Fed. Republic of Germany

[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[21] Appl. No.: **934,781**

[22] Filed: **Aug. 18, 1978**

[30] **Foreign Application Priority Data**

Oct. 21, 1977 [DE] Fed. Rep. of Germany 2747304

[51] **Int. Cl.**[2] **G06F 9/12**
[52] **U.S. Cl.** **364/200**
[58] **Field of Search** ... 364/200 MS File, 900 MS File

[56] **References Cited**

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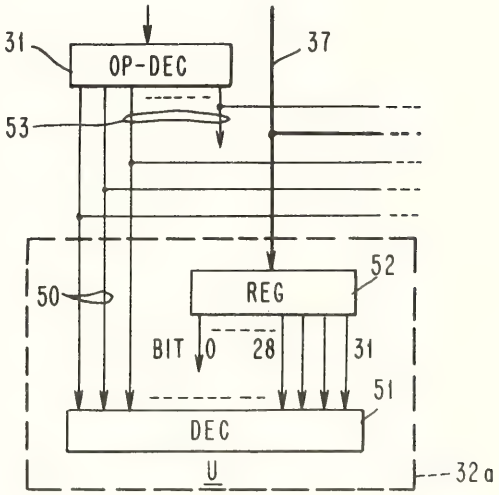
IBM Sys/370 Principles of Operation, p. 212.
"Specify Microcode Emit by Destination Field," Grice et al., IBM Tech. Disclosure Bull., vol. 20, No. 7, Dec. 1977, pp. 2556–2567.

Primary Examiner—Gareth D. Shaw
Assistant Examiner—E. Chan
Attorney, Agent, or Firm—Robert Lieber

[57] **ABSTRACT**

In a micro-controlled data handling system the number of lines and pins required to transfer control signals from the microprogram controls to be integrated circuit modules controlled by such signals is conserved by using two bussing paths for distributing the control signals to the modules. A first path is dedicated exclusively to pre-decoded control signal functions and a second path is shared for transferring both data and control signal functions. Each controlled module contains an additional decoding circuit for combinationally decoding control signal functions received through both paths.

5 Claims, 7 Drawing Figures



United States Patent [19]

Someshwar

[11] **4,190,897**

[45] **Feb. 26, 1980**

[54] **BINARY CODED DECIMAL ADDRESSED READ-ONLY-MEMORY**

[75] Inventor: **Ashok H. Someshwar**, Richardson, Tex.

[73] Assignee: **Texas Instruments Incorporated**, Dallas, Tex.

[21] Appl. No.: **783,516**

[22] Filed: **Apr. 1, 1977**

[51] **Int. Cl.**[2] **G11C 8/00**; G11C 17/00

[52] **U.S. Cl.** **364/900**; 365/230

[58] **Field of Search** ..... 364/200, 900 MS File; 365/94, 95, 96, 97, 98, 99, 100, 101, 102, 103, 104, 105, 230, 239, 240

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,921,142	11/1975	Bryant et al.	364/900

Primary Examiner—Gareth D. Shaw

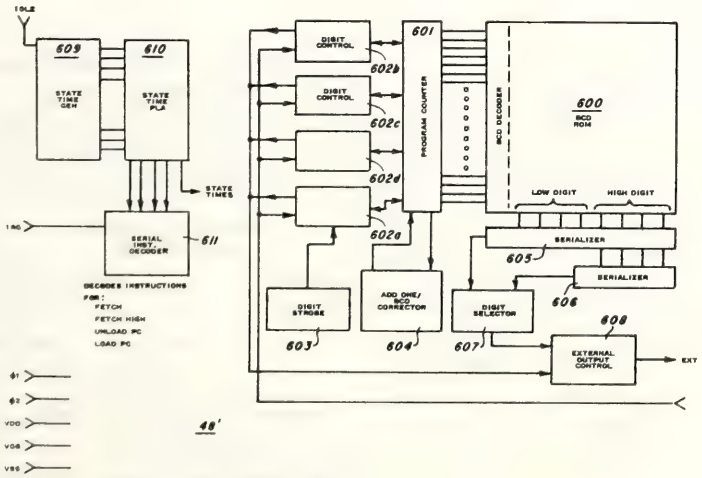
Assistant Examiner—Thomas M. Heckler

Attorney, Agent, or Firm—William K. McCord; James T. Comfort; Melvin Sharp

[57] **ABSTRACT**

A Read-Only-Memory (ROM) is addressed with a binary coded decimal (BCD) address in an address register or program counter. The ROM comprises an array of memory cells with associated row and column lines for addressing the array. Row and column decoders responsive to the address in the address register identify a unique row and column line for each BCD address. The row and column decoders comprise a plurality of decoders in cascaded levels. The decorders in any given level decode particular bits of the address in the address register; these decoders decode a one-out-of-a-prime-number, which prime number is a factor of the number of memory locations in the array.

4 Claims, 60 Drawing Figures



United States Patent [19]

Cornish et al.

[11] **4,197,589**

[45] **Apr. 8, 1980**

[54] **OPERATION SEQUENCING MECHANISM**

[75] Inventors: **Merrill A. Cornish**, Austin; **David M. Chastain**, Plano; **John C. Jensen**, Austin, all of Tex.

[73] Assignee: **Texas Instruments Incorporated**, Dallas, Tex.

[21] Appl. No.: **857,630**

[22] Filed: **Dec. 5, 1977**

[51] **Int. Cl.**[2] **G06F 9/18**

[52] **U.S. Cl.** **364/900**

[58] **Field of Search** ... 364/200 MS File, 900 MS File

[56] **References Cited**

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4,047,161	9/1977	Davis	364/200

Primary Examiner—Gareth D. Shaw

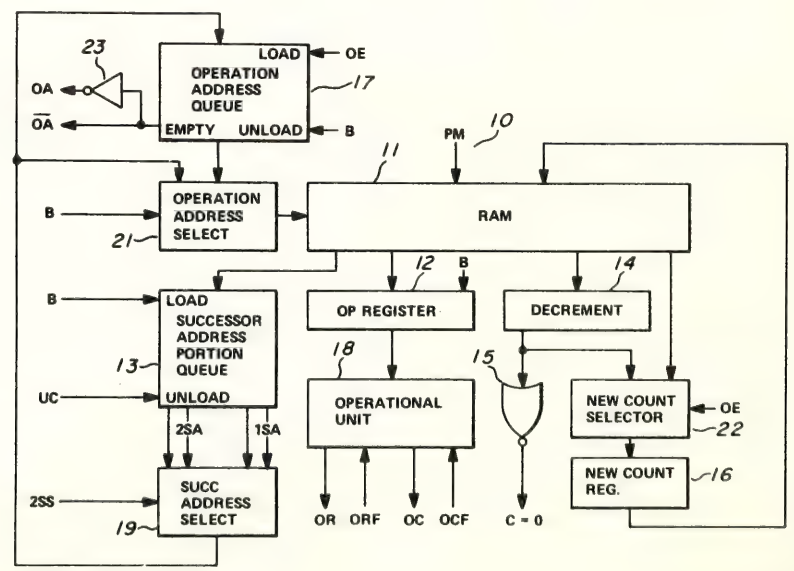
Assistant Examiner—E. Chan

Attorney, Agent, or Firm—Melvin Sharp; Leo N. Heiting; Thomas G. Devine

[57] **ABSTRACT**

A mechanism, including a memory, sequences operation in a controlled processor. Each operation is stored in memory together with a portion indicating the current state of predecessor operations required to be completed before execution of the current operation. Also associated with the current operation is provision for at least one address of a successor operation. A predecessor portion is updated as the predecessor operations are performed and at a predetermined state, the current operation is sent to the controlled processor for processing. Following the processing, the operations at the successor addresses have their predecessor portions updated. Thus, the order in which the operations are performed is totally independent of an arbitrary sequencing and instead is dependent only upon availability.

22 Claims, 6 Drawing Figures



United States Patent [19]
Cochran et al.
[11] **4,200,926**
[45] **Apr. 29, 1980**

[54] **ELECTRONIC CALCULATOR IMPLEMENTED IN SEMICONDUCTOR LSI CHIPS WITH SCANNED KEYBOARD AND DISPLAY**

[75] Inventors: **Michael J. Cochran; Jerry L. Vandierendonck**, both of Houston, Tex.

[73] Assignee: **Texas Instruments Incorporated**, Dallas, Tex.

[21] Appl. No.: **444,226**

[22] Filed: **Feb. 20, 1974**

Related U.S. Application Data

[63] Continuation of Ser. No. 255,856, May 22, 1972.

[51] **Int. Cl.**[2] **G06F 3/02; G06F 7/48**
[52] **U.S. Cl.** ..... **364/200; 340/365 S**
[58] **Field of Search** ..... 340/172.5, 365 S; 445/1; 364/200 MS File, 900 MS File, 709, 710

[56] **References Cited**

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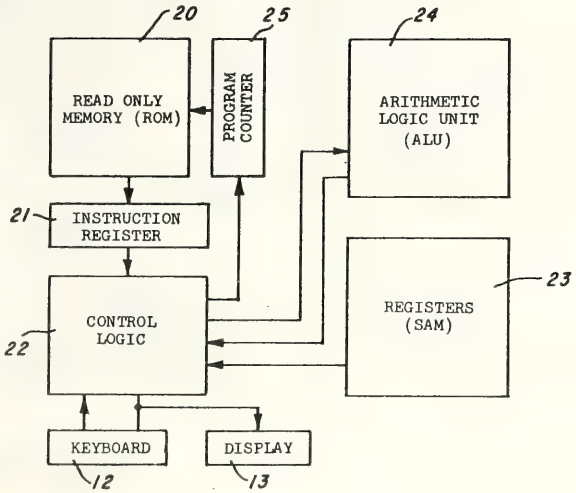
3,855,577	12/1974	Vandierendonck	340/172.5
3,892,957	7/1975	Bryant	340/172.5

Primary Examiner—Mark E. Nusbaum
Attorney, Agent, or Firm—John G. Graham

[57] **ABSTRACT**

An electronic desk top calculator implemented in MOS/LSI technology and including a scanned keyboard input and display output. Data registers are provided in a sequentially addressed random access memory array, which is addressed by a commutator also used to generate encoded timing signals for other parts of the system and control logic. The keyboard input includes an interface register into which is entered key sense line information along with encoded timing information derived from the encoded timing signals. The contents of the interface register may be entered into the data registers or used to select an address in a program storage memory via a program counter. Bits may be read out in parallel from cells in the data registers and processed through an arithmetic logic unit and then re-entered in the same cells within a bit time or state time, so the data registers do not recirculate in the usual sense.

35 Claims, 67 Drawing Figures



United States Patent [19]
Schmidt
[11] **4,213,177**
[45] **Jul. 15, 1980**

[54] **EIGHT BIT STANDARD CONNECTOR BUS FOR SIXTEEN BIT MICROCOMPUTER USING MIRRORED MEMORY BOARDS**

[75] Inventor: **Robert W. Schmidt**, Stafford, Tex.

[73] Assignee: **Texas Instruments Incorporated**, Dallas, Tex.

[21] Appl. No.: **898,735**

[22] Filed: **Apr. 24, 1978**

[51] **Int. Cl.**[2] **G06F 13/00**
[52] **U.S. Cl.** **364/200; 365/63**
[58] **Field of Search** ... 364/200 MS File, 900 MS File; 365/230, 63, 191, 220, 221

[56] **References Cited**

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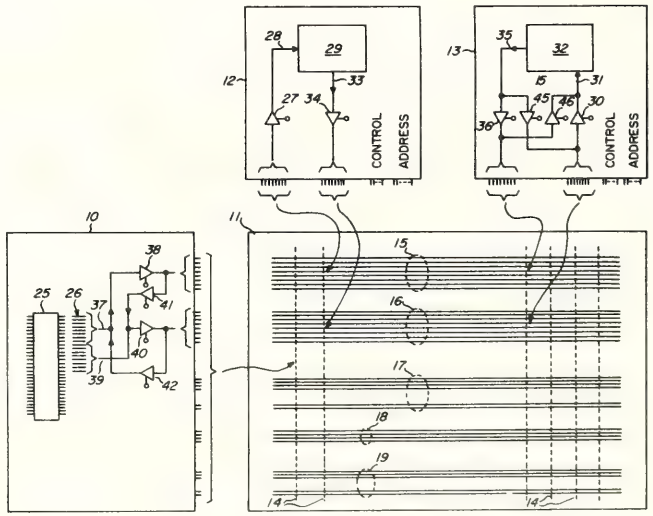
Morrow et al., "Proposed Standard for the S-100 Bus," NCC '78, Personal Computing Digest, 5/78, p. 305.
Notari, "A 16 Bit System for the S-100 Bus That Holds its Own Against A Mini," Interface Age, 7/77, pp. 72, 73.

Primary Examiner—Mark E. Nusbaum
Attorney, Agent, or Firm—John G. Graham

[57] **ABSTRACT**

A microcomputer system uses a standardized S-100 bus with eight bit Data In and eight bit Data Out lines, but has a sixteen bit microprocessor with sixteen bit bidirectional data input/output terminals. An arrangement of mirror image pairs of memory boards is provided to cross-connect the Data In lines and Data Out lines for one memory board compared to another, these two memory boards being accessed by the same address. A processor board containing the microprocessor connects the Data In and Data Out lines to the data input-/output terminals by controllable undirectional buffers which criss-cross the bytes on write compared to read operations.

9 Claims, 1 Drawing Figure



United States Patent [19]

Schmidt

[11] **4,214,302**

[45] **Jul. 22, 1980**

[54] **EIGHT BIT STANDARD CONNECTOR BUS FOR SIXTEEN BIT MICROCOMPUTER**

[75] Inventor: **Robert W. Schmidt**, Stafford, Tex.

[73] Assignee: **Texas Instruments Incorporated**, Dallas, Tex.

[21] Appl. No.: **898,736**

[22] Filed: **Apr. 24, 1978**

[51] **Int. Cl.**[2] **G06F 13/00**

[52] **U.S. Cl.** **364/200**; 365/63

[58] **Field of Search** ... 364/200 MS File, 900 MS File; 365/230, 63, 191, 220, 221

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,938,098	2/1976	Garlic	364/200
4,016,546	4/1977	Bennett et al.	364/200
4,057,846	11/1977	Cockerill et al.	364/200

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Morrow et al., "Proposed Standard for the S-100 Bus" NCC 1978, Personal Computing Digest, 5/78, p. 305.

Notari, "A 16 Bit System for the S-100 Bus that Holds its Own Against a Mini", Interface Age, 7/77, pp. 72, 73.

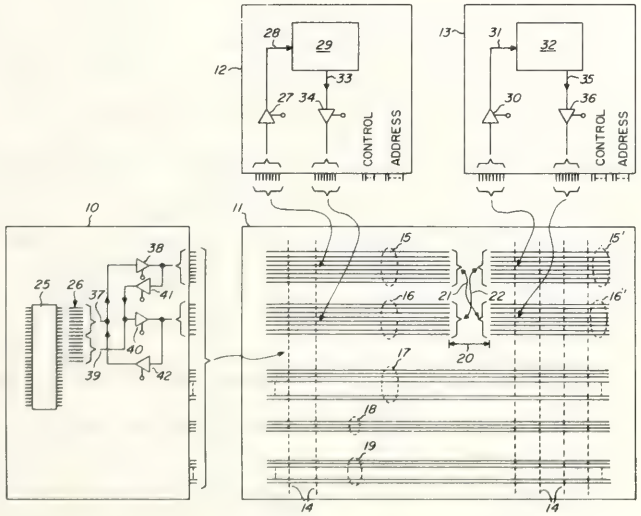
Primary Examiner—Mark E. Nusbaum

Attorney, Agent, or Firm—John G. Graham

[57] **ABSTRACT**

A microcomputer system uses a standardized S-100 bus with eight bit Data In and eight bit Data Out lines, but has a sixteen bit microprocessor with sixteen bit bidirectional data input/output terminals. An arrangement is provided to cross-connect the Data In lines and Data Out lines for one memory board compared to another, these two memory boards being accessed by the same address. A processor board containing the microprocessor connects the Data In and Data Out lines to the data input/output terminals by controllable unidirectional buffers which criss-cross the bytes on write compared to read operations.

6 Claims, 1 Drawing Figure



United States Patent [19]

Bunyard et al.

[11] **4,215,395**

[45] **Jul. 29, 1980**

[54] **DUAL MICROPROCESSOR INTELLIGENT PROGRAMMABLE PROCESS CONTROL SYSTEM**

[75] Inventors: **Michael L. Bunyard**, Lubbock; **Bobby G. Burkett**, Richardson, both of Tex.

[73] Assignee: **Texas Instruments Incorporated**, Dallas, Tex.

[21] Appl. No.: **936,533**

[22] Filed: **Aug. 24, 1978**

[51] **Int. Cl.**[2] **G06F 15/16**; G06F 15/46

[52] **U.S. Cl.** **364/101**; 364/103; 364/200

[58] **Field of Search** ..... 364/100, 101, 102, 103, 364/107, 120, 474, 200 MS File, 900 MS File

[56] **References Cited**

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3,959,775	5/1976	Valassis et al.	364/200
4,029,950	6/1977	Haga	364/104
4,034,354	7/1977	Simmons	364/104 X
4,058,711	11/1977	Ondercin et al.	364/101
4,064,395	12/1977	Schubeller et al.	364/107
4,118,771	10/1978	Pomella et al.	364/101
4,149,235	4/1979	Froyd et al.	364/107 X

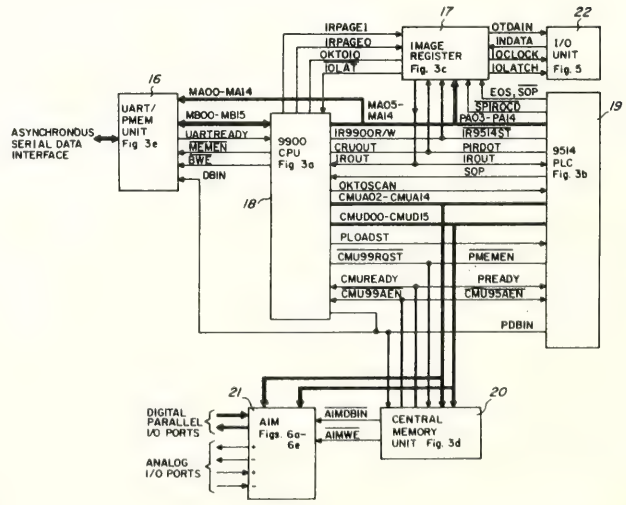
Primary Examiner—Joseph F. Ruggiero

Attorney, Agent, or Firm—Andrew M. Hassell; Rene' E. Grossman; Stephen S. Sadacca

[57] **ABSTRACT**

An intelligent programmable process control system for controlling industrial processing and manufacturing equipment and the like utilizes a unique system of cooperating multiple microprocessors. A multi-bit microprocessor is utilized for controlling the analog portion of the processing equipment, and a single-bit microprocessor is utilized for sequencing. The control processor has overall supervisory control. An arbitration circuit for resolving simultaneous or phased access to memory by the two microprocessors is provided. In addition, a circuit is provided for accomplishing parallel I/O, again accessible by both microprocessors. In one embodiment, means for linking arithmetic functions and non-arithmetic (logic) functions within a boolean-type instruction set is provided.

36 Claims, 17 Drawing Figures



United States Patent [19]

Henry et al.

[11] **4,215,396**

[45] **Jul. 29, 1980**

[54] **INTELLIGENT PROGRAMMABLE PROCESS CONTROL SYSTEM**

[75] Inventors: **Raymond W. Henry**, Dallas; **Bobby G. Burkett**, Richardson; **Michael L. Bunyard**, Lubbock, all of Tex.

[73] Assignee: **Texas Instruments Incorporated**, Dallas, Tex.

[21] Appl. No.: **936,538**

[22] Filed: **Aug. 24, 1978**

[51] **Int. Cl.**[2] **G06F 15/16**; G06F 15/46

[52] **U.S. Cl.** **364/101**; 364/200; 364/103

[58] **Field of Search** ..... 364/100, 101, 102, 103, 364/107, 120, 474, 200 MS File, 900 MS File

[56] **References Cited**

U.S. PATENT DOCUMENTS

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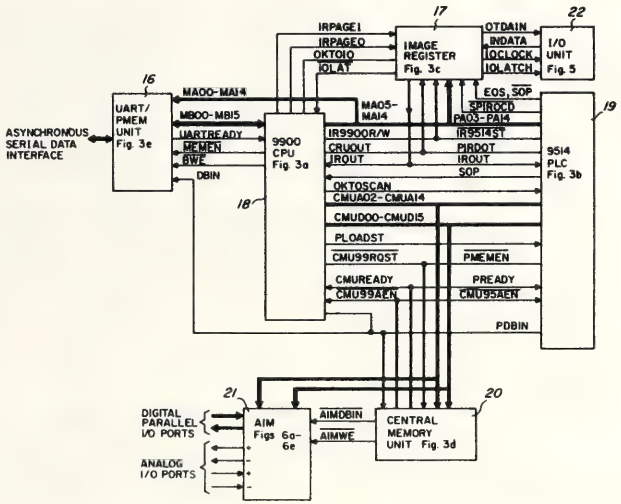
4,029,950	6/1977	Haga	364/104
4,034,354	7/1977	Simmons	364/104 X
4,058,711	11/1977	Ondercin et al.	364/101
4,064,395	12/1977	Schubeller et al.	364/107
4,118,771	10/1978	Pomella et al.	364/101
4,149,235	4/1979	Froyd et al.	364/107 X

Primary Examiner—Joseph F. Ruggiero
Attorney, Agent, or Firm—Andrew M. Hassell; Rene' E. Grossman; Stephen S. Sadacca

[57] **ABSTRACT**

An intelligent programmable process control system for controlling industrial processing and manufacturing equipment and the like utilizes a unique system of cooperating multiple processors. A digital processor is utilized for controlling the analog portion of the processing equipment, and a boolean processor is utilized for sequencing and controlling the on/off states of controllable devices. Along the process communication means is provided for communications between the processors. In one embodiment, a circuit is provided for accomplishing parallel digital I/O, accessible by the digital processor for additional control of the analog processing equipment.

6 Claims, 17 Drawing Figures



United States Patent [19]

Hom

[11] **4,215,397**

[45] **Jul. 29, 1980**

[54] **AUTOMATIC END-OF-SCAN CONTROL SYSTEM FOR A PROGRAMMABLE PROCESS CONTROLLER WITH EXPANDABLE MEMORY**

[75] Inventor: **Gim P. Hom**, Sharon, Mass.

[73] Assignee: **Texas Instruments Incorporated**, Dallas, Tex.

[21] Appl. No.: **936,547**

[22] Filed: **Aug. 24, 1978**

[51] **Int. Cl.**[2] **G06F 15/16**; G06F 15/46

[52] **U.S. Cl.** **364/101**; 364/103; 364/200

[58] **Field of Search** ..... 364/100, 101, 102, 103, 364/104, 107, 120, 474, 200 MS File, 900 MS File

[56] **References Cited**

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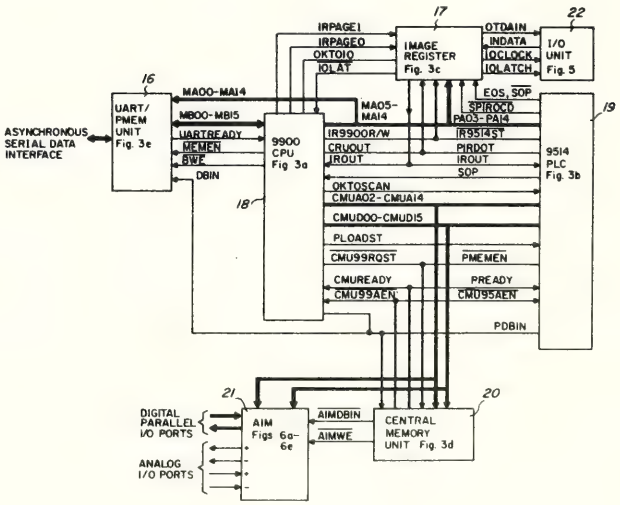
4,058,711	11/1977	Ondercin et al.	364/101
4,064,395	12/1977	Schubeler et al.	364/107
4,118,771	10/1978	Pomella et al.	364/101
4,149,235	4/1979	Froyd et al.	364/107 X

Primary Examiner—Joseph F. Ruggiero
Attorney, Agent, or Firm—Andrew M. Hassell; Rene' E. Grossman; Stephen S. Sadacca

[57] **ABSTRACT**

An intelligent programmable process control system is responsive to the states of sensors located along a process for controlling the states of controllable devices located along the process. The system includes a microprocessor which sequentially scans an addressable memory to execute a sequence of boolean logic instructions in accordance with the states of the sensors to control the controllable devices accordingly. The microprocessor includes means for generating an end-of-scan signal upon execution of the last instruction of a sequence contained in memory. Receptor means is provided for receiving extended addressable memory for storing additional instructions of the sequence if required, the receptor means including indicator signal generator means for generating a signal indicative of the presence of such extended memory in the receptor means. An end-of-scan generator means, coupled to the indicator signal generator means, automatically generates an end-of-scan signal whenever the extended memory means is addressed by the microprocessor means and the indicator signal generator indicates that the receptor does not contain extended memory. The end-of-scan signals provided by the microprocessor and the end-of-scan signal generator are utilized to control the microprocessor to begin rescanning the addressable memory, as well as, controlling the transfer of data to a communications register which communicates with the sensors and controllable devices.

10 Claims, 17 Drawing Figures



United States Patent [19]

Burkett et al.

[11] **4,215,398**

[45] **Jul. 29, 1980**

[54] **DUAL MICROPROCESSOR INTELLIGENT PROGRAMMABLE PROCESS CONTROL SYSTEM WITH COMMUNICATION LINK**

[75] Inventors: **Bobby G. Burkett**, Richardson; **Michael L. Bunyard**, Lubbock, both of Tex.

[73] Assignee: **Texas Instruments Incorporated**, Dallas, Tex.

[21] Appl. No.: **936,422**

[22] Filed: **Aug. 24, 1978**

[51] **Int. Cl.**[2] **G06F 15/46**; G06F 15/16

[52] **U.S. Cl.** **364/101**; 364/200

[58] **Field of Search** ..... 364/101, 102, 100, 103, 364/104, 107, 120, 474, 200 MS File, 900 MS File

[56] **References Cited**

U.S. PATENT DOCUMENTS

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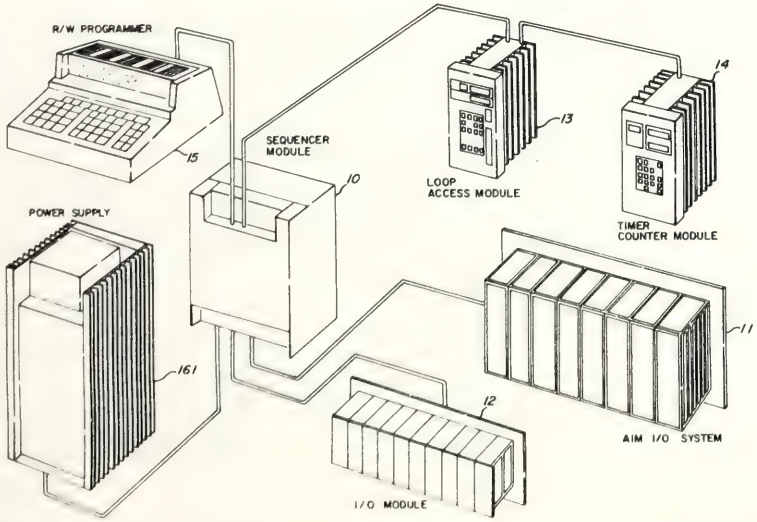
4,034,354	7/1977	Simmons	364/104 X
4,058,711	11/1977	Ondercin et al.	364/101
4,064,395	12/1977	Schubeler et al.	364/107
4,118,771	10/1978	Pomella et al.	364/101
4,149,235	4/1979	Froyd et al.	364/107 X

Primary Examiner—Joseph F. Ruggiero
Attorney, Agent, or Firm—Andrew M. Hassell; Rene' E. Grossman; Stephen S. Sadacca

[57] **ABSTRACT**

An intelligent programmable process control system for controlling industrial processing and manufacturing equipment and the like utilizes a unique system of cooperating dual microprocessors. A digital microprocessor is utilized for digital computation and for controlling the analog portion of the processing equipment, and a boolean microprocessor is utilized for sequencing and for controlling the on/off states of devices located along the process in response to the on/off states of sensors located along the process according to a sequence of boolean logic functions. The digital microprocessor has overall supervisory control. Common memory provides a communication link between the two microprocessors. An arbitration circuit for resolving simultaneous or phased access to memory by the two microprocessors is provided. In addition, a circuit is provided for accomplishing parallel digital input/output functions, again accessible by both microprocessors. In one embodiment, means for linking arithmetic functions and non-arithmetic logic functions within a boolean-type instruction set is provided.

34 Claims, 17 Drawing Figures



United States Patent [19]

Pavicic et al.

[11] **4,215,399**

[45] **Jul. 29, 1980**

[54] **SPECIAL FUNCTION CONTROL SYSTEM FOR A DUAL MICROPROCESSOR PROGRAMMABLE PROCESS CONTROL SYSTEM**

[75] Inventors: **Mark J. Pavicic; Jack L. Mahaffey, II**, both of Dallas, Tex.

[73] Assignee: **Texas Instruments Incorporated**, Dallas, Tex.

[21] Appl. No.: **936,532**

[22] Filed: **Aug. 24, 1978**

[51] **Int. Cl.**[2] **G06F 15/16**; G06F 15/46

[52] **U.S. Cl.** **364/101**; 364/107; 364/200

[58] **Field of Search** ..... 364/100, 101, 102, 103, 364/104, 107, 120, 474, 200 MS File, 900 MS File

[56] **References Cited**

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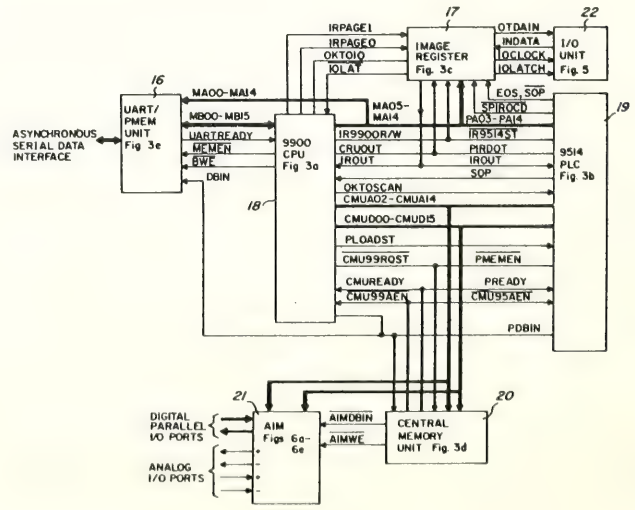
3,959,775	5/1976	Valassis et al.	364/200
4,029,950	6/1977	Haga	364/104
4,034,354	7/1977	Simmons	364/104 X
4,058,711	11/1977	Ondercin et al.	364/101
4,064,395	12/1977	Schubeler et al.	364/107
4,118,771	10/1978	Pomella et al.	364/101
4,149,235	4/1979	Froyd et al.	364/107 X

Primary Examiner—Joseph F. Ruggiero
Attorney, Agent, or Firm—Andrew M. Hassell; Rene' E. Grossman; Stephen S. Sadacca

[57] **ABSTRACT**

An intelligent programmable process control system including a first microprocessor which scans and executes a sequence of boolean logic functions and a second microprocessor which performs complex operations including arithmetic computations beyond the capabilities of the first microprocessor. The first microprocessor transmits interrupt requests to the second microprocessor when a scanned sequence instruction requires complex operations to be performed. First flag bit register indicates to the first microprocessor that a requested operation has been queued-up. Second flag bit register indicates to the first microprocessor that the requested operation has been completed. When the first microprocessor requires complex operations, it checks the state of a respective first flag bit register to determine whether the complex operation has already been queued-up and if so, checks the state of a respective second flag bit register to determine whether the queued-up function has been completed by the second microprocessor. If the complex operation has been queued-up and the second flag bit indicates that the operation has not been completed, the first microprocessor continues scanning and executing its sequence of functions asynchronously with respect to the second microprocessor. If the first flag bit indicates that the operation has not been queued-up, then the first microprocessor transmits an interrupt request to the second microprocessor.

26 Claims, 17 Drawing Figures



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United States Patent [19]
Appelt
[11] **4,224,676**
[45] **Sep. 23, 1980**

[54] **ARITHMETIC LOGIC UNIT BIT-SLICE WITH INTERNAL DISTRIBUTED ITERATIVE CONTROL**

[75] Inventor: **Daren R. Appelt**, Austin, Tex.

[73] Assignee: **Texas Instruments Incorporated**, Dallas, Tex.

[21] Appl. No.: **920,754**

[22] Filed: **Jun. 30, 1978**

[51] **Int. Cl.**[3] **G06F 7/48**
[52] **U.S. Cl.** **364/712**; 364/900
[58] **Field of Search** 364/712, 200, 900

[56] **References Cited**

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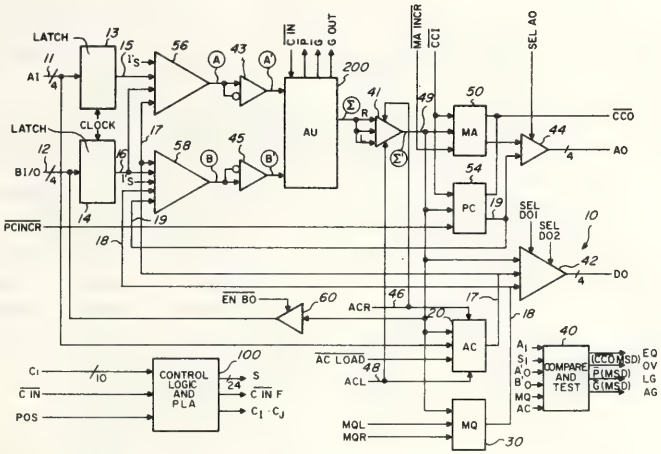
4,093,993	6/1978	Sato	364/712

Primary Examiner—David H. Malzahn
Attorney, Agent, or Firm—Thomas G. Devine; Leo N. Heiting; Melvin S. Sharp

[57] **ABSTRACT**

An arithmetic logic unit bit-slice implemented as an integrated circuit is able to perform iterative algorithms such as multiply and divide, using control logic which is also part of the integrated circuit to cause the selected algorithm to be performed. A plurality of the arithmetic logic unit bit-slices may be concatenated to provide the word size desired. The bit-slices are electrically identified as the most significant, least significant, and middle digits, such identification being provided to the control logic so that the control logic is identical on each bit-slice irresepective of its position within a word to enable the control logic to cause performance of the algorithms for any desired word length.

10 Claims, 26 Drawing Figures



United States Patent [19]
Harrington et al.
[11] **4,200,912**
[45] **Apr. 29, 1980**

[54] **PROCESSOR INTERRUPT SYSTEM**

[75] Inventors: **Wayne D. Harrington; Fuad H. Musa**, both of Austin, Tex.

[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **929,636**

[22] Filed: **Jul. 31, 1978**

[51] **Int. Cl.**[2] **G06F 9/18**
[52] **U.S. Cl.** **364/200**
[58] **Field of Search** ... 364/200 MS File, 900 MS File

[56] **References Cited**

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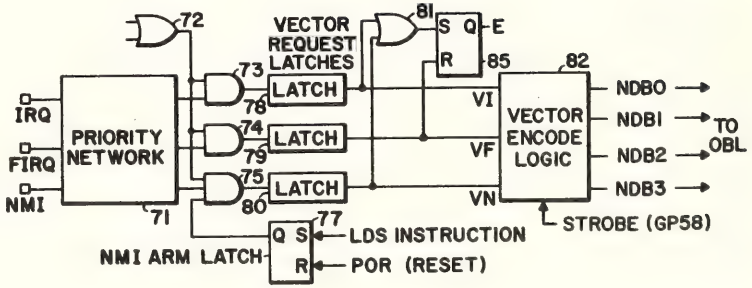
Primary Examiner—Raulfe B. Zache
Attorney, Agent, or Firm—Joe E. Barbee

[57] **ABSTRACT**

A digital data processor having the capability of handling more than one interrupt wherein one of the interrupts is a fast interrupt is provided. Interrupts are received by a priority network which establishes the priority of the interrupts should more than one interrupt occur at the same time. The output of the priority network is stored in a latch and the output of the latch is coupled to a vector and code logic circuit which encodes the vector address for the interrupt received. Whenever a fast interrupt is received a flag is set in a storage means so that when the system returns from interrupt it will be able to determine whether a fast interrupt had been serviced or not.

9 Claims, 7 Drawing Figures



United States Patent [19]

Bennett et al.

[11] **4,218,740**

[45] **Aug. 19, 1980**

[54] **INTERFACE ADAPTOR ARCHITECTURE**

[75] Inventors: **Thomas H. Bennett; Earl F. Carlow,** both of Scottsdale; **Edward C. Hepworth,** Apache Junction, all of Ariz.; **William D. Mensch, Jr.; Charles I. Peddle,** both of Norristown, Pa.; **Gene A. Schriber,** Tempe; **Michael F. Wiles,** Phoenix, both of Ariz.

[73] Assignee: **Motorola, Inc.,** Schaumburg, Ill.

[21] Appl. No.: **757,120**

[22] Filed: **Jan. 5, 1977**

Related U.S. Application Data

[63] Continuation of Ser. No. 519,138, Oct. 30, 1974.

[51] **Int. Cl.**[3] **G06F 3/00**

[52] **U.S. Cl.** ..... **364/200;** 340/147 R

[58] **Field of Search** ... 364/200 MS File, 900 MS File; 340/147 R, 147 C, 147 CN, 147 CV

[56] **References Cited**

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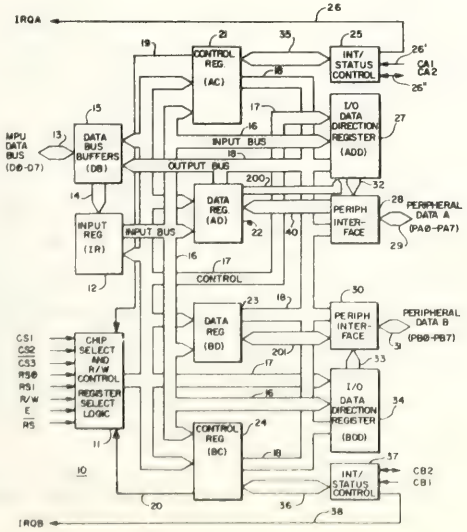
Primary Examiner—Mark E. Nusbaum
Attorney, Agent, or Firm—Walter W. Nielsen

[57] **ABSTRACT**

A peripheral interface adaptor (PIA) circuit for data processing systems contains memory elements or control registers allowing modification under program control of the logical functions of the PIA.

The peripheral interface adaptor includes a plurality of system data bus buffer circuits coupled to a system data bus and further includes peripheral interface buffer circuits coupled to a bidirectional peripheral data bus. The direction of data flow in the peripheral data bus is controlled by a data direction register. Data from the system data bus buffer is entered into an input register, and is transferred from there to an input bus coupled to the control register, a data direction register and a data register. Data from the peripheral data bus, the data direction register and the control register are transferred via an output bus to the system data bus buffers. Control signals are generated by select, read/write control, and register select logic which provides signals on a control bus coupled to the input register, the data register, the control register, and the data direction register to control data transfers between the various buses, registers, and buffer circuits.

8 Claims, 13 Drawing Figures



United States Patent [19]

Mallien, II

[11] **4,220,820**

[45] * **Sep. 2, 1980**

[54] **CONTROL CIRCUITRY FOR A RADIO TELEPHONE**

[75] Inventor: **Thomas O. Mallien, II,** Palatine, Ill.

[73] Assignee: **Motorola, Inc.,** Schaumburg, Ill.

[*] Notice: The portion of the term of this patent subsequent to Oct. 24, 1995, has been disclaimed.

[21] Appl. No.: **948,356**

[22] Filed: **Oct. 2, 1978**

Related U.S. Application Data

[63] Continuation of Ser. No. 783,888, Apr. 1, 1977, Pat. No. 4,122,304.

[51] **Int. Cl.**[2] **H04M 11/00; H04M 1/27**

[52] **U.S. Cl.** ..... **179/2 EB;** 179/90 B; 364/900

[58] **Field of Search** ..... 179/2 E, 2 EA, 2 EB, 179/90 K, 90 B; 325/53, 55, 64, 15, 16, 25; 364/200 MS File, 900 MS File

[56] **References Cited**

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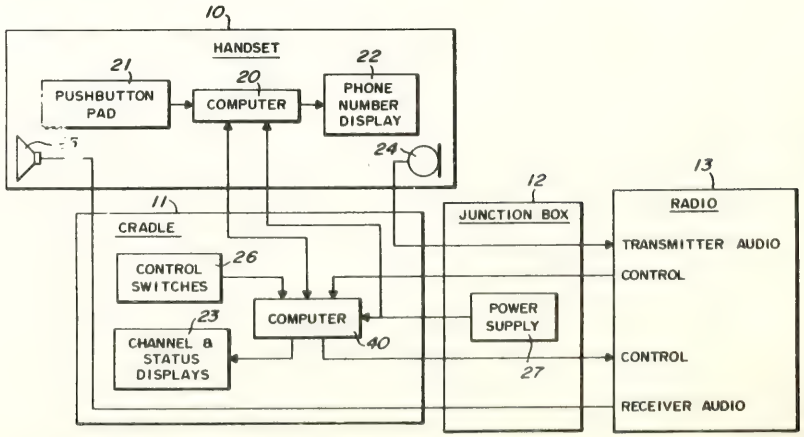
Primary Examiner—James W. Moffitt
Assistant Examiner—Joseph A. Popek
Attorney, Agent, or Firm—Rolland R. Hackbart; James W. Gillman

[57] **ABSTRACT**

A control circuitry for a radio telephone having a transmitter, a receiver, a cradle and a handset. The handset includes a first computer having a stored program control therein, a first memory, a telephone number display and a pushbutton pad. The cradle includes a second computer having a stored program control therein, a second memory, a plurality of control switches and radio telephone status indicators. A dialed number is entered into the handset memory from the pushbutton pad, under control of the handset computer. Then during a telephone call, the entered number is transferred from the handset computer to the cradle computer and transmitted by the cradle computer. Frequently called numbers can be stored in the handset memory or the cradle memory and later, can be readily recalled and transmitted. The last dialed number can be automatically retransmitted in a subsequent call.

30 Claims, 14 Drawing Figures



United States Patent [19]
Magerl

[11] **4,222,038**
[45] **Sep. 9, 1980**

[54] **MICROCOMPUTER KEYBOARD INPUT CIRCUITRY**

[75] Inventor: **Richard A. Magerl**, Schaumburg, Ill.

[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **881,090**

[22] Filed: **Feb. 24, 1978**

[51] **Int. Cl.**[3] **G06F 3/02**
[52] **U.S. Cl.** ..... **340/365 S**; 364/200
[58] **Field of Search** ..... 340/365 R, 365 S, 365 E; 365/240; 178/17 C; 179/90 K; 364/705, 706, 709, 710, 200 MS File, 900 MS File; 400/479, 472

[56] **References Cited**

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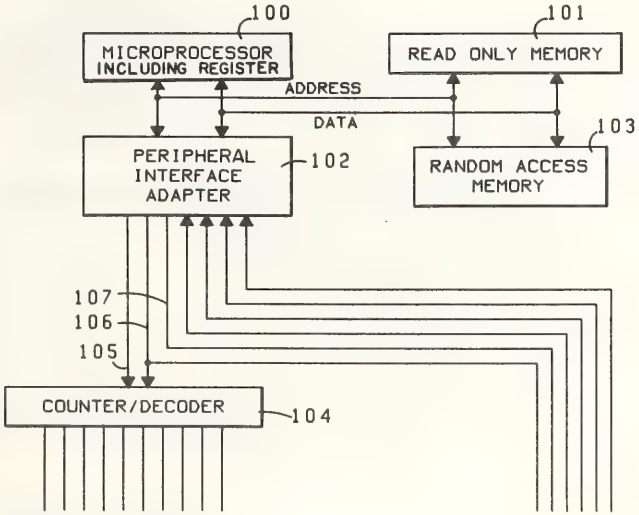
4,030,079	6/1977	Bennett et al.	364/200
4,106,011	8/1978	Melanson et al.	340/365 S

Primary Examiner—John W. Caldwell, Sr.
Assistant Examiner—James J. Groody
Attorney, Agent, or Firm—Rolland R. Hackbart; James W. Gillman

[57] **ABSTRACT**

Keyboard input circuitry for use in a microcomputer continuously scans a keyboard having a plurality of keys organized into K columns and J rows. A counter under control of a reset signal and clock signal, sequentially provides K output signals for enabling the K column conductors. When a key in the Kth column and Jth row is depressed, the Kth output signal from the counter will be coupled to the Jth row. Thus, the logical state of the J row conductors will determine whether or not a key of the enabled column of keys is depressed or not. The microcomputer includes a register, a memory, and a peripheral interface adapter circuit. The microcomputer provides the reset signal and clock signal to the register and to the counter by way of the peripheral interface adapter circuit, for maintaining synchronism between the register and counter. For each enabled column of keys, the microcomputer senses the logical states of the J row conductors via the peripheral interface adapter circuit, and then ascertains whether or not a particular key is depressed by the sensed logical state of its row conductor and the state of the register.

5 Claims, 4 Drawing Figures



United States Patent [19]
Chamberlin

[11] **4,222,103**
[45] **Sep. 9, 1980**

[54] **REAL TIME CAPTURE REGISTERS FOR DATA PROCESSOR**

[75] Inventor: **George P. Chamberlin**, Tempe, Ariz.

[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **945,737**

[22] Filed: **Sep. 25, 1978**

[51] **Int. Cl.**[3] **G06F 7/00**
[52] **U.S. Cl.** ..... **364/200**; 235/92 T
[58] **Field of Search** ..... 235/92 T; 364/900 MS File, 200 MS File, 300; 307/208, 213, 293

[56] **References Cited**

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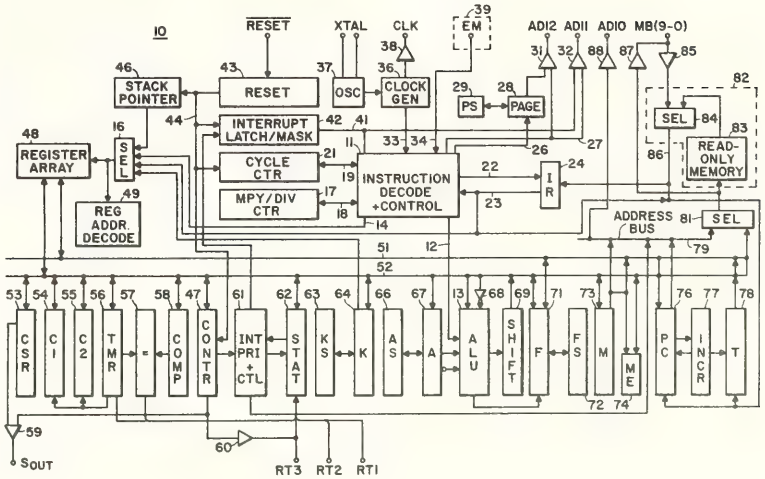
4,142,680	3/1979	Oswald et al.	235/92 T

Primary Examiner—Leo H. Boudreau
Attorney, Agent, or Firm—Walter W. Nielsen

[57] **ABSTRACT**

A microprocessor is disclosed which includes a timer and one or more capture registers. The timer is a counter which is incremented continuously at a fixed clock rate for providing a real time reference. Each capture register is loaded directly from the timer output when a triggering signal appears on a specific input pin, thus recording the time of the occurrence of the triggering signal without interrupt or software intervention.

13 Claims, 26 Drawing Figures



United States Patent [19]

Groves

[11] **4,222,116**

[45] **Sep. 9, 1980**

[54] **DIGITAL LOGIC FOR SEPARATING DATA AND CLOCK IN MANCHESTER-ENCODED DATA**

[75] Inventor: **Stanley E. Groves**, Round Rock, Tex.

[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **939,744**

[22] Filed: **Sep. 5, 1978**

[51] **Int. Cl.**[3] **H04L 7/02**

[52] **U.S. Cl.** **375/55**; 375/110; 364/900

[58] **Field of Search** ..... 178/67, 68, 69.1; 325/30, 38 R, 40, 141, 163, 150, 320, 321; 340/146.1 D

[56] **References Cited**

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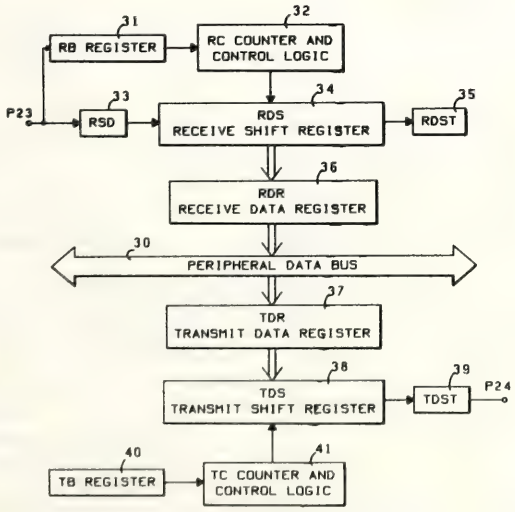
Primary Examiner—Benedict V. Safourek
Assistant Examiner—David Y. Eng
Attorney, Agent, or Firm—Walter W. Nielsen

[57] **ABSTRACT**

A single-chip microcomputer comprises a CPU (1), a RAM (2), a ROM (3), a timer (4), serial I/O communication logic (5), and four I/O ports (11–14).

The serial I/O communication logic includes a shift register (RBA-RBH, FIG. 8J) to separate the data and clock signals in a Manchester-encoded data stream. The Manchester encoding is adaptable to any data rate simply by changing the frequency of a high speed clock associated with the shift register.

4 Claims, 32 Drawing Figures



United States Patent [19]

Hepworth et al.

[11] **4,225,917**

[45] **Sep. 30, 1980**

[54] **ERROR DRIVEN INTERRUPT FOR POLLED MPU SYSTEMS**

[75] Inventors: **Edward C. Hepworth**, Austin, Tex.; **Rodney J. Means**, Tempe, Ariz.

[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **655,366**

[22] Filed: **Feb. 5, 1976**

[51] **Int. Cl.**[3] **G06F 3/04**

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** ..... 340/172.5, 147 LP; 364/200 MS File, 900 MS File

[56] **References Cited**

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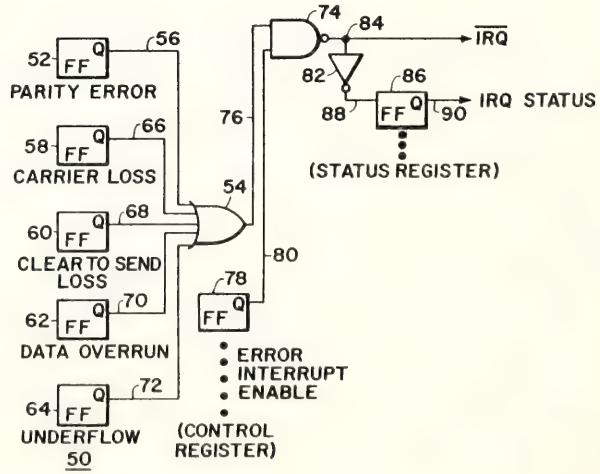
4,047,159	9/1977	Boudry	364/200
4,048,481	9/1977	Bailey, Jr. et al.	364/200

Primary Examiner—Melvin B. Chapnick
Attorney, Agent, or Firm—Anthony J. Sarli, Jr.

[57] **ABSTRACT**

A data processing system in which a central processor polls one or more peripheral devices to initiate a data transfer or to enable a data transfer. The system includes logic associated with a peripheral device or with an interface device for sensing the occurrence of data handling errors such as parity errors, carrier loss, clear to send loss, data overrun or underflow, and for interrupting the central processor upon such occurrence to avoid polling that peripheral device unnecessarily. A status signal is also generated to inform the processor of the nature of the interrupt, so as to distinguish from, for example, the interrupt of another device which is operative to communicate by means of such interrupt rather than by polling.

8 Claims, 6 Drawing Figures



United States Patent [19]

Kyu et al.

[11] **4,225,919**

[45] **Sep. 30, 1980**

[54] **ADVANCED DATA LINK CONTROLLER**

[75] Inventors: **Shikun Kyu**, Yokohama, Japan; **Edward C. Hepworth**, Chattanooga, Tenn.

[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **921,012**

[22] Filed: **Jun. 30, 1978** (Under 37 CFR 1.47)

[51] **Int. Cl.**[3] **G06F 3/04**

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** ..... 179/15 AF, 15 AL; 364/200 MS File, 900 MS File

[56] **References Cited**

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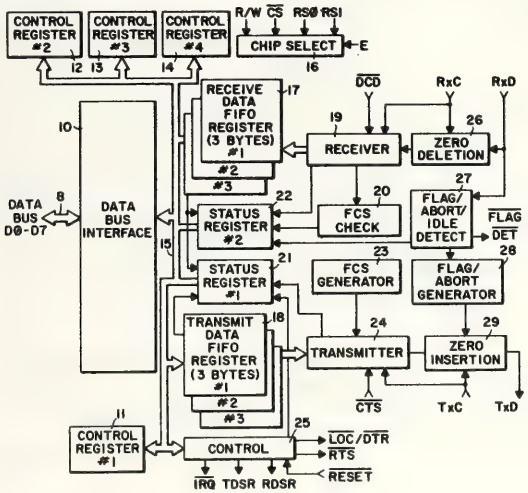
4,034,346	7/1977	Hostein	364/200
4,045,613	8/1977	Walker	179/15 AF
4,151,373	4/1979	Widmer et al.	179/15 AF

Primary Examiner—Harvey E. Springborn
Attorney, Agent, or Firm—Walter W. Nielsen

[57] **ABSTRACT**

A bit-oriented data link controller provides the interface between a microcomputer or terminal and a data communications link. The data link controller is capable of accommodating the three most commonly available bit-oriented data link control protocols, namely Synchronous Data Link Control SDLC, High Level Data Link Control HDLC, and Advanced Data Communications Control Procedure ADCCP. The data link controller provides the data communications interface for both primary and secondary stations in stand-alone, polling, and loop configurations.

7 Claims, 89 Drawing Figures



United States Patent [19]

Wagner et al.

[11] **4,184,200**

[45] **Jan. 15, 1980**

[54] **INTEGRATING I/O ELEMENT**

[75] Inventors: **Richard J. Wagner**, West St. Paul; **Robert A. Melberg**, Bloomington, both of Minn.

[73] Assignee: **Sperry Rand Corporation**, New York, N.Y.

[21] Appl. No.: **899,908**

[22] Filed: **Apr. 26, 1978**

[51] **Int. Cl.**[2] **G06F 1/00**

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** ... 364/200 MS File, 900 MS File

[56] **References Cited**

U.S. PATENT DOCUMENTS

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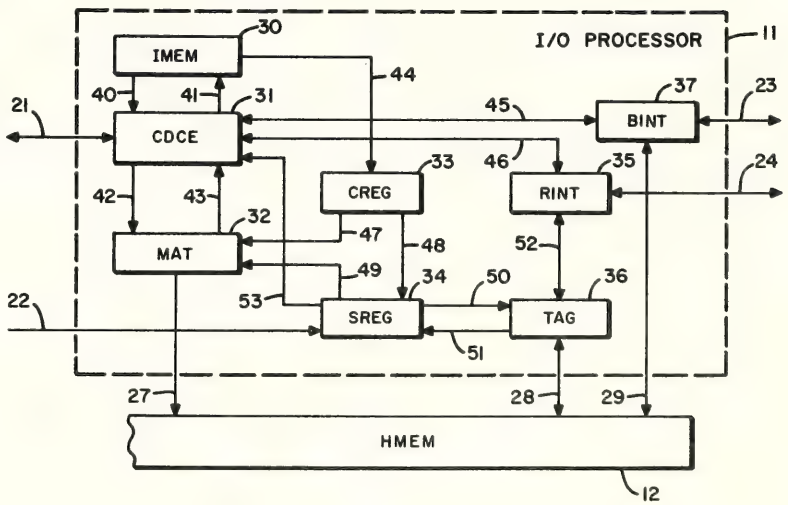
4,034,339	7/1977	Free et al.	364/900

Primary Examiner—Gareth D. Shaw
Assistant Examiner—C. T. Bartz
Attorney, Agent, or Firm—John L. Rooney; Kenneth T. Grace; Marshall M. Truex

[57] **ABSTRACT**

An integrating Input/Output (I/O) element containing an I/O processor that provides a computer with those functions normally associated with an I/O processor (or I/O controller) but which possesses architectural features to prevent compromise (i.e., unauthorized dissemination) of data in a multi-level secure environment. The I/O processor is programmable via an internal instruction memory which cannot be altered by the I/O processor and which cannot be accessed by any other portion of the computer (i.e., Central Processor Unit). The instruction memory is segmented providing a separate segment for each I/O channel. The instructions used to control each I/O channel are stored within the segment of instruction memory allocated to that I/O channel. A secondary memory, called the hand-off memory, is a read/write memory accessible by the Central Processor Unit (CPU) as well as the I/O processor. The hand-off memory is also segmented having a separate segment for each level of secure data to be stored within the hand-off memory. Each segment of the hand-off memory contains a subsegment allocated to each I/O channel permitted to handle the level of secure data associated with that segment of the hand-off memory. The control interface between the CPU and the I/O processor permits exchange of control and status information only. Therefore, all data transfers between the CPU and the I/O processor are via the hand-off memory. Because of the segmentation and subsegmentation of the hand-off memory, each such transfer is of a specific level of secure data and for a specific I/O channel.

6 Claims, 11 Drawing Figures



United States Patent [19]

Melberg et al.

[11] **4,184,201**

[45] **Jan. 15, 1980**

[54] **INTEGRATING PROCESSOR ELEMENT**

[75] Inventors: **Robert A. Melberg**, Bloomington; **Richard J. Wagner**, West St. Paul, both of Minn.

[73] Assignee: **Sperry Rand Corporation**, New York, N.Y.

[21] Appl. No.: **899,909**

[22] Filed: **Apr. 26, 1978**

[51] **Int. Cl.**[2] **G06F 1/00**

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** ... 364/200 MS File, 900 MS File

[56] **References Cited**

U.S. PATENT DOCUMENTS

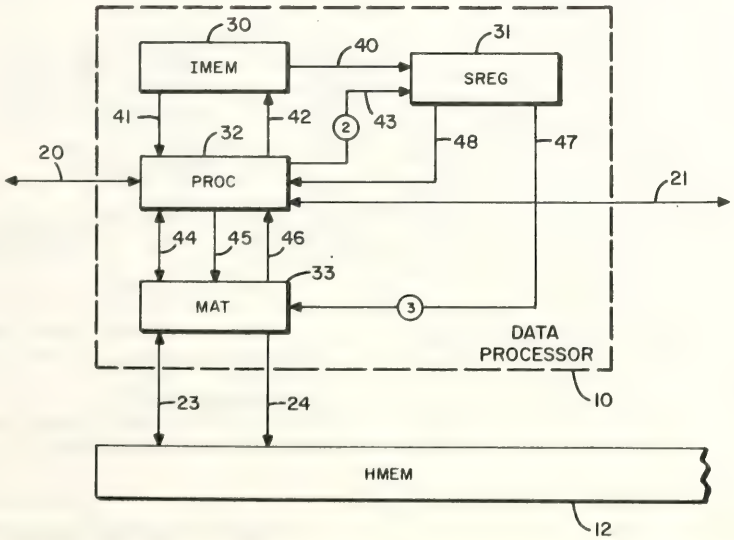
3,609,697	9/1971	Blevins	364/200
4,031,517	6/1977	Hirtle	364/200
4,034,339	7/1977	Free et al.	364/900

Primary Examiner—Gareth D. Shaw
Assistant Examiner—C. T. Bartz
Attorney, Agent, or Firm—John L. Rooney; Kenneth T. Grace; Marshall M. Truex

[57] **ABSTRACT**

An integrating processor element containing a data processor that provides a computer with those functions normally associated with the Central Processor Unit (CPU) but which possesses architectural features to prevent compromise (i.e., unauthorized dissemination) of data in a multi-level secure environment. The data processor executes instructions from an internal instruction memory which cannot be altered by the data processor and cannot be accessed by the I/O processor (i.e., I/O controller). The instruction memory is segmented providing a separate segment for each discrete level of secure data to be processed. Each computer program is stored in the segment corresponding to the highest level of security of the data it will use. A second memory, called the hand-off memory, is a read/write memory accessible by the I/O processor as well as the data processor. The hand-off memory is also segmented by security level. A computer program may only write in the hand-off memory in the segment corresponding to the same security level as the segment in the instruction memory in which it is stored. A computer program may read, however, from any segment corresponding to the same or a lower security level. The data processor contains a security register which provides the hardware assurance that a computer program can access only permitted data. A memory address translator within the data processor is provided to permit relocation of segments within the hand-off memory without corresponding changes to any computer program. This feature enables generation of computer programs having lower classifications than the data upon which they operate.

5 Claims, 7 Drawing Figures



United States Patent [19]

Borgerson et al.

[11] **4,199,811**

[45] **Apr. 22, 1980**

[54] **MICROPROGRAMMABLE COMPUTER UTILIZING CONCURRENTLY OPERATING PROCESSORS**

[75] Inventors: **Barry R. Borgerson**, Gwynedd Valley; **Garold S. Tjaden**, Doylestown, both of Pa.; **Merlin L. Hanson**, Arden Hills, Mich.

[73] Assignee: **Sperry Corporation**, New York, N.Y.

[21] Appl. No.: **830,303**

[22] Filed: **Sep. 2, 1977**

[51] **Int. Cl.**[2] **G06F 9/18**; G06F 9/16; G06F 13/00

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** ..... 364/200 MS File, 736, 364/900 MS File

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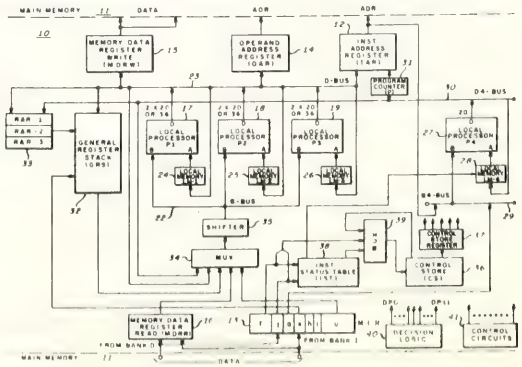
Primary Examiner—Melvin B. Chapnick
Attorney, Agent, or Firm—Howard P. Terry; Albert B. Cooper

[57] **ABSTRACT**

A microprogrammable CPU for a computer utilizes an architecture wherein macro instructions of the computer repertoire are executed by micro instruction routines stored in a control store memory. The micro instruction routines are comprised of micro instruction words for controlling the micro operations to be performed in executing the macro instructions. The CPU includes a plurality of local processors each configured to perform a plurality of the micro operations. A macro instruction fetched into the macro instruction register of the computer addresses the corresponding micro instruction routine in the control store memory and the plurality of local processors operate concurrently to simultaneously perform the micro instructions of the routine on behalf of the fetched macro instruction. Thus a stream of macro instructions flowing through the macro instruction register is decomposed into a plurality of concurrently executed micro instruction streams flowing through the respective local processors. Preferably the local processors are constructed utilizing micro processor LSI integrated circuits. Each local processor is operated in an overlapped mode with respect to micro instruction fetching, execution and storage of results. Each local processor has real and phantom branching capabilities provided by plural next address fields and plural function control fields in the micro instruction words. Decision points provided in the computer select between the next address fields and select between the function control fields to perform the real and phantom branching respectively. The decision points are provided by control logic driven by tables storing functions of plural variables where functions and variables are selectable by the micro instruction words.

65 Claims, 107 Drawing Figures



United States Patent [19]

Seppa

[11] **4,209,846**

[45] **Jun. 24, 1980**

[54] **MEMORY ERROR LOGGER WHICH SORTS TRANSIENT ERRORS FROM SOLID ERRORS**

[75] Inventor: **Dale K. Seppa**, New Brighton, Minn.

[73] Assignee: **Sperry Corporation**, New York, N.Y.

[21] Appl. No.: **856,706**

[22] Filed: **Dec. 2, 1977**

[51] **Int. Cl.**[2] **G06F 11/00**

[52] **U.S. Cl.** **364/900**; 371/38

[58] **Field of Search** ..... 235/312; 364/200 MS File, 900 MS File; 365/201, 200

[56] **References Cited**

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Primary Examiner—Gareth D. Shaw
Assistant Examiner—Thomas Heckler
Attorney, Agent, or Firm—John L. Rooney; Kenneth T. Grace; Marshall M. Truex

[57] **ABSTRACT**

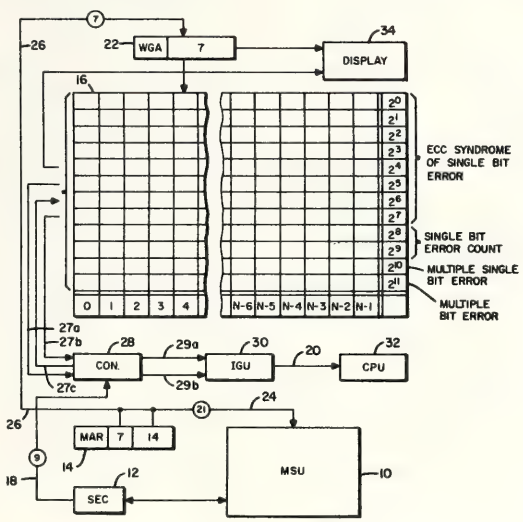
A method of and an apparatus for distinguishing between transient and solid errors within a single-error-correcting semiconductor memory storage unit (MSU) comprised of a plurality of large scale integrated (LSI) bit planes and for notifying the associated data processing system of required maintenance action. The method utilizes an error logging store (ELS) that is comprised of a plurality of memory error registers one for each separately associated word group within the MSU. Each memory error register contains storage for: (1) the Error Correction Code (ECC) defined, failing bit position; (2) the single bit error counter; (3) the multiple single bit error tag; and (4) the multiple bit error tag. Upon detection of an error within a word group, the associated memory error register is accessed to determine the history of previously detected errors within that word group. The central processing unit (CPU) is notified by a priority interrupt of the error status of that word group if:

(1) the number of consecutive errors within a word group at the same bit position reaches a set threshold indicating the high probability of a solid single bit error; or

(2) the error detected is in a different bit position from that previously identified as a solid single bit error indicating the high probability of a future uncorrectable multiple-bit error.

This method and apparatus notifies the CPU of the likelihood of imminent uncorrectable errors and maintains a history of the error indications that lead to that conclusion.

3 Claims, 8 Drawing Figures



United States Patent [19]

Borgerson et al.

[11] **4,210,960**

[45] **Jul. 1, 1980**

[54] **DIGITAL COMPUTER WITH OVERLAPPED OPERATION UTILIZING CONDITIONAL CONTROL TO MINIMIZE TIME LOSSES**

[75] Inventors: **Barry R. Borgerson**, Gwynedd Valley; **Garold S. Tjaden**, Doylestown, both of Pa.; **Merlin L. Hanson**, Arden Hills, Minn.

[73] Assignee: **Sperry Corporation**, New York, N.Y.

[21] Appl. No.: **830,305**

[22] Filed: **Sep. 2, 1977**

[51] **Int. Cl.**[3] **G06F 9/28**; G06F 9/26

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** ... 364/200 MS File, 900 MS File

[56] **References Cited**

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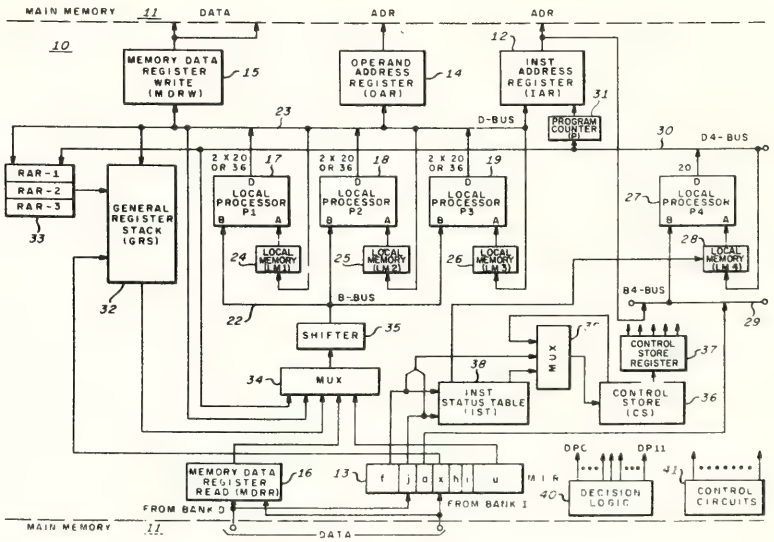
4,038,643	7/1977	Kim	364/200
4,062,058	12/1977	Haynes	364/200
4,070,703	1/1978	Negi	364/200

Primary Examiner—Melvin B. Chapnick
Attorney, Agent, or Firm—Howard P. Terry; Albert B. Cooper

[57] **ABSTRACT**

A computer which is configured to perform its operations in overlapped fashion. During each computer cycle the next instruction is fetched, the function designated by the previous instruction is executed, and values are stored that were computed with respect to the instruction previous to the one being executed. Thus a three-way overlap is effected. To minimize time penalties due to conditional branches and jumps, each instruction word includes two next instruction address fields, two function fields and two deferred action fields. The computer includes decision logic for providing binary decision signals for conditionally selecting one of the fields from each of the next address fields, the function fields and the deferred action fields thereby conditionally fetching the next instruction, conditionally selecting the function to be performed and conditionally storing values during the same cycle in accordance with the decision signals. Thus the computer has the capability of performing conditional branches each cycle, in an unbroken rhythm.

37 Claims, 100 Drawing Figures



United States Patent [19]
Thorsrud
[11] **4,223,382**
[45] **Sep. 16, 1980**

[54] **CLOSED LOOP ERROR CORRECT**

[75] Inventor: **Lee T. Thorsrud,** St. Paul, Minn.
[73] Assignee: **Sperry Corporation,** New York, N.Y.

[21] Appl. No.: **964,993**
[22] Filed: **Nov. 30, 1978**
[51] **Int. Cl.**[2] **G06F 11/00**
[52] **U.S. Cl.** **364/200;** 371/3
[58] **Field of Search** ... 364/200 MS File, 900 MS File; 365/201; 235/302.4

[56] **References Cited**

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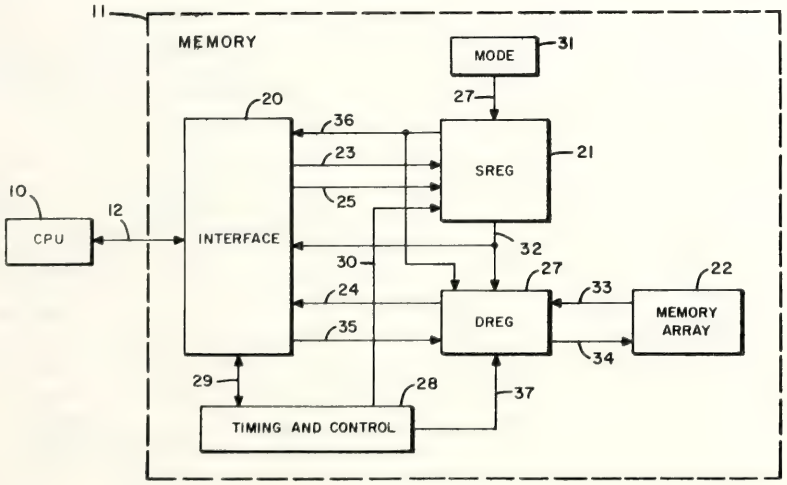
Cooper et al., "Diagnostic Error-Forcing Circuit," *IBM T.D.B.*, vol. 19, No. 5, Oct. 1976.

Primary Examiner—Raulfe B. Zache
Attorney, Agent, or Firm—John L. Rooney; Kenneth T. Grace; Marshall M. Truex

[57] **ABSTRACT**

Apparatus for providing a closed loop data path within a memory module to enable a central processing unit (CPU) to test the error correction circuitry of the memory module under software control without the necessity of accessing the memory arrays within the memory module. The memory module has error correction circuitry providing single bit correction/double bit detection. The error correction circuitry generates an error code which is appended to each data word upon being written into the memory array of the memory module. The error correction circuitry uses the error code to detect and correct errors in each data word read from the memory array of the memory module. A status register within the memory module stores control and status information for communication between the central processing unit and the memory module. Two bit positions of the status register are dedicated to closed loop error correct. If both bit positions contain binary zeroes, the memory module operates normally. If one of the bit positions contains a binary one, a read or write command to the memory module causes a read from or write into temporary storage of the error code within the error correction circuitry. If the other bit position contains a binary one, a read or write command to the memory module causes a read from or write into temporary storage of the memory module rather than a read into or write from the memory array of the memory module. Using the capability to read from and write into the temporary storage of the memory module, a CPU may directly test the error correction circuitry under software control without reading from and writing into the memory array of the memory module.

4 Claims, 13 Drawing Figures



United States Patent [19]
Thorsrud et al.
[11] **4,227,244**
[45] **Oct. 7, 1980**

[54] **CLOSED LOOP ADDRESS**

[75] Inventors: **Lee T. Thorsrud,** St. Paul; **Gary A. Spencer,** Richfield, both of Minn.
[73] Assignee: **Sperry Corporation,** New York, N.Y.

[21] Appl. No.: **964,992**
[22] Filed: **Nov. 30, 1978**
[51] **Int. Cl.**[2] **G06F 11/00;** G11C 29/00
[52] **U.S. Cl.** **364/200;** 371/21; 371/24
[58] **Field of Search** ... 364/200 MS File, 900 MS File; 235/302.3, 312; 365/201; 340/146.1 BA

[56] **References Cited**

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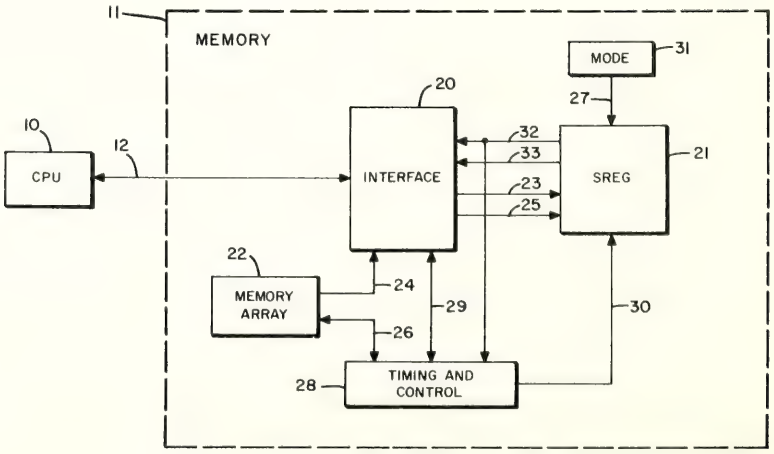
Primary Examiner—Raulfe B. Zache
Attorney, Agent, or Firm—John L. Rooney; Kenneth T. Grace; Marshall M. Truex

[57] **ABSTRACT**

An apparatus for enabling a central processing unit (CPU) to directly read the address transferred to a memory module to permit the CPU to test the address circuitry of the memory module without actually referencing an addressable location of the memory array within the memory module. A status register located within the memory module has two bit positions assigned to controlling the closed loop address capability. If the two assigned bit positions contain binary zeroes, the memory module operates normally by using each address received to address one addressable location of the memory array of the memory module. If one of the assigned bit positions contains a binary one, subsequent read commands cause the memory not to access the memory arrays but to return the portion of the address corresponding to the bit position containing the binary one (i.e., one bit position causes part of the address to be returned whereas the other bit position causes the remainder of the address to be returned) to the requesting CPU as if it were data read from the contents of the specified addressable location, thus permitting the CPU to directly verify the correct operation of the addressing circuitry of the memory module. Since the assigned bit positions of the status register may be easily altered under software control, the closed loop address capability may be rapidly and automatically invoked to periodically verify the correct operation of the addressing circuitry of the memory module.

8 Claims, 13 Drawing Figures



United States Patent [19]
Suzuki et al.
[11] **4,181,938**
[45] **Jan. 1, 1980**

[54] **PROCESSOR DEVICE**

[75] Inventors: **Seigo Suzuki**, Yokohama; **Seiji Eguchi**, Kawasaki, both of Japan

[73] Assignee: **Tokyo Shibaura Electric Co., Ltd.**, Japan

[21] Appl. No.: **849,989**

[22] Filed: **Nov. 9, 1977**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 732,760, Oct. 15, 1976, abandoned.

[30] **Foreign Application Priority Data**

Oct. 15, 1975 [JP] Japan 50-124152

[51] **Int. Cl.**[2] **G06F 13/00**
[52] **U.S. Cl.** **364/200**; 364/900
[58] **Field of Search** ... 364/200 MS File, 900 MS File

[56] **References Cited**

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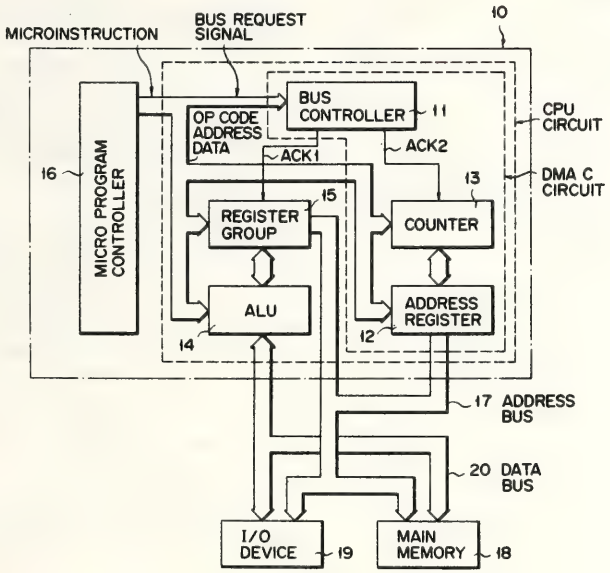
4,067,059	1/1978	Derchak	364/200
4,087,854	5/1978	Kinoshita et al.	364/200

Primary Examiner—Gareth D. Shaw
Assistant Examiner—C. T. Bartz
Attorney, Agent, or Firm—Finnegan, Henderson, Farabow & Garrett

[57] **ABSTRACT**

A processor device which comprises a processor unit integrated in a single chip and integrally assembled with a programming system, thereby providing a direct memory access-controlling function for carrying out a direct memory access between a main memory and an input-output device, and a cycle steal-controlling function for selecting a program mode or direct memory access mode.

8 Claims, 3 Drawing Figures



United States Patent [19]
Sato
[11] **4,183,461**
[45] **Jan. 15, 1980**

[54] **FAULT-DIAGNOSING METHOD FOR AN ELECTRONIC COMPUTER**

[75] Inventor: **Fumitaka Sato**, Oume, Japan

[73] Assignee: **Tokyo Shibaura Electric Co., Ltd.**, Japan

[21] Appl. No.: **886,901**

[22] Filed: **Mar. 14, 1978**

[30] **Foreign Application Priority Data**

Mar. 14, 1977 [JP] Japan 52-27109

[51] **Int. Cl.**[2] **G06F 11/06**
[52] **U.S. Cl.** **235/304**; 364/200
[58] **Field of Search** 235/303, 304, 304.1; 364/200

[56] **References Cited**

U.S. PATENT DOCUMENTS

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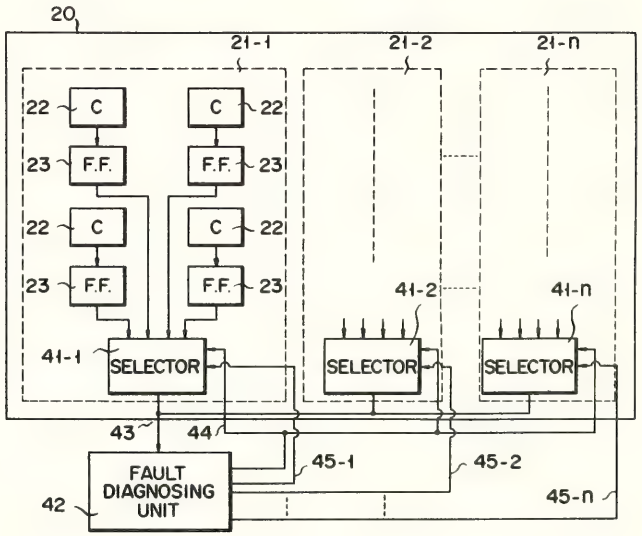
3,999,053	12/1976	Dalmasso	364/200 X

Primary Examiner—Jerry Smith
Attorney, Agent, or Firm—Finnegan, Henderson, Farabow & Garrett

[57] **ABSTRACT**

A fault-diagnosing apparatus and method for an electronic computer designed to diagnose a fault occurring in constituent circuits formed of a plurality of packages according to a signal denoting the status of a sequential circuit in the selected one of the packages, which comprises a fault-diagnosing unit for diagnosing a fault occurring in any of the sequential circuits; an exclusively fault-diagnosing circuit provided in the respective packages; and a common exclusively fault-diagnosing bus to which the output terminals of said exclusively fault-diagnosing circuits are jointly connected, and wherein the exclusively fault-diagnosing circuit sends forth to the exclusively fault-diagnosing bus signals denoting the interior status of the sequential circuit included in the package selected by the fault-diagnosing unit; and the fault-diagnosing unit diagnoses a fault occurring in any of said sequential circuits from the signal received through the bus.

10 Claims, 10 Drawing Figures



United States Patent [19]

Sato et al.

[11] **4,212,059**

[45] **Jul. 8, 1980**

[54] **INFORMATION PROCESSING SYSTEM**

[75] Inventors: **Fumitaka Sato**, Oume; **Masahiko Iwane**, Tokyo; **Masaki Murayama**, Fussa, all of Japan

[73] Assignee: **Tokyo Shibaura Electric Co., Ltd.**, Japan

[21] Appl. No.: **886,598**

[22] Filed: **Mar. 14, 1978**

[30] **Foreign Application Priority Data**

Mar. 14, 1977	[JP]	Japan	52-27788
Mar. 15, 1977	[JP]	Japan	52-28428
Mar. 15, 1977	[JP]	Japan	52-28429

[51] **Int. Cl.**[2] **G06F 11/00**

[52] **U.S. Cl.** **364/200**; 371/18

[58] **Field of Search** ... 364/200 MS File, 900 MS File; 235/304, 304.1

[56] **References Cited**

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Kanada et al., *Fujitsu*, vol. 27, No. 4, Jun. 10, 1976.

M6800 Microprocessor Application Manual, 1975, pp. 5–113.

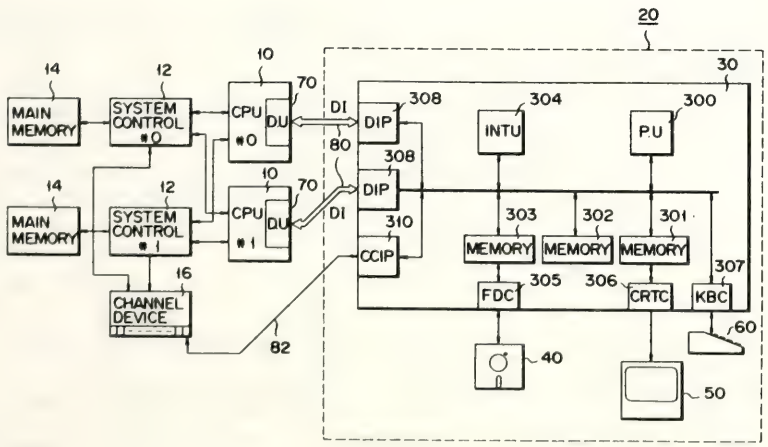
Primary Examiner—Raulfe B. Zache

Attorney, Agent, or Firm—Finnegan, Henderson, Farabow, Garrett & Dunner

[57] **ABSTRACT**

An information processing system includes an information processing unit and an operation console. The information processing unit includes a CPU having a fault diagnostic unit which is coupled with the diagnostic interface port of the operation console, through a diagnostic interface. The operation console is provided with a microprocessor having a first operation mode carrying out at least a normal operation processing function and a second mode executing both a maintenance command processing function and a normal operation processing function, and with a memory for storing a maintenance command processing routine for executing the maintenance command processing function. When an operator issues an instruction for shifting the first operation mode to the second operation mode control is transferred to the operation console so that the microprocessor executes the maintenance command processing function and the normal operation processing function.

21 Claims, 11 Drawing Figures



United States Patent [19]

Denko

[11] **4,215,400**

[45] **Jul. 29, 1980**

[54] **DISK ADDRESS CONTROLLER**

[75] Inventor: **Masatoshi Denko**, Oume, Tokyo, Japan

[73] Assignee: **Tokyo Schibaura Electric Co. Ltd.** Kawasaki, Japan

[21] Appl. No.: **850,146**

[22] Filed: **Nov. 10, 1977**

[30] **Foreign Application Priority Data**

Nov. 17, 1976 [JP] Japan 51-138174

[51] **Int. Cl.**[2] **G06F 13/04**; G06F 3/06; G06F 7/38

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** ... 364/200 MS File, 900 MS File

[56] **References Cited**

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3,638,195	1/1972	Brender et al.	364/200
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3,710,324	1/1973	Cohen et al. .	
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M6800 Microprocessor Application Manual, Motorola Inc., 1975, p. 5–113 to p. 5–117.

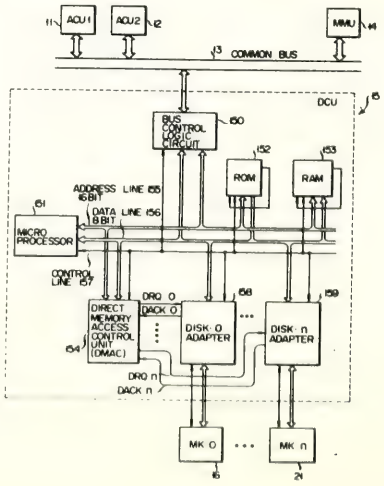
Primary Examiner—Gareth D. Shaw

Assistant Examiner—E. Chan

[57] **ABSTRACT**

A disk address controller includes: a random access memory for storing the upper and lower limit addresses of the access area of each of processing units which are allotted to a disk unit, and storing the disk address specified by a disk input/output instruction from the processing unit; a read only memory for storing a microprogram corresponding to the disk input/output instruction; a microprocessor for executing the microprogram; disk channel units provided corresponding to the respective disk units; and a direct memory access control unit for performing data transfer with the disk unit via the disk channel. The disk address controller sets up the upper and lower addresses of the area arbitrarily allotted to the disk unit by the processing unit. When the real address which is the sum of the lower limit address and the disk address specified by the disk input/output instruction fed from the processing unit to the disk address controller, falls within the access area, the disk input/output instruction in executed by using the real disk address, while the real disk address exists outside the access area, an error interruption is made into the processing unit.

7 Claims, 6 Drawing Figures



United States Patent [19]

Namimoto et al.

[11] **4,217,638**

[45] **Aug. 12, 1980**

[54] **DATA-PROCESSING APPARATUS AND METHOD**

[75] Inventors: **Keiji Namimoto**, Yokohama; **Seiji Eguchi**, Kawasaki; **Yutaka Murao**, Tokyo, all of Japan

[73] Assignee: **Tokyo Shibaura Electric Co., Ltd.**, Japan

[21] Appl. No.: **907,856**

[22] Filed: **May 19, 1978**

[30] **Foreign Application Priority Data**

May 19, 1977 [JP] Japan 52/57100
May 19, 1977 [JP] Japan 52/57101
May 19, 1977 [JP] Japan 52/57102

[51] **Int. Cl.**[2] **G06F 9/18**; G06F 13/00

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** ... 364/200 MS File, 900 MS File

[56] **References Cited**

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3,793,631	2/1974	Silverstein	364/200
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4,087,854	5/1978	Kinoshita	364/200

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"PDP 11/45 Processor Handbook", Digital Equipment Corp., 1971, pp. 9–13.

"Microprocessors and Microcomputers", B. Soucek, 1976, pp. 427–466.

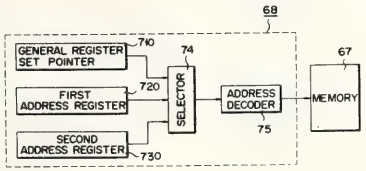
Primary Examiner—James D. Thomas

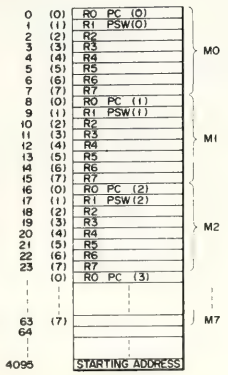
Attorney, Agent, or Firm—Finnegan, Henderson, Farabow, Garrett & Dunner

[57] **ABSTRACT**

The data-processing apparatus of this invention comprises a central processing unit (hereinafter referred to as the "CPU"), and a plurality of groups of memory units in the CPU to be applied as a general register set. The groups of memory units are provided in a number which is equal to the number of interrupt programs and each group has been previously supplied with information on the individual interrupt programs (such information includes, for example, data on entry address, program status word, etc.). The present data-processing apparatus further has a general register-set pointer provided in the CPU. Where the general register set pointer is supplied with a particular numerical value, the corresponding one of the memory unit groups is selectively used as a general register set.

10 Claims, 12 Drawing Figures





United States Patent [19]

Daughton et al.

[11] **4,183,089**

[45] **Jan. 8, 1980**

[54] **DATA COMMUNICATIONS SYSTEM FOR A REPRODUCTION MACHINE HAVING A MASTER AND SECONDARY CONTROLLERS**

[75] Inventors: **John W. Daughton**, Perinton, N.Y.; **Kenneth Gillett**, Redondo Beach; **Frank M. Nelson**, Sherman Oaks, both of Calif.

[73] Assignee: **Xerox Corporation**, Stamford, Conn.

[21] Appl. No.: **829,013**

[22] Filed: **Aug. 30, 1977**

[51] **Int. Cl.**[2] **G06F 3/04**; G06F 9/06; G03G 15/00

[52] **U.S. Cl.** **364/900**; 364/104

[58] **Field of Search** ... 364/900 MS File, 200 MS File, 364/104, 107; 355/14

[56] **References Cited**

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4,016,549	4/1977	Hutner	364/900
4,054,380	10/1977	Donohue et al.	355/14
4,058,850	11/1977	Sheikh	364/900
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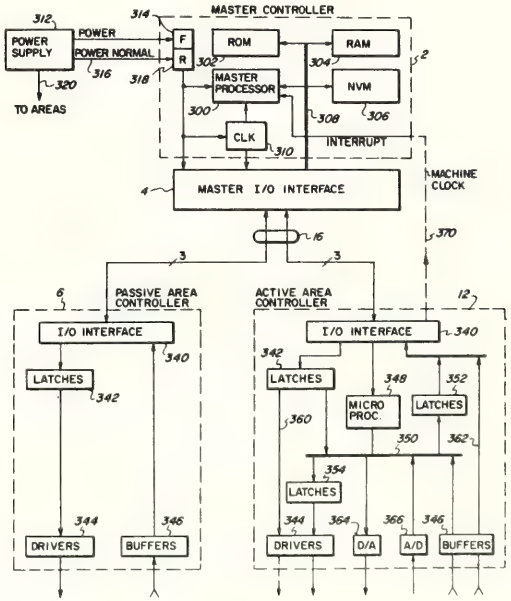
Primary Examiner—Melvin B. Chapnick

[57] **ABSTRACT**

A data communications system for an electrophotographic type reproduction machine or copier. The system includes a programmable master controller with memory and a command byte generator. A plurality of secondary controllers provide input data bytes reflecting the machine status to the master controller and receive command bytes from the master controller for operating the machine components. The secondary controllers are each connected to the master controller such that corresponding data bits of the secondary controller are ORed together to provide simultaneous transmission of input data bytes from the secondary controllers to the master controller while assuring that corresponding bits of the simultaneously transmitted bytes have mutually exclusive data therein.

6 Claims, 71 Drawing Figures



United States Patent [19]

Mager

[11] **4,194,241**

[45] **Mar. 18, 1980**

[54] **BIT MANIPULATION CIRCUITRY IN A MICROPROCESSOR**

[75] Inventor: **George E. Mager**, Manhattan Beach, Calif.

[73] Assignee: **Xerox Corporation**, Stamford, Conn.

[21] Appl. No.: **814,051**

[22] Filed: **Jul. 8, 1977**

[51] **Int. Cl.**[2] **G06F 7/00; G06F 9/08**

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** ... 364/200 MS File, 900 MS File

[56] **References Cited**

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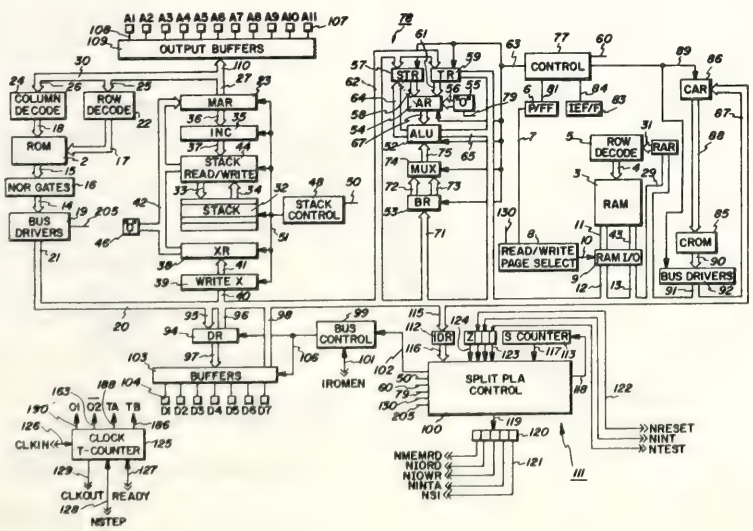
Primary Examiner—Mark E. Nusbaum
Attorney, Agent, or Firm—Ronald L. Taylor

[57] **ABSTRACT**

A method and apparatus for bit manipulation in a digital processor being suitable for executing a plurality of instructions stored in a memory and carried from said memory in accordance with a plurality of machine cycles, each of said instructions including an operational code. A decoder generates a bit mask in response to an operational code. The bit mask generated is in binary digits which are the complement of 2^i where i is the number in base 10 represented by the three least significant bits of the operational code. A register stores the particular bit-mask. An additional register stores a word in which a bit is to be manipulated. Logic circuitry performs one or more logic operations on the output of the registers whereby a desired bit in said word is manipulated. The output of the logic circuitry may be tested and depending on the result, a jump to a particular instruction stored in the memory may be made.

5 Claims, 84 Drawing Figures



United States Patent [19]

Tu et al.

[11] **4,195,352**

[45] **Mar. 25, 1980**

[54] **SPLIT PROGRAMMABLE LOGIC ARRAY**

[75] Inventors: **George K. Tu**, Rolling Hills; **George E. Mager**; **Lamar T. Baker**, both of Manhattan Beach; **Robert E. Markle**, Palos Verdes, all of Calif.

[73] Assignee: **Xerox Corporation**, Stamford, Conn.

[21] Appl. No.: **814,054**

[22] Filed: **Jul. 8, 1977**

[51] **Int. Cl.**[2] **G06F 9/00**; H03K 19/08; H03K 19/34

[52] **U.S. Cl.** **364/900**; 364/716; 307/207

[58] **Field of Search** ... 364/200 MS File, 900 MS File, 364/716; 307/207; 340/166 R; 328/92

[56] **References Cited**

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3,975,623	8/1976	Weinberger	364/716
3,983,538	9/1976	Jones	364/900
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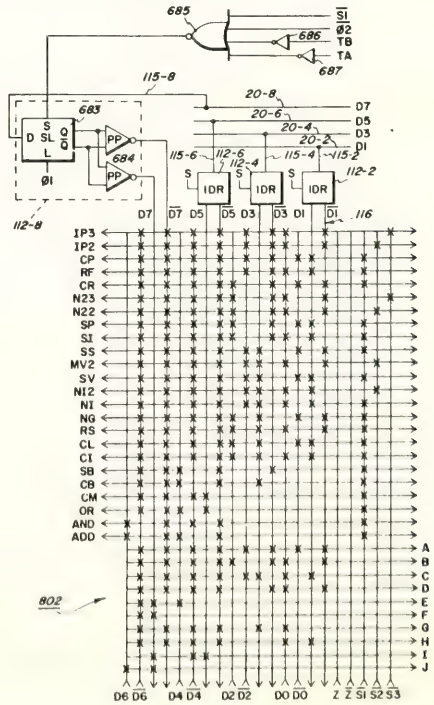
3,987,287	10/1976	Cos et al.	364/716
4,034,356	7/1977	Howley et al.	364/716
4,037,089	7/1977	Horninger	364/900

Primary Examiner—Mark E. Nunsbaum
Attorney, Agent, or Firm—Ronald L. Taylor

[57] **ABSTRACT**

A mask programmable logic array (PLA) for producing a particular digital output given a certain digital input. The input signals to the PLA first pass through a series of AND gates resulting in a predetermined number of product terms being formed. The product signals then pass through a set of OR gates to become the final output signals. In the subject invention, the AND gates and OR gates are implemented through the use of NOR-NOR logic. A first set of NOR gates is implemented in an array to receive input signals and to produce product terms. A second and third set of NOR gates form two arrays. These two arrays are then located on either side of the first array to receive selected product signals in order to produce final output signals. In effect the OR portion of the PLA has been split into two arrays.

4 Claims, 85 Drawing Figures



United States Patent [19]
Steiner
[11] **4,196,476**
[45] **Apr. 1, 1980**

[54] **REPRODUCTION MACHINE WITH SELECTIVELY DISCLOSABLE PROGRAMS**

[75] Inventor: **Edward L. Steiner**, Macedon, N.Y.
[73] Assignee: **Xerox Corporation**, Stamford, Conn.

[21] Appl. No.: **829,017**
[22] Filed: **Aug. 30, 1977**
[51] **Int. Cl.**[2] **G06F 9/06**; G06F 3/00; G03G 15/00
[52] **U.S. Cl.** ..... **364/900**; 355/14 R
[58] **Field of Search** ..... 355/14; 364/200 MS File, 900 MS File

[56] **References Cited**

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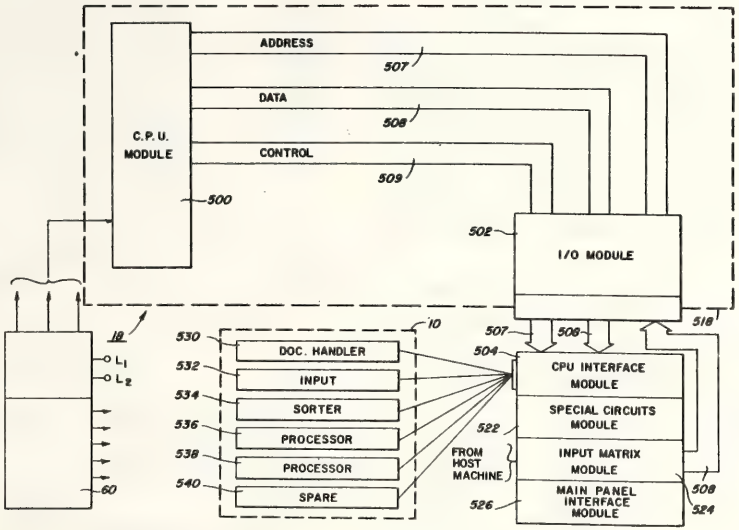
4,035,072	7/1977	Deetz et al.	355/14

Primary Examiner—Harvey E. Springborn
Attorney, Agent, or Firm—John E. Beck; Frederick E. McMullen; Ronald F. Chapuran

[57] **ABSTRACT**

An electrostatographic type copying or reproduction machine incorporating a programmable digital computer to operate various machine components. The computer includes a memory which contains a plurality of different operating programs with each program instructing the machine to operate in a different manner. Provision is made for selectively permitting the user to access the programs of lesser complexity, while providing access to all of the programs to trained service personnel. The service personnel can expand or restrict the number of programs that the user is permitted to use depending on her familiarity with the machine.

12 Claims, 57 Drawing Figures



United States Patent [19]
Heartz
[11] **4,205,389**
[45] **May 27, 1980**

[54] **APPARATUS FOR GENERATING A RASTER IMAGE FROM LINE SEGMENTS**

[75] Inventor: **Robert A. Heartz**, Deland, Fla.
[73] Assignee: **General Electric Company**, Philadelphia, Pa.

[21] Appl. No.: **886,974**
[22] Filed: **Mar. 15, 1978**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 726,304, Sep. 24, 1976, abandoned.

[51] **Int. Cl.**[2] **G06F 3/14**
[52] **U.S. Cl.** **364/900**; 340/744; 340/747; 340/793; 364/521
[58] **Field of Search** ... 364/900 MS File, 200 MS File, 364/521; 35/10.4; 340/324 R, 324 A, 324 AD, 724, 731, 744, 747, 793

[56] **References Cited**

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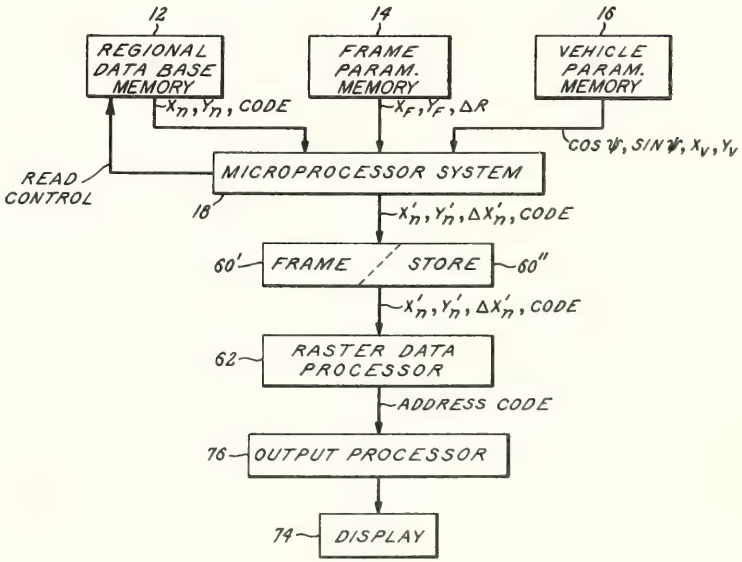
4,023,025	5/1977	Rowe et al.	35/10.4 X

Primary Examiner—Melvin B. Chapnick
Attorney, Agent, or Firm—Allen E. Amgott; Raymond H. Quist

[57] **ABSTRACT**

Apparatus for processing data whereby a digital control signal is generated for effecting the presentation of a selected portion of a map image on a raster display. The data includes stored data words describing characteristics of line segments utilizable to construct the image. The line segments include line vectors representative of elongated features of the image and boundary vectors identifying boundaries between image areas of different brightness. Processing of the data is accomplished by means of two control loops. The first control loop performs selected macrosteps including arithmetic manipulations, on the data words to effect generation of the digital control signal. The second control loop effects selection of the macrosteps to be performed by the first loop and routes the data words within the generator in response to the instant data being processed by the generator. In accordance with an additional feature of the invention, data words are generated for defining intersections to be displayed adjacent each intersection of a line segment with a raster line where the line segment has a slope of less than a predetermined magnitude. These additional intersections prevent the stepped appearance of line segments intersecting raster lines at small angles.

4 Claims, 14 Drawing Figures



United States Patent [19]
Devlin et al.
[11] **4,212,057**
[45] **Jul. 8, 1980**

[54] **SHARED MEMORY MULTI-MICROPROCESSOR COMPUTER SYSTEM**

[75] Inventors: **Charles L. Devlin**, Ballston Lake; **Charles W. Eichelberger**, Schenectady, both of N.Y.

[73] Assignee: **General Electric Company**, Schenectady, N.Y.

[21] Appl. No.: **679,408**

[22] Filed: **Apr. 22, 1976**

[51] **Int. Cl.**[2] **G06F 15/16**; G06F 13/00; G06F 9/18

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** ..... 340/172.5, 147 LP; 445/1; 364/200 MS File, 900 MS File

[56] **References Cited**

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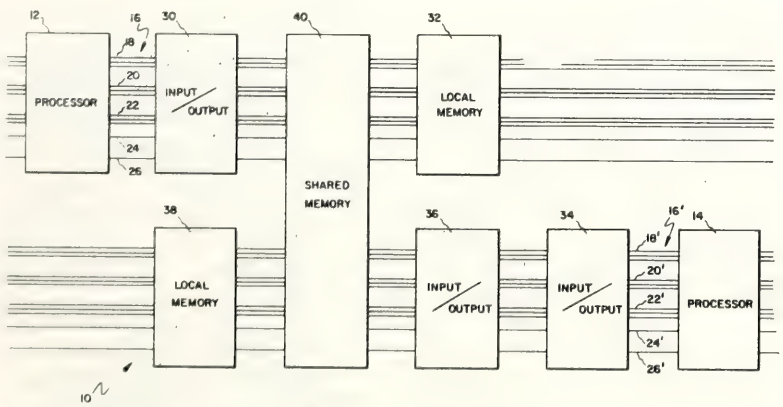
Primary Examiner—Melvin B. Chapnick
Attorney, Agent, or Firm—Geoffrey H. Krauss; James C. Davis; Marvin Snyder

[57] **ABSTRACT**

A multiprocessor microcomputer system having two or more substantially independent processors each of which has its own bus-type interconnection structure, and a shared memory accessible by any of the processors without interferring with the proper operation of the other processors. Controlled access to the memory by connecting the memory to the processor requesting access when only one such request is present and to the last processor to have received access when more than one request is received simultaneously allows autosynchronous operation, automatic selection of priority and high speed of operation.

9 Claims, 4 Drawing Figures



United States Patent [19]
Eichelberger et al.
[11] **4,213,182**
[45] **Jul. 15, 1980**

[54] **PROGRAMMABLE ENERGY LOAD CONTROLLER SYSTEM AND METHODS**

[75] Inventors: **Charles W. Eichelberger; Edward B. Miller**, both of Schenectady, N.Y.

[73] Assignee: **General Electric Company**, Schenectady, N.Y.

[21] Appl. No.: **966,816**

[22] Filed: **Dec. 6, 1978**

Related U.S. Application Data

[63] Continuation of Ser. No. 871,989, Jan. 24, 1978, abandoned.

[51] **Int. Cl.**[2] **G01R 21/00**; G06F 15/06

[52] **U.S. Cl.** ..... **364/493**; 179/2 AM; 315/312; 324/103 R; 364/120; 364/900

[58] **Field of Search** ..... 364/492–494, 364/119, 120, 200, 900, 483; 340/150, 151, 309.1; 324/103 R, 103 P; 179/2 AM; 361/78–82, 84; 315/294, 312–318; 307/38

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Primary Examiner—Errol A. Krass

Attorney, Agent, or Firm—Geoffrey H. Krauss; James C. Davis; Marvin Snyder

[57] **ABSTRACT**

A programmable energy load controller system, allowing each of a multiplicity of energy loads to be established in a selected one of an unenergized condition and a plurality of energized conditions, utilizes a central microcomputer facility in communication with a selected one of a plurality of remotely located load control processors, each configured with a unique address and capable of selectively energizing a plurality of energy loads coupled thereto under control of the central facility. The central facility includes at least one user input device, allowing a plurality of maps of load conditions, established in accordance with a user-selectable criteria, such as time-of-day and day-of-week requirements, to be loaded into a data storage associated with the central computer. A real time clock means are utilized in association with the computer and the memory to enable the desired map of load energization under the selected criteria, with means being provided for entering, on a high priority basis, overrides to at least a selected portion of the map currently implemented. Programmable energy load control methods are also disclosed.

43 Claims, 31 Drawing Figures

United States Patent [19]

Olander, Jr. et al.

[11] **4,181,965**

[45] **Jan. 1, 1980**

[54] **PROGRAMMABLE CALCULATOR INCLUDING PROGRAM TRACE MEANS**

[75] Inventors: **Emil E. Olander, Jr.**, Fort Collins; **Rex L. James**, Loveland; **Ivar W. Larson**, Loveland; **Wayne F. Covington**, Loveland; **Jack M. Walden**, Loveland; **Robert E. Watson**, Loveland; **Francis J. Yockey**, Loveland; **Fred Wenninger, Jr.**, Loveland; **Homer C. Russell**, Berthoud, all of Colo.

[73] Assignee: **Hewlett-Packard Company**, Palo Alto, Calif.

[21] Appl. No.: **802,832**

[22] Filed: **Jun. 1, 1977**

Related U.S. Application Data

[62] Division of Ser. No. 510,921, Sep. 30, 1974, Pat. No. 4,028,538, which is a division of Ser. No. 212,581, Dec. 27, 1971, Pat. No. 3,839,630.

[51] **Int. Cl.**[2] **G06F 3/12**

[52] **U.S. Cl.** **364/710**; 364/200

[58] **Field of Search** 364/710, 709, 706, 200, 364/900

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,760,171	9/1973	Wang et al.	364/710 X
3,859,635	1/1975	Watson et al.	364/200

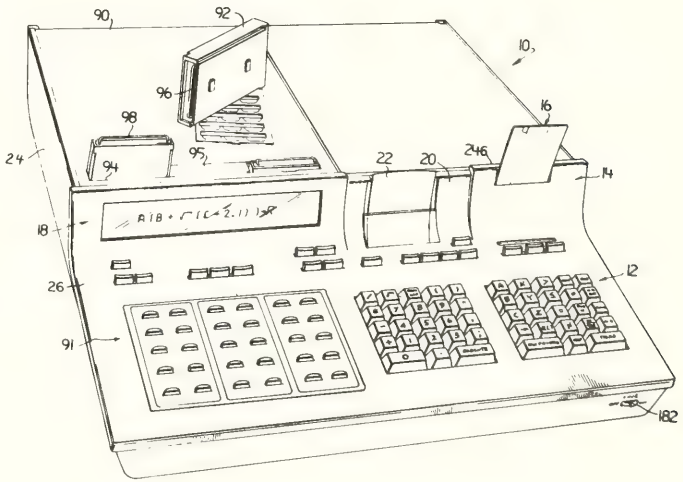
Primary Examiner—David H. Malzahn

Attorney, Agent, or Firm—William E. Hein

[57] **ABSTRACT**

An adaptable programmable calculator is provided by employing modular read-write and read-only memory units capable of being expanded to provide the calculator with additional program and data storage functions, a central processing unit, and an input-output control unit capable of bidirectionally transferring information between the memory or central processing units and a number of input and output units. The memory, central processing, and input-output control units are controlled by a microprocessor included in the central processing unit. The input and output units include a keyboard input unit, a magnetic card reading and recording unit, a solid state multi-character display unit capable of displaying every alphabetic and numeric character and many other symbols individually and in a line of one or more alphameric statements, and an alphameric printer unit. The calculator includes a TRACE key that permits the user to manually or programmably obtain an alphameric print-out of the number of each line of alphameric statements executed by the calculator and the value of each numeric assignment made therein. The calculator includes a NORMAL key for permitting the user to manually or programmably terminate a previously established TRACE mode of operation. An alphameric listing of each line of one or more alphameric statements, as that line is being executed by the calculator or stored as part of a program in the calculator read-write memory, may be obtained when the calculator is operating in the TRACE mode.

8 Claims, 4 Drawing Figures



United States Patent [19]
Olander, Jr. et al.
[11] **4,187,547**
[45] **Feb. 5, 1980**

[54] **PROGRAMMABLE CALCULATOR INCLUDING MEANS FOR CONTROLLABLY INTRODUCING BLANK LINES ON A PRINTED RECORD DURING PROGRAM EXECUTION**

[75] Inventors: **Emil E. Olander, Jr.**, Fort Collins; **Rex L. James**, Loveland; **Ivar W. Larson**, Loveland; **Wayne F. Covington**, Loveland; **Jack M. Walden**, Loveland; **Robert E. Watson**, Loveland; **Francis J. Yockey**, Loveland; **Fred Wenninger, Jr.**, Loveland; **Homer C. Russell**, Berthoud, all of Colo.

[73] Assignee: **Hewlett-Packard Company**, Palo Alto, Calif.

[21] Appl. No.: **802,322**

[22] Filed: **Jun. 1, 1977**

Related U.S. Application Data

[62] Division of Ser. No. 510,921, Sep. 30, 1974, Pat. No. 4,028,538, which is a division of Ser. No. 212,581, Dec. 27, 1971, Pat. No. 3,839,630.

[51] **Int. Cl.**[2] **G06F 3/12**
[52] **U.S. Cl.** **364/710**; 364/200
[58] **Field of Search** 364/710, 706, 200, 900

[56] **References Cited**

U.S. PATENT DOCUMENTS

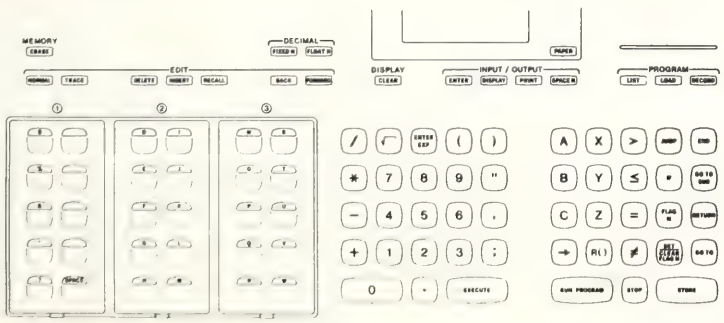
3,859,635	1/1975	Watson et al.	364/200
3,996,562	12/1976	Reach et al.	364/900

Primary Examiner—David H. Malzahn
Attorney, Agent, or Firm—William E. Hein

[57] **ABSTRACT**

An adaptable programmable calculator is provided by employing modular read-write and read-only memory units capable of being expanded to provide the calculator with additional program and data storage functions oriented towards the environment of the user, a central processing unit, and an input-output control unit capable of bidirectionally transferring information between the memory or central processing units and a number of input and output units. The memory, central processor, and input-output control units are controlled by a microprocessor included in the central processing unit. The input and output units include a keyboard input unit with a plurality of sections capable of being defined by plug-in read-only memory modules and stored programs added by the user, a magnetic card reading and recording unit capable of bidirectionally transferring information between an external magnetic card and the calculator, a solid state output display unit capable of displaying every alphabetic and numeric character and many other symbols individually and in a line of one or more alphameric statements, and a line printer capable of printing on thermally sensitive paper every alphabetic and numeric character and many other symbols individually and in alphameric statements or messages. A printer spacing control command that may be executed either from the keyboard input unit or under control of a program stored in the read-write memory unit enables the user to introduce a blank space between printed lines on the paper, the blank space being equal to the number of lines specified in the printer spacing control command.

5 Claims, 4 Drawing Figures



United States Patent [19]
Watson et al.
[11] **4,203,152**
[45] **May 13, 1980**

[54] **PROGRAMMABLE CALCULATOR INCLUDING KEY-LOG PRINTING MEANS**

[75] Inventors: **Robert E. Watson; Jack M. Walden; Charles W. Near**, all of Loveland, Colo.

[73] Assignee: **Hewlett-Packard Company**, Palo Alto, Calif.

[21] Appl. No.: **850,332**

[22] Filed: **Nov. 10, 1977**

Related U.S. Application Data

[62] Division of Ser. No. 535,750, Dec. 23, 1974, which is a division of Ser. No. 153,437, Jun. 15, 1971, Pat. No. 3,859,635.

[51] **Int. Cl.**[2] **G06F 3/12**; G06F 3/02
[52] **U.S. Cl.** **364/200**; 364/710
[58] **Field of Search** ... 364/200 MS File, 900 MS File, 364/300, 710, 706, 709

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,593,313	7/1971	Tomaszewski et al.	364/200
3,623,012	11/1971	Lowry et al.	364/200
3,744,031	7/1973	Avery et al.	364/200
3,760,171	9/1973	Wang et al.	364/706

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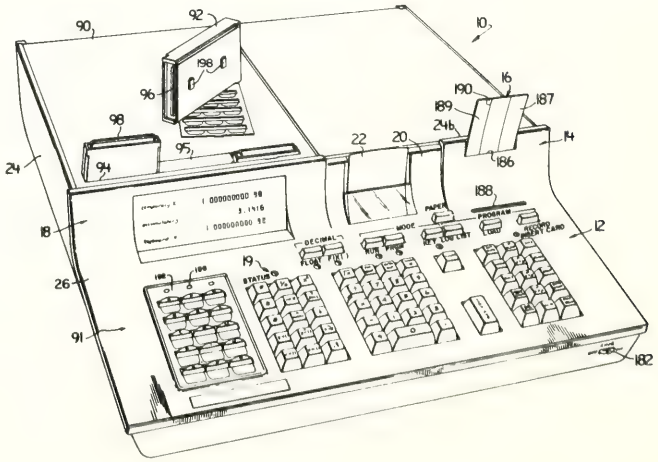
Programmer's Guide to the IBM System/360, Bradley, 1969, pp. 246–255, 294–297.

Primary Examiner—Mark E. Nusbaum
Attorney, Agent, or Firm—F. D. LaRiviere

[57] **ABSTRACT**

The modular read-write and read-only memory, central processing, input-output control keyboard input and output printer units of the calculator described herein provide an adaptable programmable calculator that may be operated manually by the user from the keyboard input unit or automatically by a program stored in memory. Programs may be loaded directly into memory from the keyboard and either data or programs may be separately transferred bi-directionally between the memory unit and an external magnetic card. Programs stored in the memory unit may be edited and key-coded logs, program lists, labels, and messages may be printed by the output printer unit by specifying one of several modes of the calculator. In one of the modes, the printer will print a log comprising a listing of a key code for each key actuated, of nearly all programmable operations performed from the keyboard.

13 Claims, 3 Drawing Figures



200

United States Patent [19]
Giraud
[11] **4,215,421**
[45] **Jul. 29, 1980**

[54] **DATA-PROCESSING SYSTEM WHICH PROTECTS THE SECRECY OF CONFIDENTIAL DATA**

[75] Inventor: **Georges J. L. Giraud**, Le Vesinet, France

[73] Assignee: **Compagnie Internationale pour l'Informatique CII-Honeywell Bull (Societe Anonyme)**, Paris, France

[21] Appl. No.: **912,855**

[22] Filed: **Jun. 5, 1978**

[30] **Foreign Application Priority Data**

Jun. 7, 1977 [FR] France 77 17436

[51] **Int. Cl.**[2] **G06F 1/00**; H04L 9/02; G08B 29/00

[52] **U.S. Cl.** ..... **364/900**; 178/22; 340/149 A

[58] **Field of Search** ... 364/200 MS File, 900 MS File; 340/149 R, 149 A; 178/22; 179/2 DP, 2 CA

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,764,742	10/1973	Abbott et al.	340/149 A X
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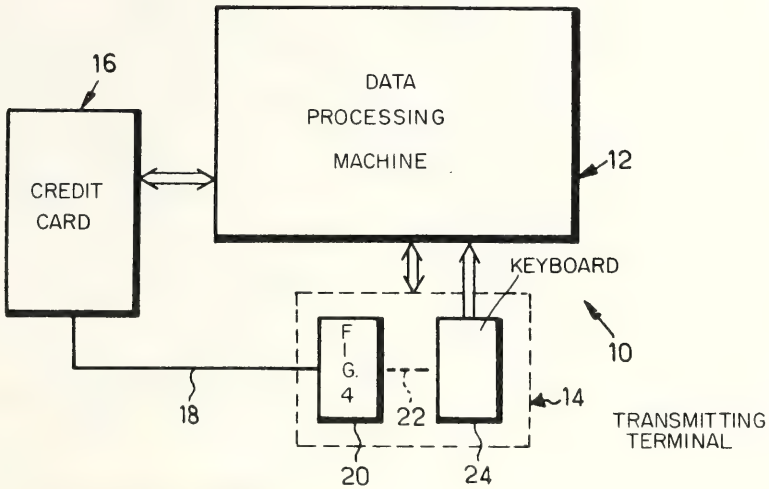
3,962,539	6/1976	Ehrsam et al.	178/22
3,984,637	10/1976	Caudill et al.	340/149 R X

Primary Examiner—Raulfe B. Zache
Attorney, Agent, or Firm—Kerkam, Stowell, Kondracki & Clarke

[57] **ABSTRACT**

A data processing system is provided which protects the secrecy of confidential data at the stages where it is formulated and transmitted to a card (first auxiliary member) having a code key thereon. The data processing system includes a data-processing machine having a device or terminal for transmitting data, including confidential data, and a plurality of first members auxiliary to the machine which are each intended to receive the confidential data from the transmitting device via the same transmission line and to process this confidential data. The transmitting device includes a plurality of second auxiliary members which correspond to respective ones of the first auxiliary members. Each pair of corresponding first and second auxiliary members include respective generators for generating first and second code keys and the system includes a means for causing one of the first code keys to correspond with one of the second code keys. One of the pair of corresponding first and second members includes modulating means to mix the confidential data with the code key corresponding to the said members of that pair to form a combined signal, while the corresponding members of the other pair include a demodulating means which reacts to the code key which has been made to correspond and to the said combined signal to reconstitute the said confidential data.

15 Claims, 14 Drawing Figures



United States Patent [19]
Lemaire et al.
[11] **4,223,392**
[45] **Sep. 16, 1980**

[54] **CLOCK-SIGNAL GENERATOR FOR A DATA-PROCESSING SYSTEM**

[75] Inventors: **Francis Lemaire; Pierre Salkazanov**, both of Plaisir; **Robert Bavoux**, Rueil-Malmaison, all of France

[73] Assignee: **Compagnie Internationale pour l'Informatique Cii-Honeywell Bull**, Paris, France

[21] Appl. No.: **873,845**

[22] Filed: **Jan. 31, 1978**

[30] **Foreign Application Priority Data**

Feb. 7, 1977 [FR] France 77 03316

[51] **Int. Cl.**[2] **G06M 3/02**; H03K 3/00; G06F 1/04

[52] **U.S. Cl.** **364/900**; 328/63; 307/269

[58] **Field of Search** ... 364/200 MS File, 900 MS File; 235/92 SH, 92 PE, 92 ST; 328/37, 63, 72; 307/269, 260

[56] **References Cited**

U.S. PATENT DOCUMENTS

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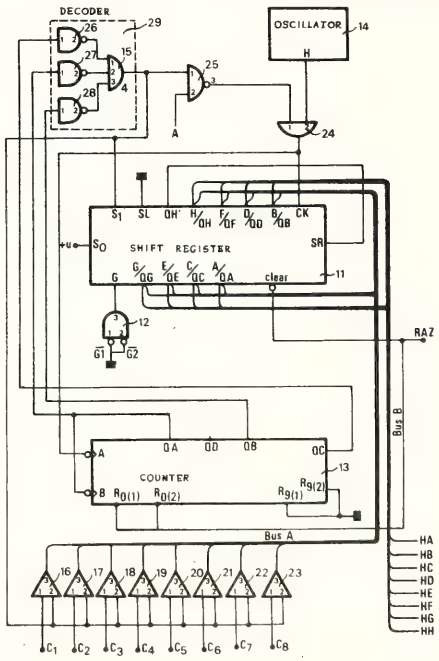
3,691,531	9/1972	Saltini et al.	364/200
3,949,199	4/1976	Odour	235/92 SH
3,971,920	7/1976	Johnson	235/92 SH

Primary Examiner—Gareth D. Shaw
Assistant Examiner—E. Chan
Attorney, Agent, or Firm—Lowe, King, Price and Becker

[57] **ABSTRACT**

A plurality of sub-clock signals are derived from a main clock signal source by advancing a shift register and a counter with pulses from the main clock source. The shift register is selectively loaded with a desired combination of sub-clock bits in response to a predetermined number of main clock pulses being supplied to the counter. The sub-clock signals are derived from output terminals at different stages of the shift register. The state of the sub-clock signals can be selectively frozen by decoupling pulses from the main clock source to inputs of the counter and shift register.

8 Claims, 2 Drawing Figures



United States Patent [19]

Giraud

[11] **4,224,666**

[45] **Sep. 23, 1980**

[54] **DATA PROCESSING SYSTEM WHICH PROTECTS THE SECRECY OF CONFIDENTIAL DATA**

[75] Inventor: **Georges J. L. Giraud**, Le Vesinet, France

[73] Assignee: **Compagnie Internationale pour l'Informatique Cii-Honeywell Bull**, Paris, France

[21] Appl. No.: **900,503**

[22] Filed: **Apr. 27, 1978**

[30] **Foreign Application Priority Data**

Apr. 27, 1977 [FR] France 77 12781

[51] **Int. Cl.**[2] **G06F 3/00**

[52] **U.S. Cl.** **364/200**; 235/380; 235/487

[58] **Field of Search** ..... 235/379, 380, 382, 487; 340/149 A; 364/200 MS File, 900 MS File

[56] **References Cited**

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4,001,550	1/1977	Schatz	235/379
4,016,405	4/1977	McCune et al.	235/380
4,138,057	2/1979	Atalla	235/487

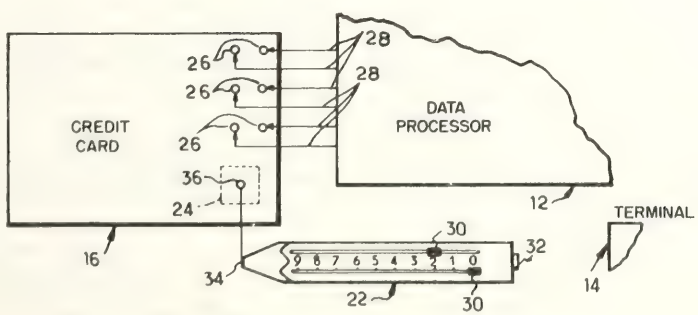
Primary Examiner—Leo H. Boudreau

Attorney, Agent, or Firm—Kerkam, Stowell, Kondracki & Clarke

[57] **ABSTRACT**

A data processing system is provided which protects the secrecy of confidential data transmitted between a transmitting terminal and key, such as a credit card, which is used to authorize a dialogue between a data processing machine and an operator. A light pen is provided which is personal to each operator and which includes means for formulating the confidential data in a predetermined code and transmitting the coded information by means of an information carrying light wave. The light pen includes a keyboard which may be in the form of cursors movable along a longitudinal graduated scale which sets the coded data in accordance with the position of the cursors. To this end, the light pen houses an encoder, the output of which is fed to a shift register. The output of the shift register is modulated and fed to an optical-electrical transducer system which is screened to prevent unauthorized detection. The credit card receives the coded information through its own electrical transducer. The information is demodulated, and fed to a register, the output of which is compared to information stored in a memory contained in an integrated circuit chip which forms part of the card. A control responsive to the output of the comparator authorizes the dialogue to take place.

18 Claims, 9 Drawing Figures



United States Patent [19]

Carmody

[11] **4,191,998**

[45] **Mar. 4, 1980**

[54] **VARIABLE SYMMETRY MULTIPHASE CLOCK GENERATOR**

[75] Inventor: **Joseph P. Carmody**, Willow Grove, Pa.

[73] Assignee: **Honeywell Inc.**, Minneapolis, Minn.

[21] Appl. No.: **891,076**

[22] Filed: **Mar. 29, 1978**

[51] **Int. Cl.**[2] **G06F 1/04**

[52] **U.S. Cl.** **364/200**; 328/62; 307/269

[58] **Field of Search** ... 364/200 MS File, 900 MS File, 364/701; 307/221 R, 265, 267, 269; 328/62

[56] **References Cited**

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Primary Examiner—Mark E. Nusbaum

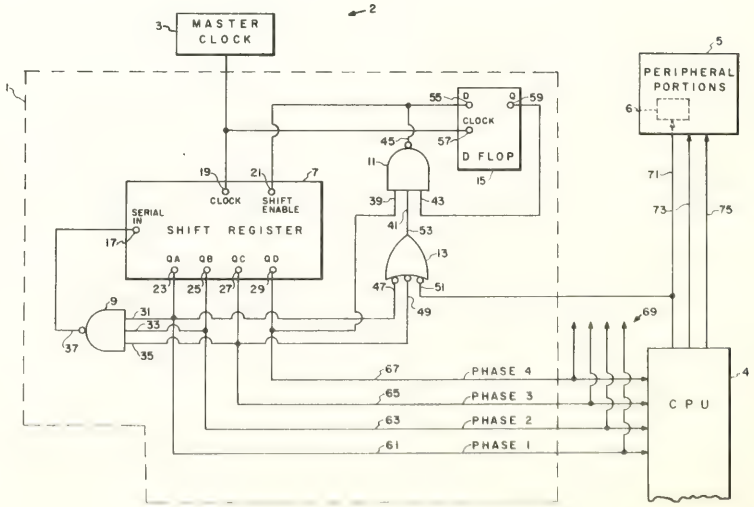
Assistant Examiner—Thomas M. Heckler

Attorney, Agent, or Firm—Laurence J. Marhoefer; Lockwood D. Burton

[57] **ABSTRACT**

The clock generator, which is shown as being a part of a data processor, includes a recirculating shift register and gate combination for deriving a set of four clock phase signals from a master clock signal. The generator also includes two gates and a D flop which form sequential circuitry. The latter controls the shift register to impart a desired nonsymmetry to the clock signals, and to vary that symmetry, as necessary to minimize the clock cycle time and to maximize the processor operating speed. To this end, the circuitry normally makes the clock pulse widths a minimum, consistent with the processor requirements, and, on demand, doubles the widths of only those clock pulses which are actually timing the slowest processor portion, thereby lengthening only those specific clock cycles which contain the demanded widened clock pulses.

14 Claims, 2 Drawing Figures



United States Patent [19]
Templeton
[11] **4,219,875**
[45] **Aug. 26, 1980**

[54] **DIGITAL EVENT INPUT CIRCUIT FOR A COMPUTER BASED PROCESS CONTROL SYSTEM**

[75] Inventor: **Steven R. Templeton**, Phoenix, Ariz.
[73] Assignee: **Honeywell Inc.**, Minneapolis, Minn.

[21] Appl. No.: **903,103**
[22] Filed: **May 5, 1978**
[51] **Int. Cl.**[2] **G06F 11/06**; G06F 15/46
[52] **U.S. Cl.** **364/200**; 364/554
[58] **Field of Search** ... 364/200 MS File, 900 MS File, 364/552, 554; 235/92 CA, 92 ST; 340/183

[56] **References Cited**

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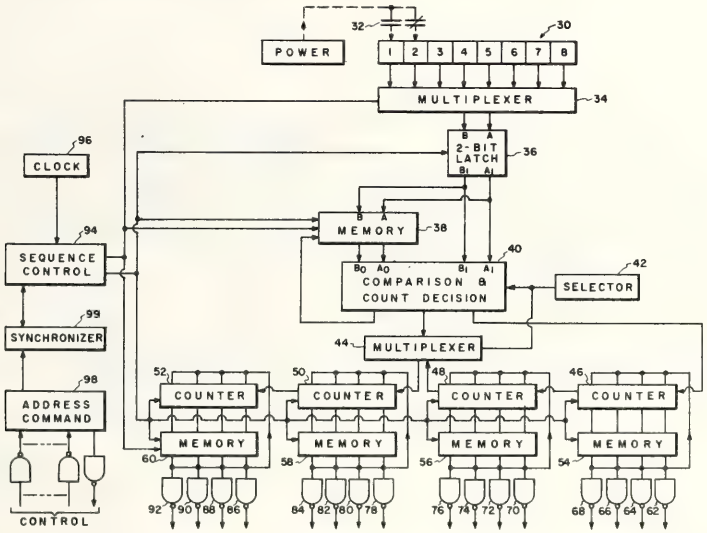
4,057,847	11/1977	Lowell et al.	364/200

Primary Examiner—Gareth D. Shaw
Assistant Examiner—E. Chan
Attorney, Agent, or Firm—L. J. Marhoefer; L. D. Burton

[57] **ABSTRACT**

A computer based process control system includes a digital event counter input circuit wherein a number of data sources are scanned. A sensed status of the individual input point is compared with the previous status of that point to determine if a change of status has occurred, indicative of an event to be counted. The previous status is stored in a dedicated register. If the comparison indicates that a countable event has occurred, a counter is incremented; also the dedicated register is updated to indicate the present status of the scanned point. The counter status is stored in an accompanying memory which may then be read out by an external device such as a processor.

7 Claims, 7 Drawing Figures



United States Patent [19]
Wilske
[11] **4,219,881**
[45] **Aug. 26, 1980**

[54] **DIGITAL INPUT CONTROL CIRCUIT**

[75] Inventor: **Lowell D. Wilske**, Phoenix, Ariz.
[73] Assignee: **Honeywell Inc.**, Minneapolis, Minn.

[21] Appl. No.: **866,000**
[22] Filed: **Dec. 30, 1977**
[51] **Int. Cl.**[3] **G06F 11/00**
[52] **U.S. Cl.** **364/900**
[58] **Field of Search** ... 364/200 MS File, 900 MS File, 364/119, 552, 105

[56] **References Cited**

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3,916,170	10/1975	Norimatsu et al.	364/105
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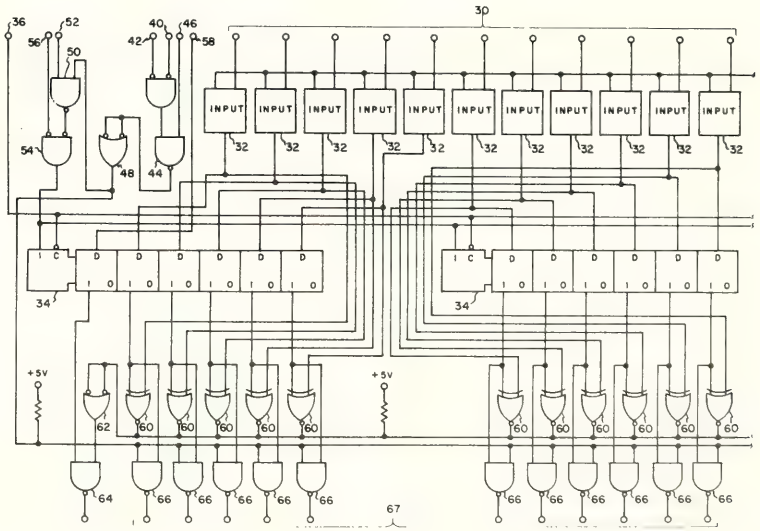
4,070,702	1/1978	Grants et al.	364/200
4,115,847	9/1978	Osder et al.	364/119
4,117,317	9/1978	Dooley, Jr. et al.	364/119

Primary Examiner—Gareth D. Shaw
Assistant Examiner—C. T. Bartz
Attorney, Agent, or Firm—L. J. Marhoefer; L. D. Burton

[57] **ABSTRACT**

A digital input circuit is provided wherein previous digital data is stored in a holding register. Subsequent data is compared with the data in the holding register to determine whether or not a change had occurred in the input data from the primary sensors. If no change is detected, the system effectively "passes" on that scan of the data. If, on the other hand, a change has been detected an interrupt signal is generated for transmission back to the host computer. The host computer may then initiate a "read" sequence. The "read" sequence under ordinary circumstances, includes updating the data in the storage register before enabling the outputting of the digital data.

5 Claims, 5 Drawing Figures



United States Patent [19]
Kober

[11] **4,183,086**
[45] **Jan. 8, 1980**

[54] **COMPUTER SYSTEM HAVING INDIVIDUAL COMPUTERS WITH DATA FILTERS**

[75] Inventor: **Rudolf Kober**, Munich, Fed. Rep. of Germany

[73] Assignee: **Siemens Aktiengesellschaft**, Berlin & Munich, Fed. Rep. of Germany

[21] Appl. No.: **870,756**

[22] Filed: **Jan. 9, 1978**

[30] **Foreign Application Priority Data**

Jan. 28, 1977 [DE] Fed. Rep. of Germany 2703559

[51] **Int. Cl.**[2] **G06F 15/16**; G06F 13/00
[52] **U.S. Cl.** **364/200**
[58] **Field of Search** ... 364/200 MS File, 900 MS File

[56] **References Cited**

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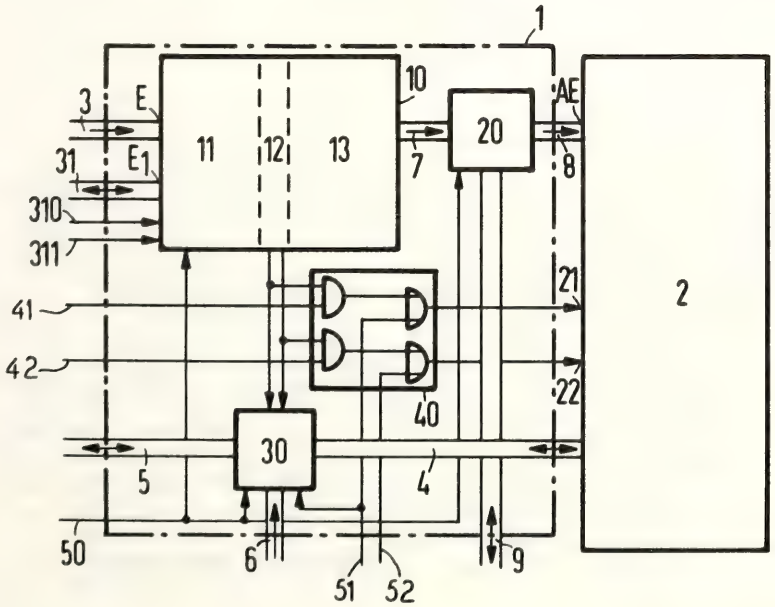
3,967,247	6/1976	Andersen	364/200

Primary Examiner—James D. Thomas
Attorney, Agent, or Firm—Hill, Van Santen, Steadman, Chiara & Simpson

[57] **ABSTRACT**

A computer system which is made up of a number of individual computers and which has a system bus for transmitting data among the individual computers, has a data filter interposed between the system bus and the individual computers which allows communication between the system bus and one of the individual computers only when that computer is being accessed.

9 Claims, 3 Drawing Figures



United States Patent [19]
Stark et al.

[11] **4,215,413**
[45] **Jul. 29, 1980**

[54] **MEASURING DEVICE FOR INTEGRAL VALUES FORMED OVER A TIME SPAN**

[75] Inventors: **Reinhard Stark; Günter Steinmüller**, both of Nuremberg, Fed. Rep. of Germany

[73] Assignee: **Siemens Aktiengesellschaft**, Munich, Fed. Rep. of Germany

[21] Appl. No.: **920,253**

[22] Filed: **Jun. 29, 1978**

[30] **Foreign Application Priority Data**

Jun. 30, 1977 [DE] Fed. Rep. of Germany 2729617

[51] **Int. Cl.**[2] **G06M 3/14**; G01F 1/00
[52] **U.S. Cl.** ..... **364/570**; 235/92 DP; 364/510; 364/734; 364/900
[58] **Field of Search** ..... 364/509, 510, 570, 728, 364/900, 442, 556, 561, 565, 734, 200; 235/92 DP, 92 FQ; 324/160, 161, 178; 307/220 R, 221 R; 179/156

[56] **References Cited**

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4,086,470	4/1978	Ashbee	235/92 DP
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FOREIGN PATENT DOCUMENTS

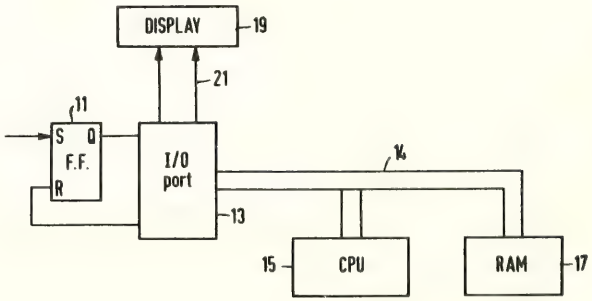
2446602 4/1976 Fed. Rep. of Germany .

Primary Examiner—Errol A. Krass
Attorney, Agent, or Firm—Kenyon & Kenyon

[57] **ABSTRACT**

In a measuring device for integral values formed over a time span which is constantly up-dated, the system being one in which pulses represent a fixed quantity of the value being measured, the pulses are stored in a random access memory of a microcomputer with the central processing unit of the microcomputer sequentially addressing individual memory cells, in a repetitive manner after each sweep of the time span.

2 Claims, 3 Drawing Figures



United States Patent [19]
Kober et al.
[11] **4,219,873**
[45] **Aug. 26, 1980**

[54] **PROCESS FOR CONTROLLING OPERATION OF AND DATA EXCHANGE BETWEEN A PLURALITY OF INDIVIDUAL COMPUTERS WITH A CONTROL COMPUTER**

[75] Inventors: **Rudolf Kober**, Munich; **Herbert Kopp**, Sauerlach; **Christian Kuznia**, Munich, all of Fed. Rep. of Germany

[73] Assignee: **Siemens Aktiengesellschaft**, Berlin & Munich, Fed. Rep. of Germany

[21] Appl. No.: **732,988**

[22] Filed: **Oct. 15, 1976**

[30] **Foreign Application Priority Data**

Oct. 15, 1975 [DE] Fed. Rep. of Germany 2546202

[51] **Int. Cl.**[2] **G06F 15/16**
[52] **U.S. Cl.** **364/200**
[58] **Field of Search** ..... 364/200 MS File

[56] **References Cited**

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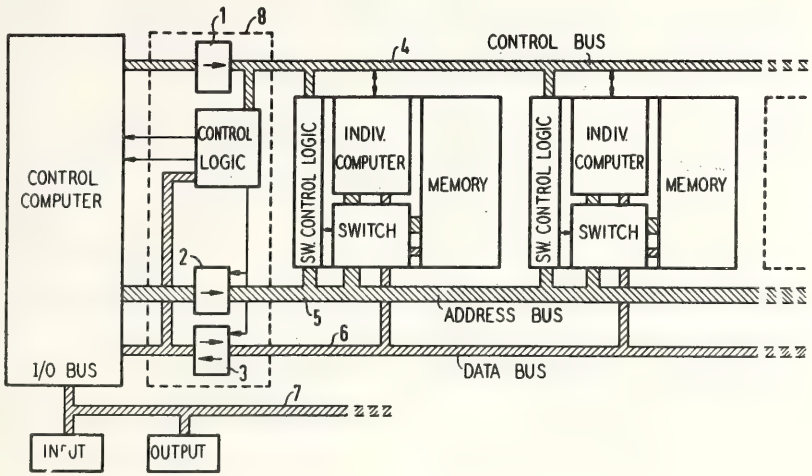
3,593,300	7/1971	Driscoll, Jr.	364/200
3,618,045	11/1971	Campbell	364/200
3,905,023	9/1975	Perpiglia	364/200

Primary Examiner—James D. Thomas
Attorney, Agent, or Firm—Hill, Van Santen, Steadman, Chiara & Simpson

[57] **ABSTRACT**

A computer system comprises a control or supervisory computer and a plurality of individual computers which are connected to and cooperate with each other under control of a process which establishes a three phase operation. In a control phase only the control computer operates, executes its program and informs the individual computers which function they must carry out during the next phase, the autonomous phase. In the autonomous phase the individual computers simultaneously and independently fulfill their assigned functions and report completion thereof to the control computer. Finally, a communication phase is utilized for a data exchange between the computers.

3 Claims, 21 Drawing Figures



United States Patent [19]
Struger et al.
[11] **4,200,915**
[45] **Apr. 29, 1980**

[54] **PROGRAM LOADER FOR PROGRAMMABLE CONTROLLER**

[75] Inventors: **Odo J. Struger**, Chagrin Falls; **Valdis Grants**, Lyndhurst; **Raymond A. Grudowski**, South Euclid, all of Ohio

[73] Assignee: **Allen-Bradley Company**, Milwaukee, Wis.

[21] Appl. No.: **893,252**

[22] Filed: **Apr. 5, 1978**

[51] **Int. Cl.**[2] **G06F 9/00**
[52] **U.S. Cl.** **364/900**; 364/101
[58] **Field of Search** ..... 364/101, 107, 115, 120, 364/200 MS File, 900 MS File

[56] **References Cited**

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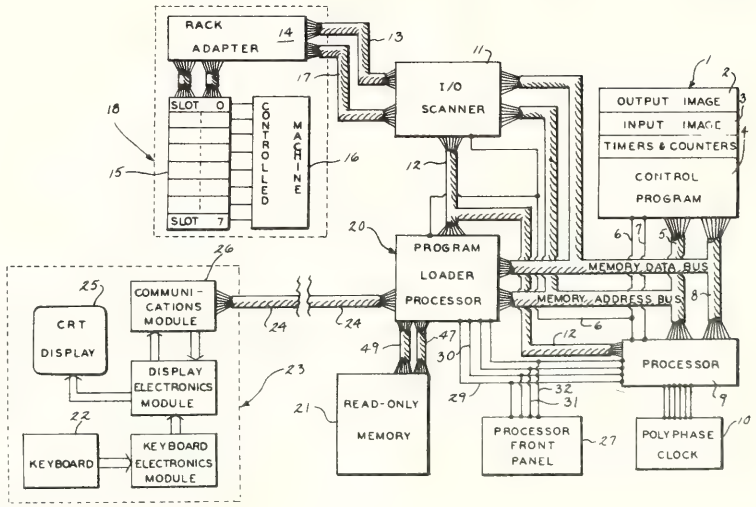
4,003,033	11/1977	O'Keefe et al.	364/200
4,034,354	7/1977	Simmons	364/900

Primary Examiner—Mark E. Nusbaum
Assistant Examiner—E. Chan
Attorney, Agent, or Firm—Quarles & Brady

[57] **ABSTRACT**

A microprocessor based program loader is connected to the memory data bus and memory address bus of a programmable controller. The program loader is responsive to commands entered through a keyboard to load and edit the programmable controller control program. A mode switch associated with the programmable controller provides a number of selectable positions which determine the mode of operation of the programmable controller and the functions that can be performed by the program loader. One of the positions on this mode switch enables the program loader through a control line to assume control of the mode selection. The operator can thus control the mode of operation through the program loader keyboard which may be located remotely from the programmable controller.

11 Claims, 10 Drawing Figures



United States Patent [19]

Bernhard et al.

[11] **4,228,495**

[45] **Oct. 14, 1980**

[54] **MULTIPROCESSOR NUMERICAL CONTROL SYSTEM**

[75] Inventors: **Theodore L. Bernhard**, Mentor on the Lake; **Ernst Dummermuth**, Chesterland; **Thomas M. Hoch**, Woodmere; **Bruce S. Jaffe**, Mayfield Heights; **Gregory L. Merrell**, Cleveland Heights, all of Ohio

[73] Assignee: **Allen-Bradley Company**, Milwaukee, Wis.

[21] Appl. No.: **970,959**

[22] Filed: **Dec. 19, 1978**

[51] **Int. Cl.**[3] **G05B 19/18**; G06F 15/16

[52] **U.S. Cl.** **364/101**; 364/200; 364/474

[58] **Field of Search** ..... 364/104, 107, 474, 101, 364/102, 200 MS File, 900 MS File

[56] **References Cited**

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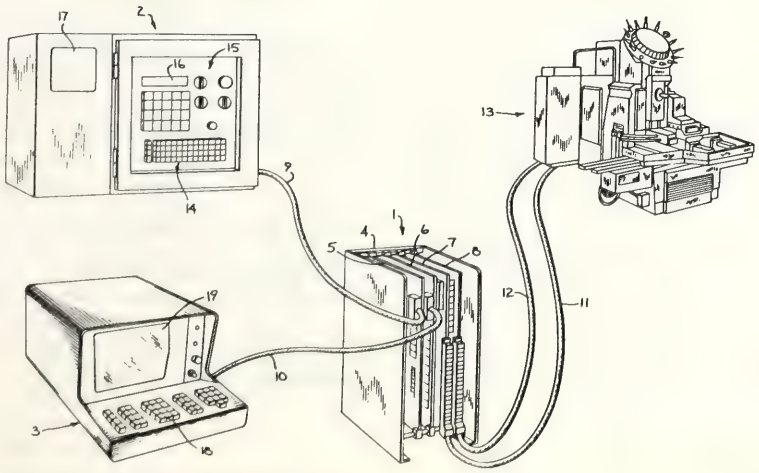
Primary Examiner—Joseph F. Ruggiero

Attorney, Agent, or Firm—Quarles & Brady

[57] **ABSTRACT**

A numerical control system includes a main processor which performs such functions as interpolation and outputting of motion command signals to the servomechanisms on a machine tool. A separate programmable interface processor connects to the main processor bus structure and it operates as a programmable controller to control the discrete digital I/O devices associated with the machine tool. A third processor couples through a serial data link with the main processor and it operates to service peripheral I/O devices associated with the front control panel on the numerical control system.

26 Claims, 44 Drawing Figures



United States Patent [19]

Ahuja

[11] **4,189,767**

[45] **Feb. 19, 1980**

[54] **ACCESSING ARRANGEMENT FOR INTERLEAVED MODULAR MEMORIES**

[75] Inventor: **Sudhir R. Ahuja**, Matawan, N.J.

[73] Assignee: **Bell Telephone Laboratories, Incorporated**, Murray Hill, N.J.

[21] Appl. No.: **912,369**

[22] Filed: **Jun. 5, 1978**

[51] **Int. Cl.**[2] **G06F 13/00**; G06F 7/38; G11C 8/00

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** ... 364/200 MS File, 900 MS File, 364/746, 715

[56] **References Cited**

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4,124,893	11/1978	Joyce et al.	364/200

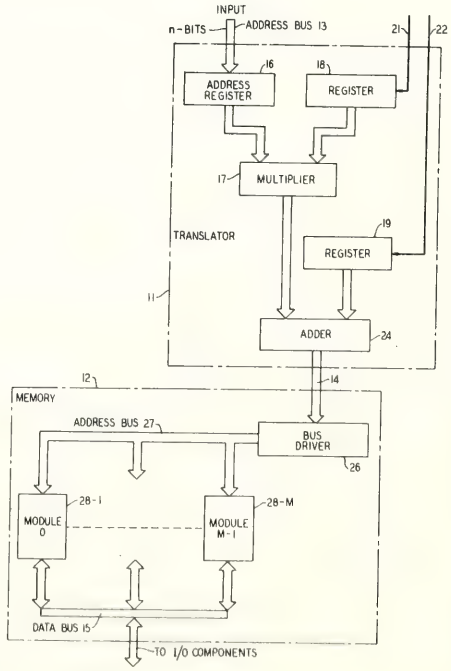
Primary Examiner—Melvin B. Chapnick

Attorney, Agent, or Firm—John F. Moran

[57] **ABSTRACT**

An address translator, which is designated to operate in a fraction of the memory cycle time, and associated modular organized memory accepts logical addresses and converts each to a corresponding physical address. Each physical address uniquely identifies a particular module and a particular storage location therein for data transfer. The overall structure is adaptable for full utilization of a variable number of modules occasioned by failure thereby providing a soft fail feature. The access time provided by the address translator and associated modules remains constant independent of the storage location being used. Adaption for accommodating changes in the number of modules is provided by altering the parameters of the address translation and changing the identification constants associated with each module.

10 Claims, 6 Drawing Figures



United States Patent [19]

Hunsberger et al.

[11] **4,231,087**

[45] **Oct. 28, 1980**

[54] **MICROPROCESSOR SUPPORT SYSTEM**

[75] Inventors: **Dennis J. Hunsberger**, Fair Haven; **Charles E. Nahabedian**, Mendham; **Thomas M. Quinn**, Little Silver; **James H. VanOrnum**, Hazlet, all of N.J.

[73] Assignee: **Bell Telephone Laboratories, Incorporated**, Murray Hill, N.J.

[21] Appl. No.: **952,278**

[22] Filed: **Oct. 18, 1978**

[51] **Int. Cl.**[3] **G06F 11/00**

[52] **U.S. Cl.** **364/200**; 364/900; 371/16

[58] **Field of Search** 364/200, 900; 235/302, 235/304, 304.1, 304.2; 371/15, 16, 19

[56] **References Cited**

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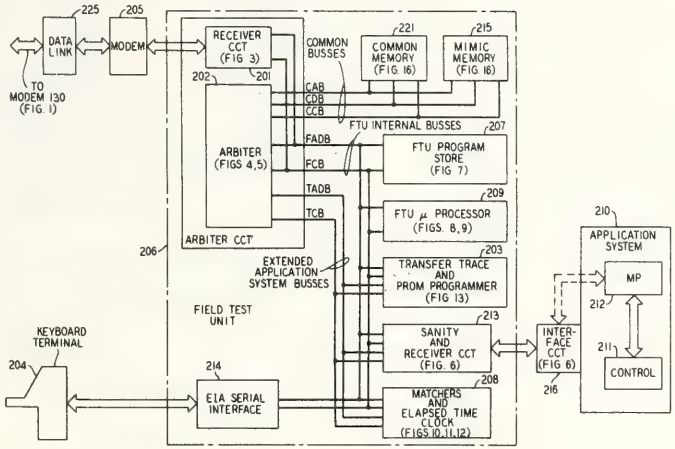
Primary Examiner—Charles E. Atkinson
Attorney, Agent, or Firm—James M. Graziano

[57] **ABSTRACT**

The disclosed microprocessor support system provides a total "laboratory" environment for developing and testing application software as well as for debugging the microprocessor-based application machine itself. The microprocessor support system contains a time shared minicomputer equipped with a full set of peripherals which functions as the main or operating system. A data link connects this operating system with test equipment located at the site of the application machine. This test equipment consists of a field test unit which provides an interface between the application machine, a local keyboard terminal and the operating system such that an engineer at the site of the application machine has access through the field test unit to both the microprocessor-based application machine and the operating system with its sophisticated hardware and software resources to assist in developing and testing application software, as well as debugging the application machine itself.

18 Claims, 23 Drawing Figures



United States Patent [19]

Rawlings et al.

[11] **4,200,930**

[45] **Apr. 29, 1980**

[54] **ADAPTER CLUSTER MODULE FOR DATA COMMUNICATIONS SUBSYSTEM**

[75] Inventors: **Robert L. Rawlings**, El Toro; **Ronald D. Mathews**, Mission Viejo, both of Calif.

[73] Assignee: **Burroughs Corporation**, Detroit, Mich.

[21] Appl. No.: **932,698**

[22] Filed: **Aug. 10, 1978**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 799,265, May 23, 1977, abandoned.

[51] **Int. Cl.**[2] **G06F 3/04**

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** ..... 364/200 MS

[56] **References Cited**

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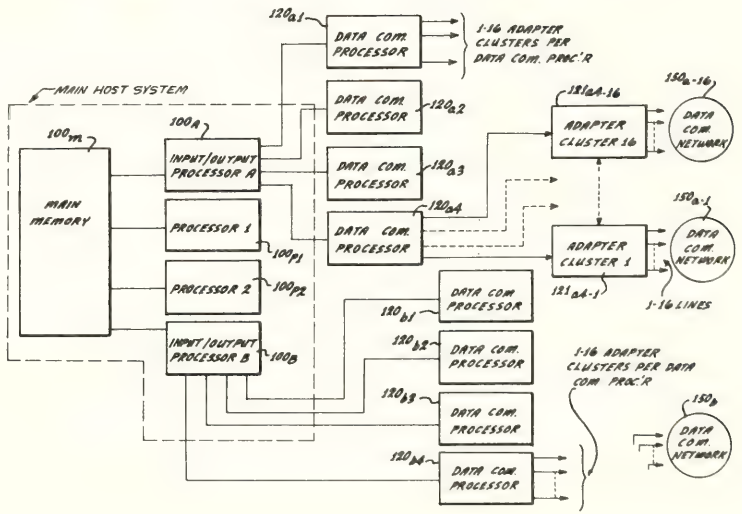
Primary Examiner—Harvey E. Springborn
Attorney, Agent, or Firm—Alfred W. Kozak; Nathan Cass; Kevin R. Peterson

[57] **ABSTRACT**

In a digital data communication network there is provided a data communications subsystem working in conjunction with a main host system having a central host processor and main memory. The data communications subsystem provides a data communications processor and a local autonomous data communications memory connected to a basic control interface unit which supports a plurality of front-end controllers. The data communications subsystem can sense a halt in the main system and operate autonomously and independently of the main host system during such down-time. The present disclosure describes a front-end controller-processor called an adapter cluster module which is used to control a plurality of line adapters, each of which communicates with remote terminals on low to medium speed transmission lines. Up to 16 such adapter cluster modules may be accommodated as front-end controllers within a single data communications subsystem. Each adapter cluster module can handle up to eight transmission lines operating in full duplex mode. A ROM memory area is provided for standard program routines. A RAM memory is provided for storage of special routines and instructions in addition to a scratch-pad area for accumulation of a full message block before any interruption is made to the data communications processor requesting further data transfer instructions. Thus, a large magnitude of overhead operations are removed from the data communications processor which formerly was interrupted each time a byte of information was received by the adapter cluster module.

16 Claims, 31 Drawing Figures



United States Patent [19]
Drogichen
[11] **4,218,757**
[45] **Aug. 19, 1980**

[54] **DEVICE FOR AUTOMATIC MODIFICATION OF ROM CONTENTS BY A SYSTEM SELECTED VARIABLE**

[75] Inventor: **Daniel P. Drogichen**, West Chester, Pa.

[73] Assignee: **Burroughs Corporation**, Detroit, Mich.

[21] Appl. No.: **920,557**

[22] Filed: **Jun. 29, 1978**

[51] **Int. Cl.**[2] **G06F 13/00**; G06F 9/20
[52] **U.S. Cl.** **364/900**
[58] **Field of Search** ... 364/900 MS File, 200 MS File; 365/94

[56] **References Cited**

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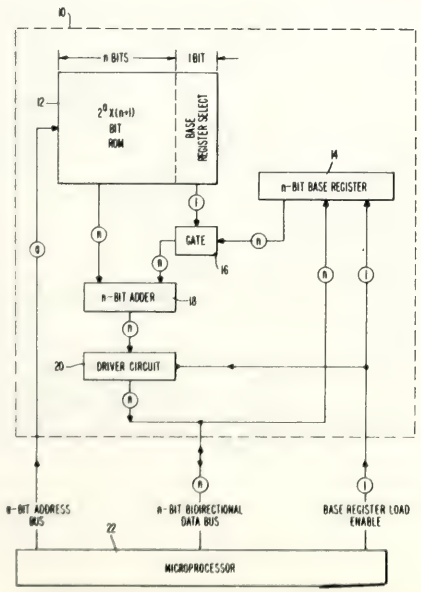
Primary Examiner—Gareth D. Shaw
Assistant Examiner—E. Chan
Attorney, Agent, or Firm—Mark T. Starr

[57] **ABSTRACT**

A device for use with a digital computer for storing standard software used by the computer and modifying the address portions of the standard software prior to transmission to the computer. The device includes a ROM package containing a ROM within which is stored a standard software subprogram written assuming it is stored at an absolute location in the computer's memory other than its actual location in the computer's memory system. Also included in the ROM package is a base register which can be loaded, under control of the operating system software, with an offset value reflecting the difference between the actual starting memory system location of the subprogram stored in the ROM and the assumed absolute starting location of the subprogram. Each ROM word includes an extra bit to indicate whether the corresponding data word contains an address requiring relocation. As a word is read out of ROM, a gating circuit tests whether an address relocation is required. If the test is positive, the gating circuit gates the value in the base register into one input of an adder located on the ROM package, the other input to the adder coming from the data word read out of the ROM. The resulting modified data word outputted from the adder is sent to the computer. If the ROM output does not indicate that a relocation is required, the gating circuit provides a zero input to the adder so that the adder output reflects the unmodified input from the ROM.

3 Claims, 3 Drawing Figures



United States Patent [19]
Hendrie
[11] **4,218,753**
[45] **Aug. 19, 1980**

[54] **MICROCODE-CONTROLLED MEMORY REFRESH APPARATUS FOR A DATA PROCESSING SYSTEM**

[75] Inventor: **Gardner C. Hendrie**, Carlisle, Mass.

[73] Assignee: **Data General Corporation**, Westboro, Mass.

[21] Appl. No.: **773,023**

[22] Filed: **Feb. 28, 1977**

[51] **Int. Cl.**[2] **G06F 13/00**; G11C 7/00
[52] **U.S. Cl.** **364/900**; 365/222
[58] **Field of Search** ... 364/200 MS File, 900 MS File; 340/173 DR; 365/222

[56] **References Cited**

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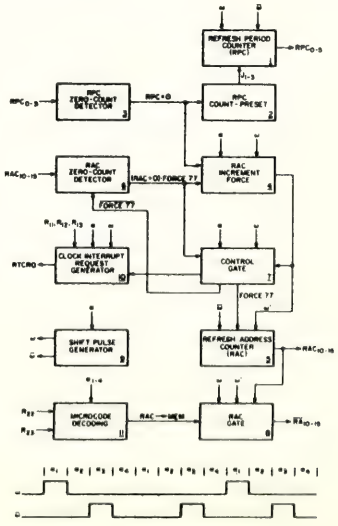
Vrba, "Dynamic Memory Research System" in *IBM Tech. Discl. Bull.*, vol. 19, No. 3, Aug. 1976, pp. 758–759.

Primary Examiner—Melvin B. Chapnick
Attorney, Agent, or Firm—Joel Wall; Jacob Frank

[57] **ABSTRACT**

A data processing system which employs a CPU and a MOS memory, the memory requiring replenishing or refreshing periodically. The CPU includes microcode containing microinstructions, the microinstructions providing control for the CPU including control for the memory. The refreshing scheme employs apparatus for decoding of these microinstructions and for providing refreshing signals to the memory in such a manner that all non-refreshing operations of the data processing system proceed without being delayed by operation of the refreshing apparatus. The algorithm which guides the operation of the CPU includes a number of system operating modes (such as FETCH, MULTIPLY, DIVIDE, HALT, DATA CHANNEL, and others). These modes each contain an operating state designated RAC→MEM which indicates that a refresh signal automatically is forwarded to the MOS memory when a particular operating mode runs through its respective operating states.

5 Claims, 12 Drawing Figures



United States Patent [19]
Frissell

[11] **4,228,501**
[45] **Oct. 14, 1980**

[54] **DATA TRANSFER TECHNIQUE FOR USE WITH PERIPHERAL STORAGE DEVICES**

[75] Inventor: **John M. Frissell,** Dracut, Mass.

[73] Assignee: **Data General Corporation,** Westboro, Mass.

[21] Appl. No.: **917,631**

[22] Filed: **Jun. 21, 1978**

[51] **Int. Cl.**[2] **G06F 13/04**
[52] **U.S. Cl.** **364/200**
[58] **Field of Search** ... 364/200 MS File, 900 MS File

[56] **References Cited**

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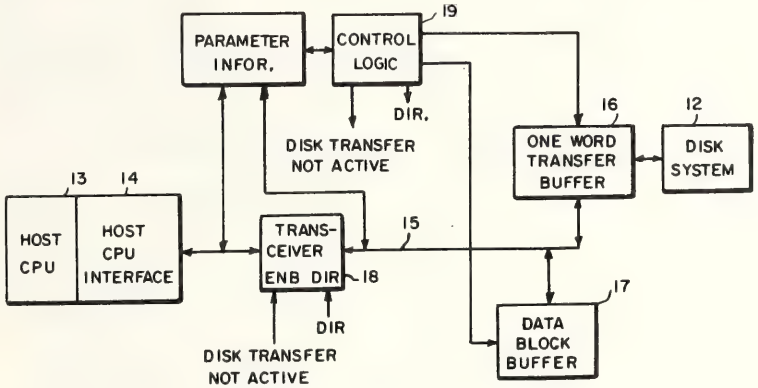
4,101,969	7/1978	Lawson et al.	364/900

Primary Examiner—Mark E. Nusbaum
Attorney, Agent, or Firm—Robert F. O'Connell

[57] **ABSTRACT**

Data processing apparatus wherein circuitry for data transfer between a central processor unit (CPU) and a peripheral storage unit, such as a hard disk storage unit, comprises a data transfer bus by which a block of data words being transferred is supplied to a temporary storage unit capable of storing the entire block. Means are provided to prevent any data transfer between the data bus and the CPU interface unit while the block of data words is transferred between the temporary storage unit and the peripheral storage unit and to permit transfer between the CPU interface unit and the bus when data is not being transferred between the temporary storage unit and the peripheral storage unit.

7 Claims, 2 Drawing Figures



United States Patent [19]
Kintner

[11] **4,200,914**
[45] **Apr. 29, 1980**

[54] **MEMORY PROGRAMMING CONTROL SYSTEM FOR STORING A WIRE NUMBER PROGRAM OF A LADDER DIAGRAM FOR A PROGRAMMABLE CONTROLLER**

[75] Inventor: **Paul M. Kintner,** Bayside, Wis.

[73] Assignee: **Eaton Corporation,** Cleveland, Ohio

[21] Appl. No.: **853,879**

[22] Filed: **Nov. 22, 1977**

[51] **Int. Cl.**[2] **G06F 15/46; G06F 9/16**
[52] **U.S. Cl.** **364/900**
[58] **Field of Search** 364/900, 104, 200

[56] **References Cited**

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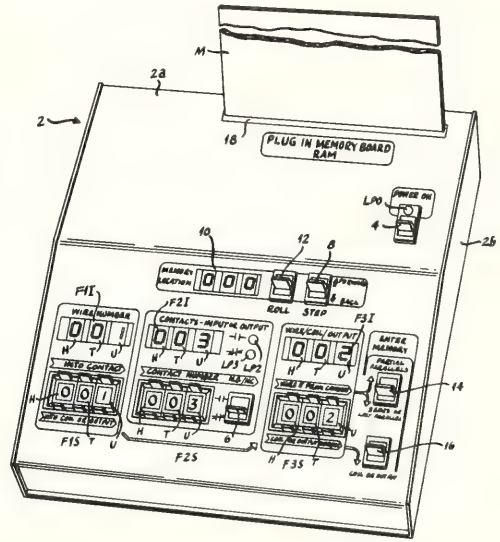
Primary Examiner—Gareth D. Shaw
Assistant Examiner—David Y. Eng
Attorney, Agent, or Firm—Hugh R. Rather; William A. Autio

[57] **ABSTRACT**

A portable programmer panel incorporating switches, logic circuits and data indicators for storing a wire number program of a ladder diagram in a memory. A memory board is plugged into the panel. Selected sets of switches corresponding to fields F1, F2 and F3 are repeatedly set on a decimal basis for three successive instruction words (data) to be multiplexed into memory locations, respectively indicative of the input wire number (F1), the contact number (F2), and the output wire number (F3) for a series contact or the last parallel contact; or the input wire number (F1) and the control coil or other output device number (F3) for an output function; or the input wire number (F1) and the contact number (F2) for a parallel contact other than the last. Simultaneously, a switch in the F2 field is set to program the normally-open (N.O.) or normally-closed (N.C.) nature of the contact. Write-control switches are selectively actuated to enter the data in the memory and distinguish between all but the last one of parallel contacts, series contacts or the last parallel contact, and a control coil or other output function, and to display such data in decimal form and to step to the next memory address. Switches are incorporated along with a decimal indicator for displaying the memory location being addressed and for "rolling" at high speed or for stepping to locations forward or back and for displaying the data stored in each memory location being traversed.

18 Claims, 15 Drawing Figures



United States Patent [19]

Kintner

[11] **4,227,247**

[45] **Oct. 7, 1980**

[54] **INTEGRATED CIRCUIT CONTROLLER PROGRAMMABLE WITH UNIDIRECTIONAL-LOGIC INSTRUCTIONS REPRESENTATIVE OF SEQUENTIAL WIRE NODES AND CIRCUIT ELEMENTS OF A LADDER DIAGRAM**

[75] Inventor: **Paul M. Kintner**, Bayside, Wis.

[73] Assignee: **Eaton Corporation**, Cleveland, Ohio

[21] Appl. No.: **841,431**

[22] Filed: **Oct. 12, 1977**

[51] **Int. Cl.**[3] **G06F 9/06**; G05B 11/01

[52] **U.S. Cl.** **364/900**; 364/104

[58] **Field of Search** ... 364/200 MS File, 900 MS File, 364/104, 107, 200, 900

[56] **References Cited**

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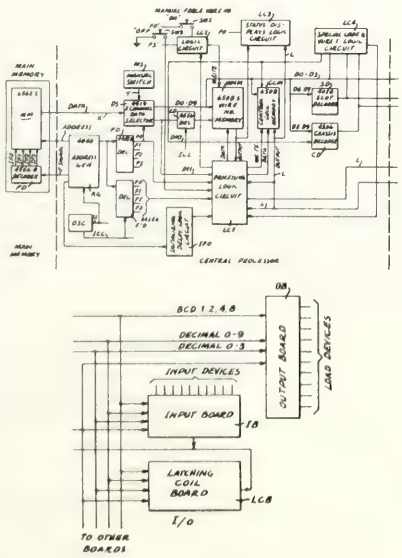
4,051,326	9/1977	Badagnani et al.	364/900 X
4,078,259	3/1978	Soulsby et al.	364/900

Primary Examiner—Gareth D. Shaw
Assistant Examiner—Thomas M. Heckler
Attorney, Agent, or Firm—Hugh R. Rather; William A. Autio

[57] **ABSTRACT**

A programmable controller that is programmed to simulate a ladder diagram and accepts input signals to control output devices in accordance with the ladder diagram program and comprising, in addition to a main memory that stores the program, a logic processor and input/output circuits, of a special wire number memory and a control coil memory for receiving, storing and making available to the processor the result of every logic function representing the current on-off status of each wire node and each control coil and associated contacts. This controller affords the maintenance of a complete current record of the changing status of the contacts and their interconnecting circuit nodes. This makes possible a particularly simple unidirectional-logic programming mode because the programmer does not have to keep track of which logic operations must be temporarily stored. This storage affords a powerful monitoring means in that signal tracing can be accomplished by merely calling up predetermined wire numbers from the special wire number memory and displaying the status thereof, or calling up predetermined input devices or control coils to view the status thereof. Moreover, for maintenance purposes, this architecture provides a selector switch and logic circuitry whereby a predetermined wire node may be manually forced "on" or "off" for maintenance purposes or the like.

21 Claims, 20 Drawing Figures



United States Patent [19]

Conners

[11] **4,212,076**

[45] **Jul. 8, 1980**

[54] **DIGITAL COMPUTER STRUCTURE PROVIDING ARITHMETIC AND BOOLEAN LOGIC OPERATIONS, THE LATTER CONTROLLING THE FORMER**

[75] Inventor: **John P. Conners**, Fond du Lac, Wis.

[73] Assignee: **Giddings & Lewis, Inc.**, Fond du Lac, Wis.

[21] Appl. No.: **726,277**

[22] Filed: **Sep. 24, 1976**

[51] **Int. Cl.**[2] **G06F 9/06**

[52] **U.S. Cl.** **364/706**; 364/200

[58] **Field of Search** 235/156, 164; 364/200, 364/900, 706

[56] **References Cited**

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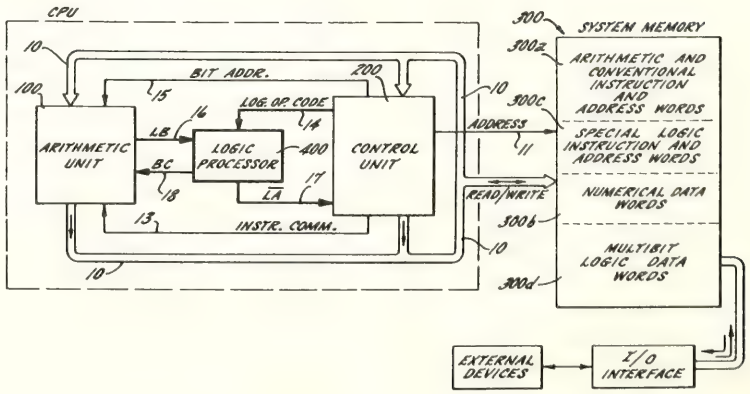
4,010,452	3/1977	Cazanove	445/1

Primary Examiner—David H. Malzahn
Attorney, Agent, or Firm—Leydig, Voit, Osann, Mayer & Holt, Ltd.

[57] **ABSTRACT**

A digital computer of relatively simple and efficient structural organization which is capable not only of conventional arithmetic operations according to a program but also of (i) performing chained Boolean logic processing on any selected bit of any of various selected words held in memory, (ii) using the logic processing result by storing it at any selected bit location in any of various selected words held in memory, and/or (iii) causing different, predetermined instructions within a program to have their execution dependent upon the results of previously performed single bit logic processing. The logic processing is carried out in response to specially coded instruction words which may be randomly interspersed between conventional arithmetic instruction steps within an overall program. Existing registers and apparatus components necessary for conventional arithmetic operations are utilized in large measure to carry out the routing of signals to and from the logic processor, and very little added hardware is required to create the logic processing, storing, and dependent conditioning.

35 Claims, 13 Drawing Figures



United States Patent [19]
Beadle et al.
[11] **4,225,918**
[45] **Sep. 30, 1980**

[54] **SYSTEM FOR ENTERING INFORMATION INTO AND TAKING IT FROM A COMPUTER FROM A REMOTE LOCATION**

[75] Inventors: **Bruce R. Beadle; John P. Conners; Michael E. Larson,** Fond du Lac, all of Wis.

[73] Assignee: **Giddings & Lewis, Inc.,** Fond du Lac, Wis.

[21] Appl. No.: **775,986**

[22] Filed: **Mar. 9, 1977**

[51] **Int. Cl.**[2] **G06F 3/04;** G06F 11/00
[52] **U.S. Cl.** **364/200**
[58] **Field of Search** ... 364/200 MS File, 900 MS File; 179/2 DP; 235/302, 304, 304.1; 340/146.1 R, 146.1 C; 324/73 R, 73 AT

[56] **References Cited**

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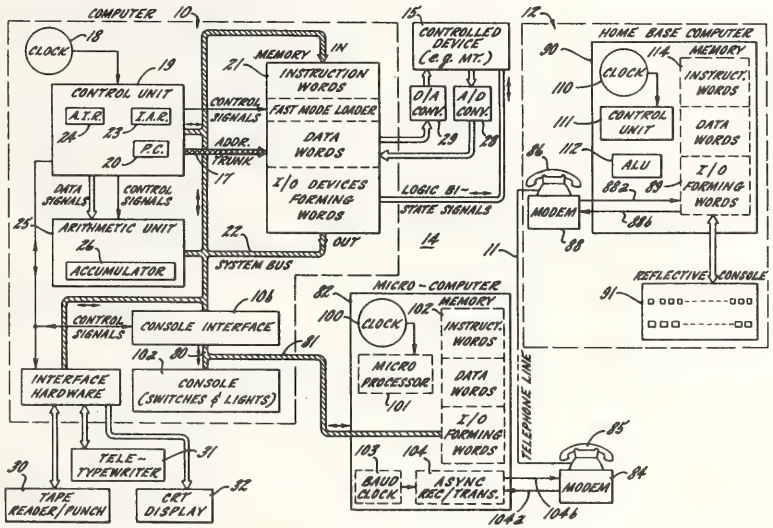
4,109,309	8/1978	Johnstone et al.	364/900 X

Primary Examiner—Melvin B. Chapnick
Attorney, Agent, or Firm—Leydig, Voit, Osann, Mayer & Holt, Ltd.

[57] **ABSTRACT**

A system for transmitting binary instruction or data words to or from a computer by control from a home base remote from the computer site, and characterized by the entry of signals into the computer or the extraction of signals from the computer performed by apparatus which directly connects to the computer console manual switches and indicator lights. A single telephone line forming two simultaneously active channels transmitting time-spaced pulses in opposite directions, by modems known in the art, is used as the communication link. A special purpose microcomputer directly connected to the main computer console acts figuratively to actuate the console push buttom switches in response to pulse train signals received from home base and representing single bits or multibit words. It returns to the home base a rapidly iterated and updated pulse train representative of the status of all console lights. The system includes another computer at the home base with a duplicate, reflective console like that of the main computer. The apparatus at the home base computer responds to binary messages to the main computer, due to actuation of the reflective console, with the same effect as if it were bing used and observed at the computer site.

26 Claims, 9 Drawing Figures



United States Patent [19]
Fauchier et al.
[11] **4,188,617**
[45] **Feb. 12, 1980**

[54] **SYSTEM FOR CONVERTING ANALOG SIGNALS TO MULTIPLEXED DIGITAL DATA**

[75] Inventors: **Jess F. Fauchier; William H. Seipp,** both of Bettendorf; **Stephen E. Whiteside,** Davenport, all of Iowa

[73] Assignee: **Gulf & Western Industries, Inc.,** New York, N.Y.

[21] Appl. No.: **916,287**

[22] Filed: **Jun. 16, 1978**

Related U.S. Application Data

[63] Continuation of Ser. No. 727,792, Sep. 29, 1976, abandoned.

[51] **Int. Cl.**[2] **G08C 15/06**
[52] **U.S. Cl.** ..... **340/183;** 364/900; 179/15 R
[58] **Field of Search** ..... 340/347 M, 347 AD, 183, 340/147 C, 150; 364/900; 179/15 R

[56] **References Cited**

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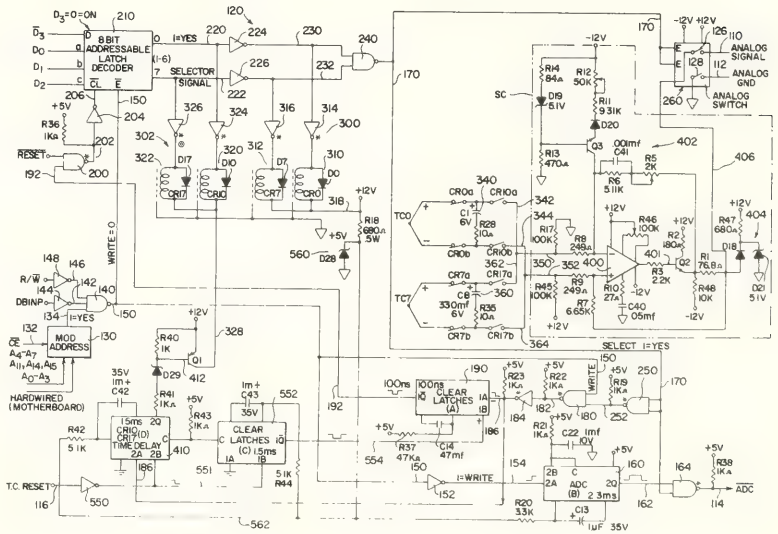
Hnatek, A User's Handbook of D/A and A/D Converters, J. Wiley & Sons, 6/76, pp. 395-401.

Primary Examiner—Thomas J. Sloyan
Attorney, Agent, or Firm—Meyer, Tilberry & Body

[57] **ABSTRACT**

A system for providing digital data representative of a selected analog signal on the data lines of a programmable controller using a central processing unit. The system employs a conversion circuit which converts the input analog signal to digital data on output data terminals upon receipt of a conversion signal simultaneously with an analog signal and which creates a completion signal when the conversion is completed. The system can use at least two analog inputs that receive at least two analog conditions and convert a selected one of the analog conditions to an analog signal. Upon actuation of one of the input modules, the selected analog signal of the selected module is directed to the conversion circuit. After conversion, the conversion completion signal of a conversion circuit then deactivates the actuated input module for the next conversion cycle.

4 Claims, 11 Drawing Figures



United States Patent [19]

Seipp

[11] **4,200,916**

[45] **Apr. 29, 1980**

[54] **PROGRAMMABLE CONTROLLER USING MICROPROCESSOR**

[75] Inventor: **William H. Seipp**, Bettendorf, Iowa

[73] Assignee: **Gulf & Western Industries, Inc.**, New York, N.Y.

[21] Appl. No.: **914,807**

[22] Filed: **Jun. 12, 1978**

Related U.S. Application Data

[62] Division of Ser. No. 701,858, Jul. 1, 1976, Pat. No. 4,107,785.

[51] **Int. Cl.**[2] **G05B 11/01**

[52] **U.S. Cl.** **364/900**

[58] **Field of Search** ... 364/200 MS File, 900 MS File

[56] **References Cited**

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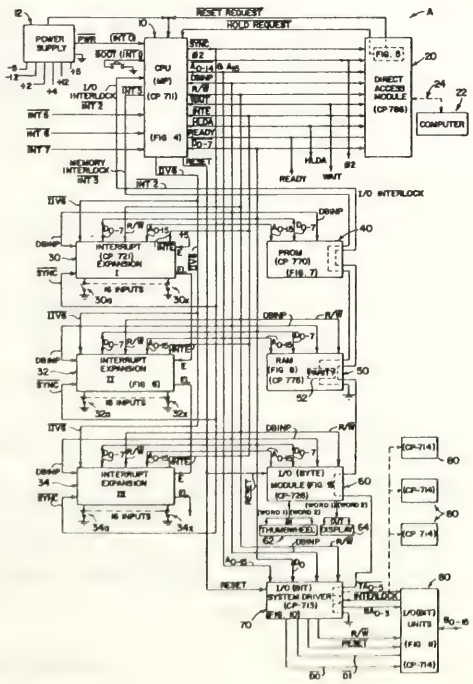
4,028,538	6/1977	Olander, Jr. et al.	364/900
4,062,061	12/1977	Batchelor et al.	364/900
4,078,259	3/1978	Soulsby et al.	364/900

Primary Examiner—Gareth D. Shaw
Assistant Examiner—C. T. Bartz
Attorney, Agent, or Firm—Meyer, Tilberry & Body

[57] **ABSTRACT**

There is provided a programmable controller comprising a standard microprocessor having output address terminals and input/output bi-directional data terminals and means for providing a binary code on the data terminals indicative of the status of the machine cycle to be processed by the microprocessor. This programmable controller includes a logic decoder means for producing a selected signal in response to logic signals on selected address terminals and in the status binary code of the data terminals. In addition, the programmable controller includes means for programming the HOLD state for the microprocessor. There is also provided an arrangement for expanding the number of interrupt conditions which can affect the INTERRUPT state of the microprocessor in the programmable controller.

6 Claims, 28 Drawing Figures



United States Patent [19]

McCarthy

[11] **4,204,208**

[45] **May 20, 1980**

[54] **DISPLAY OF VIDEO IMAGES**

[75] Inventor: **Edward C. McCarthy**, Indian Harbor Beach, Fla.

[73] Assignee: **Harris Corporation**, Cleveland, Ohio

[21] Appl. No.: **829,044**

[22] Filed: **Aug. 30, 1977**

[51] **Int. Cl.**[2] **G06K 15/20**

[52] **U.S. Cl.** **340/745**; 340/751; 340/799; 364/900

[58] **Field of Search** ..... 340/324 AD, 745, 751, 340/799

[56] **References Cited**

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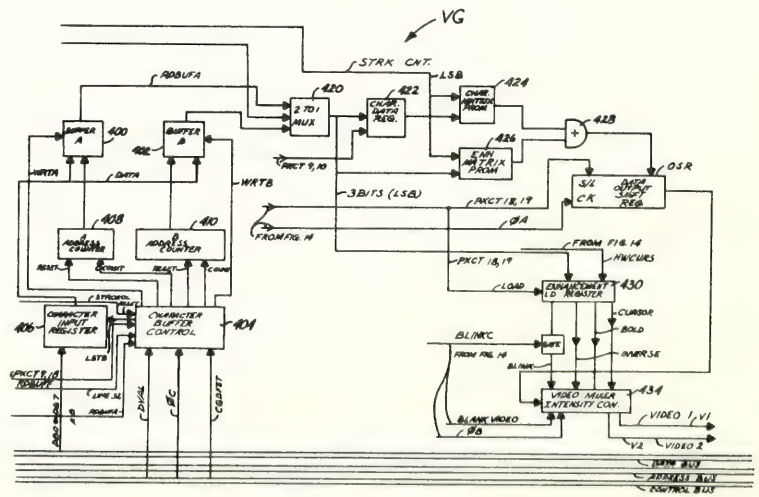
3,696,387	10/1972	Nussbaum	340/324 AD
3,821,730	6/1974	Carey et al.	340/324 AD
3,883,728	5/1975	Schwartz et al.	340/751 X

Primary Examiner—David L. Trafton

[57] **ABSTRACT**

The system displays video images of data characters or other graphics with video modifications being made thereto. A coded data character is provided which represents a first graphical image from a first library, such as a font, of related images to be displayed. A second coded data character is provided which represents a second graphical image from a second library, such as a font, of related images wherein the first library of related images is independent of the second library of related images. A storage facility is provided for each library with the facility storing video display instructions for forming each character or graphical image in the library of graphical images. The storage facility for the first library of images is interrogated by the first coded data character to obtain therefrom the video display instructions for forming the image represented by that data character. The storage facility of images for the second library of images is interrogated by the second coded data character to obtain from the storage facility the video display instructions for forming the graphical image represented by that data character. The video display instructions for forming the video image of the character from the first library are combined with the instructions for forming the graphical image from the second library. The combined video display instructions are employed for forming a graphical image having the combined video characteristics of the images represented by the first coded data character and the second coded data character.

12 Claims, 32 Drawing Figures



United States Patent [19]

Rozell et al.

[11] **4,223,381**

[45] **Sep. 16, 1980**

[54] **LOOKAHEAD MEMORY ADDRESS CONTROL SYSTEM**

[75] Inventors: **James O. Rozell**, Richardson; **David W. Abmayr**, Carrollton, both of Tex.

[73] Assignee: **Harris Corporation**, Cleveland, Ohio

[21] Appl. No.: **921,075**

[22] Filed: **Jun. 30, 1978**

[51] **Int. Cl.**[2] **G06F 13/00**; G06F 9/06

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** ... 364/200 MS File, 900 MS File; 365/230, 236, 239

[56] **References Cited**

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3,760,369	9/1973	Kemp	364/200
4,025,903	5/1977	Kaufman	364/200
4,118,773	10/1978	Raguin	364/200

Primary Examiner—James D. Thomas
Attorney, Agent, or Firm—Craig & Antonelli

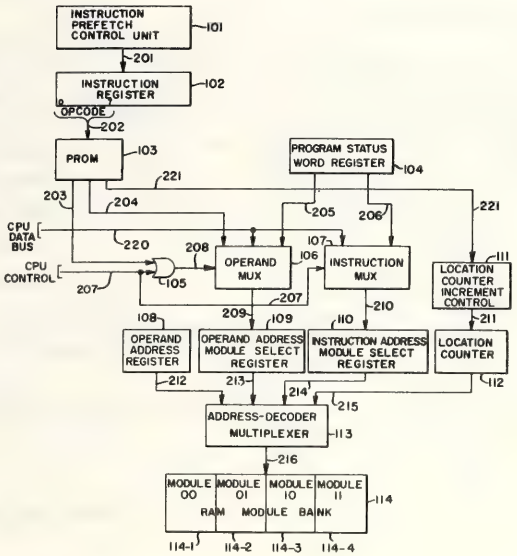
[57] **ABSTRACT**

A selective memory addressing scheme employs a programmable read only memory (PROM) which responds to the opcode of the next instruction to be executed and supplies control information to memory module selection registers.The memory module selection registers operate in conjunction with the internal address registers to provide the necessary steering information for properly addressing the intended memory location. The PROM is programmed in accordance with the instruction set by which the processor operates and is coupled to decode the opcode contents of the instruction register that has been loaded, in a lookahead fashion, with the instruction following the instruction presently being executed by the central processing unit.

The PROM has a first output that defines whether or not a second output of the PROM is to be used to select the memory module containing the operand to be referenced in the execution of the next instruction. This second output of the PROM is of a code size required to identify any one of the modules in the bank. The PROM has a third output that may be used to increment the location counter based upon the length of the next instruction. Where the second output of the PROM is not to be used to select the memory module containing the operand to be referenced, the first output of the PROM has a state such that it gates out information stored in a program status word register to identify the memory module containing the operand of the next instruction to be executed.

To provide for direct CPU intervention in the execution of instructions, such as may occur in the case of an interrupt, prescribed bits of the CPU data bus may be selectively coupled to the module selection circuitry, so that the opcode-dependent operation of the PROM is bypassed and direct CPU selection within the memory bank may be achieved.

19 Claims, 2 Drawing Figures



United States Patent [19]

Furukawa et al.

[11] **4,183,090**

[45] **Jan. 8, 1980**

[54] **MAGNETIC BUBBLE MEMORY EQUIPMENT**

[75] Inventors: **Kazuo Furukawa; Takeshi Masuda**, both of Yokohama; **Masakatu Nunotani**, Tokyo; **Norio Amano**, Higashiyamato, all of Japan

[73] Assignee: **Hitachi, Ltd.**, Japan

[21] Appl. No.: **897,392**

[22] Filed: **Apr. 18, 1978**

[30] **Foreign Application Priority Data**

Apr. 20, 1977 [JP] Japan 52-44444

[51] **Int. Cl.**[2] **G06C 13/00**; G11C 19/08

[52] **U.S. Cl.** **364/900**; 365/15

[58] **Field of Search** ..... 364/200 MS File, 900, 364/200; 365/15

[56] **References Cited**

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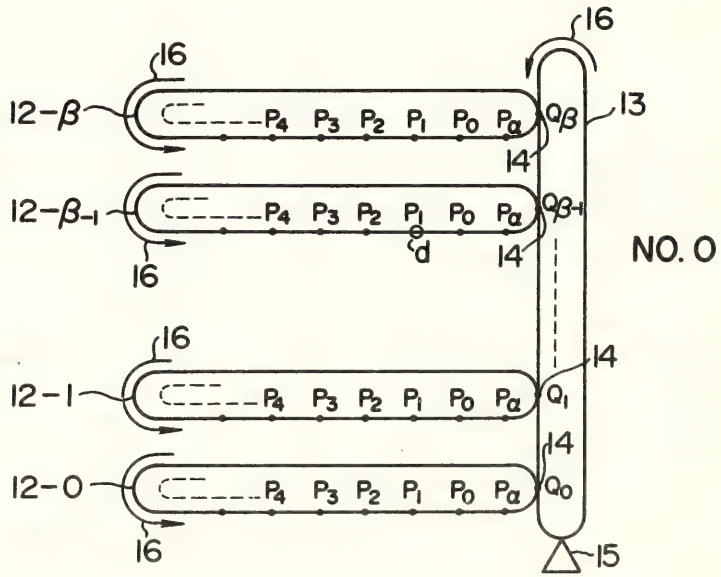
4,064,556	12/1977	Edelberg	364/900

Primary Examiner—Gareth D. Shaw
Assistant Examiner—David Y. Eng
Attorney, Agent, or Firm—Craig and Antonelli

[57] **ABSTRACT**

A magnetic bubble memory equipment includes means for receiving address information for a plurality of access requests as a whole, and means for executing address matching operations in parallel for a plurality of addresses. Read-out or write-in command information is fetched for each of the access requests in the sequential order as the coincidence is found in the matching of address and data transfer is sequentially executed in accordance with the command information, thereby to reduce the effective access time for the plurality of the access requests.

8 Claims, 18 Drawing Figures



United States Patent [19]
Hirosawa et al.
[11] **4,206,346**
[45] **Jun. 3, 1980**

[54] **SYSTEM FOR GATHERING DATA REPRESENTING THE NUMBER OF EVENT OCCURRENCES**

[75] Inventors: **Toshio Hirosawa**, Hachioji; **Tsugio Momose**, Hatano; **Shigeo Nagashima**, Hachioji, all of Japan

[73] Assignee: **Hitachi, Ltd.**, Tokyo, Japan

[21] Appl. No.: **827,361**

[22] Filed: **Aug. 24, 1977**

[30] **Foreign Application Priority Data**

Sep. 1, 1976 [JP] Japan 51/103646

[51] **Int. Cl.**[2] **G06M 3/08**; G07C 3/10
[52] **U.S. Cl.** ..... **235/92 PD**; 235/92 DP; 364/900
[58] **Field of Search** ... 364/200 MS File, 900 MS File; 235/92 CC, 92 DP, 92 ST, 92 PL, 92 SA, 92 EA

[56] **References Cited**

U.S. PATENT DOCUMENTS

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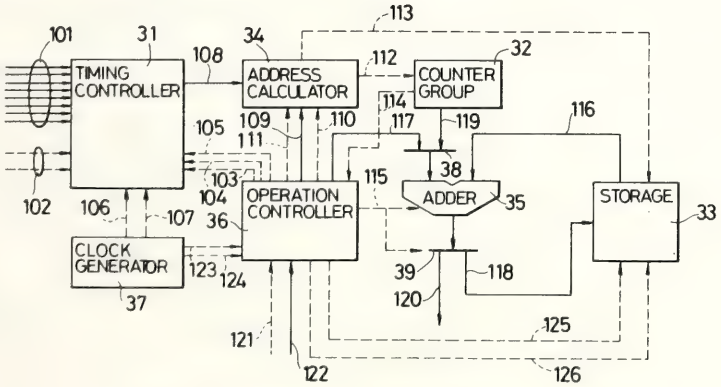
3,829,841	8/1974	Steinberg	364/200
3,906,454	9/1975	Martin	364/200

Primary Examiner—Joseph M. Thesz
Attorney, Agent, or Firm—Craig and Antonelli

[57] **ABSTRACT**

A gathering system in an electronic computer including detecting means for detecting the occurrences of each of a plurality of events, a counter group having a plurality of counters each of which counts the number of occurrences of corresponding event until the number thereof becomes 2^l, a storage having a plurality of memory areas, each storing 2^{K-l} occurrences of the corresponding event and a processing unit for gathering data representative of the number of occurrences of each of the events from the counter and the storage unit.

9 Claims, 8 Drawing Figures



United States Patent [19]
Cooper
[11] **4,213,176**
[45] **Jul. 15, 1980**

[54] **SYSTEM AND METHOD FOR INCREASING THE OUTPUT DATA THROUGHPUT OF A COMPUTER**

[75] Inventor: **Paul J. Cooper**, Acton, Mass.

[73] Assignee: **NCR Corporation**, Dayton, Ohio

[21] Appl. No.: **753,398**

[22] Filed: **Dec. 22, 1976**

[51] **Int. Cl.**[2] **G06F 3/00**
[52] **U.S. Cl.** **364/200**
[58] **Field of Search** ... 364/200 MS File, 900 MS File

[56] **References Cited**

U.S. PATENT DOCUMENTS

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3,924,240	12/1975	Given	364/200
3,938,098	2/1976	Garlic	364/200
3,990,049	11/1976	Wirth	364/900
4,017,841	4/1977	Jensen	364/900

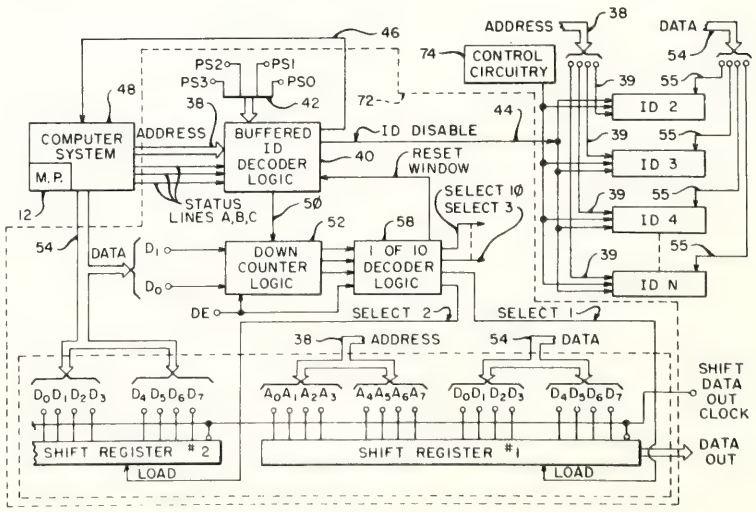
Primary Examiner—Leo H. Boudreau
Attorney, Agent, or Firm—J. T. Cavender; Albert L. Sessler, Jr.; Elmer Wargo

[57] **ABSTRACT**

A circuit and method for increasing the output data per unit time from a computer to its associated peripheral terminals or utilization devices is disclosed in which the computer output address and data lines are time multiplexed by a novel decoding technique which enables the address bits and data bits to be interpreted together to form a new data word having a number of bits equal to the sum of the original data bits and the address bits interpreted as data bits. A plurality of decoders, each at a peripheral terminal and each having an identification address code, enable a window for decoding multiple transfers of data on output address and data lines, said window having a predetermined time duration during which all other peripheral identification address codes are locked out, until the data transfer is completed.

A microprocessor embodying the invention is also disclosed in which the output data capability is increased from eight to sixteen bits without hardware modification to the microprocessor.

14 Claims, 5 Drawing Figures



United States Patent [19]

Antonaccio et al.

[11] **4,223,380**

[45] **Sep. 16, 1980**

[54] **DISTRIBUTED MULTIPROCESSOR COMMUNICATION SYSTEM**

[75] Inventors: **Joseph C. Antonaccio**, Hazlet, N.J.; **Bernard J. Verreau**, Milford, Del.

[73] Assignee: **NCR Corporation**, Dayton, Ohio

[21] Appl. No.: **893,856**

[22] Filed: **Apr. 6, 1978**

[51] **Int. Cl.**[3] **G06F 15/16; H04J 3/00**

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** ... 364/200 MS File, 900 MS File; 179/15 AL

[56] **References Cited**

U.S. PATENT DOCUMENTS

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4,099,233	7/1978	Barbagelata et al.	364/200

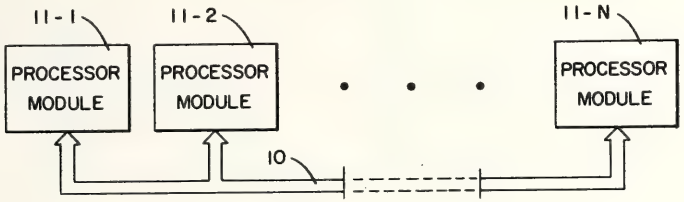
Primary Examiner—Gareth D. Shaw
Assistant Examiner—Thomas M. Heckler
Attorney, Agent, or Firm—J. T. Cavender; Wilbert Hawk, Jr.; Richard W. Lavin

[57] **ABSTRACT**

A distributed multiprocessor communication system, wherein the central processing unit (CPU) is relieved of the burden of bus management by a scheme which multiplexes the interprocessor module communications bus, to which all processors are guaranteed access, so that only an addressed CPU may be interrupted from performing its dedicated data processing function. Associated with each independent processor is a communications interface unit or communications network routing unit which relieves the processor of the task of decoding communications on the interprocessor or intermodule communications bus and, in addition, upon decoding its address and buffering message data, transmits a "handshake" signal over the bus back to the sender during a designated time slot, thereby informing the sender that the transmitted message was actually received. Moreover, if one module is in a high priority mode of communication with another module, all lower priority messages are prevented from entering that particular module; yet, any other pairs of modules may still communicate. In other words, no module can possibly tie up the bus, preventing other modules from communicating.

Once the data is placed onto the bus, under CPU direction, the transmission, reception, priority discrimination, and handshake are completely independent on CPU operation so that the time required to transfer a byte of data is independent of any processor in the system.

22 Claims, 6 Drawing Figures



United States Patent [19]

Davis et al.

[11] **4,187,540**

[45] **Feb. 5, 1980**

[54] **CONTROL PANEL SELF-TEST**

[75] Inventors: **Thomas T. Davis; Marvin C. Burk**, both of Bartlesville, Okla.

[73] Assignee: **Phillips Petroleum Company**, Bartlesville, Okla.

[21] Appl. No.: **870,546**

[22] Filed: **Jan. 18, 1978**

[51] **Int. Cl.**[2] **G06F 11/06**; G06F 3/14; G06F 3/02

[52] **U.S. Cl.** **364/200**; 235/302

[58] **Field of Search** ... 364/200 MS File, 900 MS File, 364/480, 481, 488, 489, 490; 235/302, 304; 324/73 R, 73 AT

[56] **References Cited**

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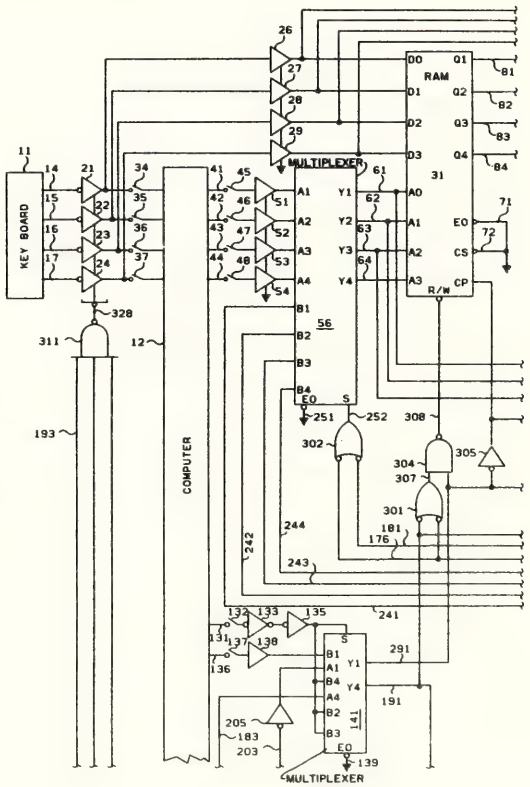
3,831,148	8/1974	Greenwald	364/200
3,866,171	2/1975	Loshbough	235/302
3,909,802	9/1975	Cassarino, Jr.	364/200

Primary Examiner—James D. Thomas

[57] **ABSTRACT**

A control panel which provides an interface to a digital computer, and which comprises at least a data input device such as a keyboard and a data output device such as an alphanumeric display or a light emitting diode display, is tested without the use of the digital computer. The digital computer is disconnected or bypassed and the timing and other functions of the computer are simulated to enable an independent test of the data input device and the data output device which make up at least a part of the control panel.

14 Claims, 4 Drawing Figures



United States Patent [19]

DeShon

[11] **4,188,664**

[45] **Feb. 12, 1980**

[54] **I/O TERMINAL IDENTIFICATION**

[75] Inventor: **Wallace E. DeShon**, Bartlesville, Okla.

[73] Assignee: **Phillips Petroleum Company**, Bartlesville, Okla.

[21] Appl. No.: **851,650**

[22] Filed: **Nov. 15, 1977**

[51] **Int. Cl.**[2] **G06F 3/02**

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** ... 364/200 MS File, 900 MS File; 340/167 R, 152 R

[56] **References Cited**

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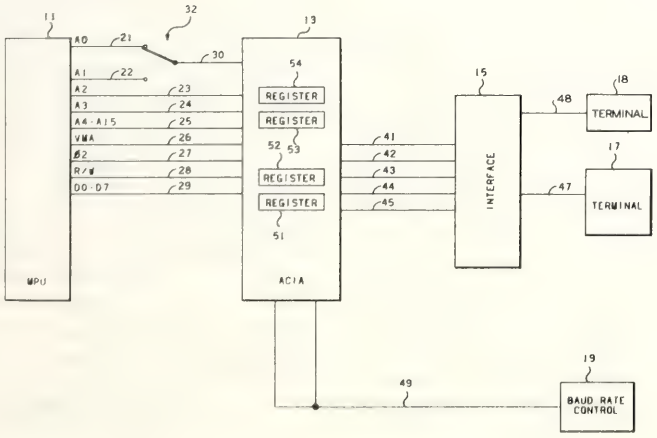
4,016,369	4/1977	Pedersen	364/900
4,079,452	3/1978	Larson	364/900

Primary Examiner—James D. Thomas

[57] **ABSTRACT**

Control of the data format programmed into an interface means by a computer means is provided in response to the data format required by an I/O device. A register in the interface means is programmed to respond to only a first digital address from the computer means. A switching means having first and second positions is utilized to create "don't care" positions in a digital address from the computer means to the interface means. Because of the "don't care" positions in the digital address the register in the interface means will respond to a second digital address when the switching means is in the first position. The register will not respond to the second digital address when the switching means is in the second position. When the register responds to the second digital address then the computer programs the data format required by a first I/O means into the interface means. When the register does not respond to the second digital address then the computer programs the data format required by a second I/O means into the interface means. Thus, the position of the switching means determines the data format which will be programmed into the interface means.

9 Claims, 1 Drawing Figure



United States Patent [19]

Mueller et al.

[11] **4,213,189**

[45] **Jul. 15, 1980**

[54] **REACTIVE COMPUTER SYSTEM ADAPTIVE TO A PLURALITY OF PROGRAM INPUTS**

[75] Inventors: **David J. Mueller**, Elk Grove Village; **Daniel G. Prysby**, Chicago; **John V. Moravec**, Berwyn, all of Ill.; **George A. Watson**, Tustin, Calif.

[73] Assignee: **Admiral Corporation**, Schaumburg, Ill.

[21] Appl. No.: **806,304**

[22] Filed: **Jun. 13, 1977**

[51] **Int. Cl.**[2] **G06F 3/00**; G06K 15/20

[52] **U.S. Cl.** ..... **364/100**; 340/703; 340/709; 340/725; 340/741; 340/748; 340/798; 340/799; 273/85 G; 273/DIG. 28

[58] **Field of Search** ... 364/200 MS File, 900 MS File, 364/521, 200, 900; 358/81, 82, 903; 340/324 AD, 745, 725, 701, 703, 731, 756, 799; 273/DIG. 28

[56] **References Cited**

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4,142,180	2/1979	Burson	273/DIG. 28 X
4,155,095	5/1979	Kirschner	273/DIG. 28 X

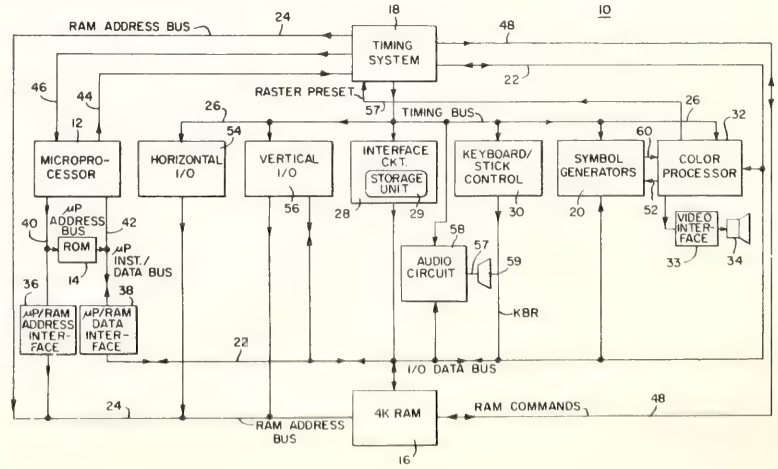
Primary Examiner—Raulfe B. Zache

Attorney, Agent, or Firm—R. Lewis Gable; Albert G. Marriott

[57] **ABSTRACT**

There is disclosed a computer system including a storage means such as a random access memory (RAM) for receiving data to be displayed upon a display means, e.g. a color cathode ray tube, a microprocessor for control of the computer system operations, and viewer input devices such as a control stick or keyboard, whereby the viewer may respond selectively to the data displayed upon the display means. A limited capacity storage unit, illustratively in the form of a tape cassette, stores data in the form of a program for permitting the viewer to store useful material in the form of a repository, such as a Christmas list; the program to be displayed by the display means can assume any of a limitless number of programs and may be adapted to an exceptionally wide range of uses for the home, office or school. The computer system permits the viewer to respond as through the input devices, to the material being displayed, whereby subsequent material may be effected. To effect a variety of operations, the computer system includes a record/read device for receiving the storage unit, whereby the stored data thereon may be read out and stored in the RAM for subsequent use by the computer system. In this regard, graphic material to be displayed upon the display means is stored in select locations in the RAM to be selectively read out, dependent upon the image to be displayed. Further, there is included a second storage means in the form of a read-only memory (ROM) for storing utility sub-routines, whereby various operations of the computer system may be controlled.

53 Claims, 55 Drawing Figures



United States Patent [19]

Morley et al.

[11] **4,213,174**

[45] **Jul. 15, 1980**

[54] **PROGRAMMABLE SEQUENCE CONTROLLER WITH DRUM EMULATION AND IMPROVED POWER-DOWN POWER-UP CIRCUITRY**

[75] Inventors: **Richard E. Morley**, Mason; **Michael A. Bromberg**, Nashua; **William A. Taylor**, Campton, all of N.H.

[73] Assignee: **Andover Controls Corporation**, Andover, Mass.

[21] Appl. No.: **802,261**

[22] Filed: **May 31, 1977**

[51] **Int. Cl.**[2] **G06F 15/46**; G06F 9/00; G05B 11/32

[52] **U.S. Cl.** **364/104**; 364/900

[58] **Field of Search** ..... 364/104, 107, 200, 900, 364/100, 103, 418, 550, 551; 307/141, 141.4, 141.8; 165/13, 14; 236/44 R, 44 C, 46 R, 46 A, 46 C, DIG. 8

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Primary Examiner—Joseph F. Ruggiero

Attorney, Agent, or Firm—Mattern, Ware, Davis & Stoltz

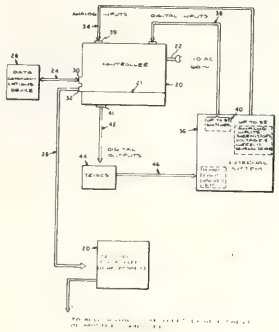
[57] **ABSTRACT**

A programmable sequence controller is disclosed utilizing digital and analog inputs in order to generate digital output driver signals for the control of external systems or devices. The controller emulates mechanical sequence drums so that at any one time each of the simulated drums within the controller executes one of the addressable drum lines programmed within the drum. Each line of each simulated drum can be programmed to specify the energization or deenergization of any output driver as well as the energization or de-energization of any memory bit utilized by the controller in order to provide communication between drums. Each drum may also be programmed to have one or two sets of exit conditions, which if met, cause the controller to effectively rotate the drum to a specified drum line and execute this new drum line during the next scan of the controller. The controller can also sense emergency conditions and cause any or all of the drums to rotate to a specified line regardless of the drum line then being executed by the controller for each of the drums. An improved power-down, power-up circuitry insures an ordered and complete shutdown of the controller if any of a number of conditions exist, including utility AC failure and impending failure of several of the power supply voltages. Handshaking circuitry between the power supply and the remainder of the controller insures that the controller maintains memory validity for all types of shutdown situations, including momentary losses of any supply voltage.

The programmable sequence controller includes a clock-calendar capable of continued operation during periods of extended power outages. The clock-calendar can be utilized in any drum line to form part of the control scheme.

All programming of the simulated drum lines is performed through an interconnected data communication device such as a teletypewriter and utilizes a simple user-oriented language, with monitoring and diagnostic capability to facilitate debugging.

57 Claims, 63 Drawing Figures



United States Patent [19]

Wozniak

[11] **4,210,959**

[45] **Jul. 1, 1980**

[54] **CONTROLLER FOR MAGNETIC DISC, RECORDER, OR THE LIKE**

[75] Inventor: **Stephen G. Wozniak**, San Jose, Calif.

[73] Assignee: **Apple Computer, Inc.**, Cupertino, Calif.

[21] Appl. No.: **904,420**

[22] Filed: **May 10, 1978**

[51] **Int. Cl.**[2] **G06F 13/08**; G06F 3/06

[52] **U.S. Cl.** **364/200**; 360/78

[58] **Field of Search** ... 364/200 MS File, 900 MS File, 364/200, 900; 360/69, 71, 78, 135

[56] **References Cited**

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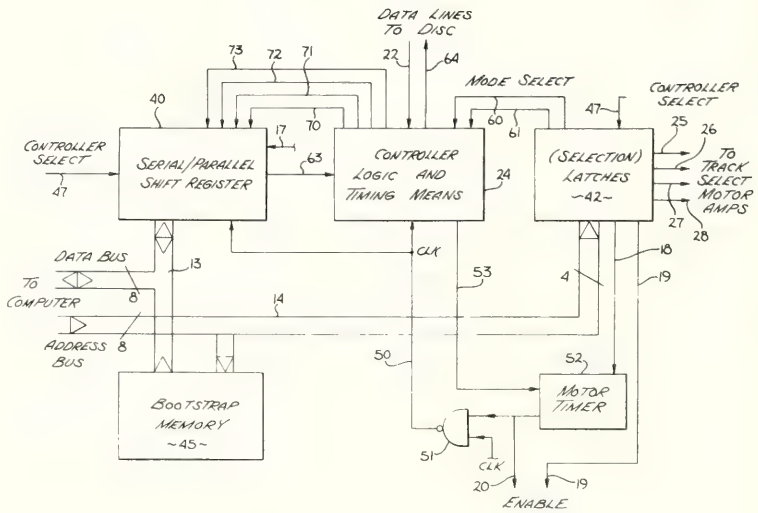
Primary Examiner—Mark E. Nusbaum

Attorney, Agent, or Firm—Blakely, Sokoloff, Taylor & Zafman

[57] **ABSTRACT**

A controller for interfacing between a digital computer and a magnetic disc recorder, such as a "floppy" disc, or other recorder or memory is disclosed. The controller, which permits accessing of the disc with minimum control by the computer, is realized with relatively few components and is particularly suited for interfacing between a microcomputer and a "minifloppy". Track selection with a computed velocity profile is employed. Synchronization with a soft sectored disc is achieved without additional hardware.

14 Claims, 6 Drawing Figures



United States Patent [19]

Steiner

[11] **4,205,388**

[45] **May 27, 1980**

[54] **TAXIMETER**

[75] Inventor: **Jack Steiner**, Laval, Canada

[73] Assignee: **Centrodyne Corporation**, Montreal, Canada

[21] Appl. No.: **816,296**

[22] Filed: **Jul. 18, 1977**

[51] **Int. Cl.**[2] **G07B 13/10**

[52] U.S. Cl. ..... **364/900**; 364/467; 235/30 R

[58] **Field of Search** ..... 364/900 MS File, 467, 364/464, 200 MS File; 235/30 R, 45, 92 TC; 346/15, 16

[56] **References Cited**

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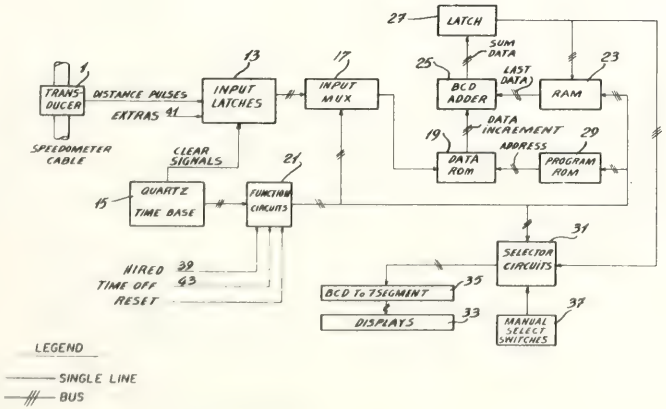
Primary Examiner—Raulfe B. Zache

[57] **ABSTRACT**

The invention relates to a dedicated microprocessor for an electronic taximeter, and a taximeter including the microprocessor. The microprocessor includes, (a) a main memory for storing data at a plurality of storage locations therein; (b) a data memory for receiving input data at a plurality of storage locations therein; (c) a combiner for combining the data storage locations of the main memory with the input data of respective storage locations of the data memory for updating the main memory; (d) a program memory for controlling the operation of the data memory, and comprising a plurality of storage locations therein; (e) a counter for sequentially selecting the storage locations of the main memory and the program memory; and (f) clock means for driving the counter means through its cycle. The main memory means is preferably a random access memory (RAM), and the data memory means and the program memory means can comprise, respectively, first and second read only memory (ROM) means. Each of the storage locations of the RAM and the first ROM comprise four bits of information whereby a single binary coded digit (BCD) can be stored at each of the aforesaid storage locations, and the combiner is preferably a BCD adder.

3 Claims, 3 Drawing Figures



United States Patent [19]

Gilham et al.

[11] **4,209,832**

[45] **Jun. 24, 1980**

[54] **COMPUTER-GENERATED DISPLAY FOR A FIRE CONTROL COMBAT SIMULATOR**

[75] Inventors: **Arthur W. S. Gilham**, Sterling Heights; **Stuart W. Flockencier**, Chesterfield Twp., Macomb County, both of Mich.

[73] Assignee: **Chrysler Corporation**, Highland Park, Mich.

[21] Appl. No.: **915,323**

[22] Filed: **Jun. 13, 1978**

[51] **Int. Cl.**[2] **G06F 3/14**

[52] **U.S. Cl.** **364/521**; 35/25; 340/721; 340/725; 358/104; 364/423; 364/528; 364/900

[58] **Field of Search** 364/423, 514, 515, 518, 364/520–523, 526, 578, 200, 900; 340/721, 725, 747; 35/25; 358/104, 903, 22

[56] **References Cited**

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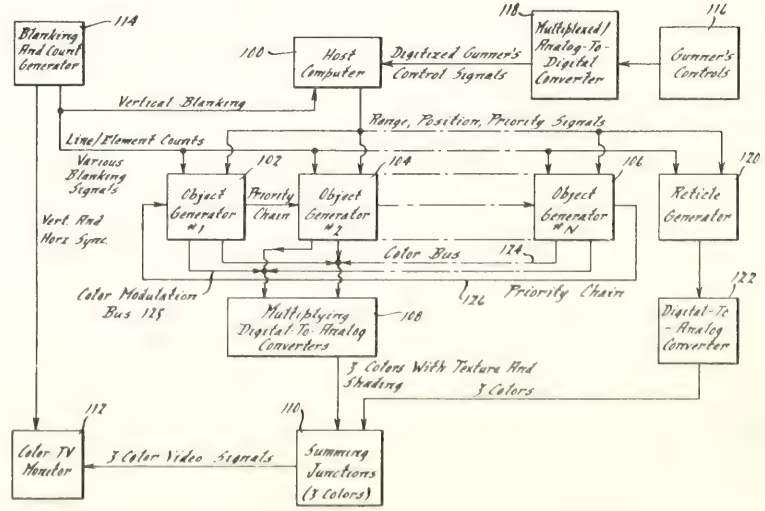
Primary Examiner—Errol A. Krass

Attorney, Agent, or Firm—Baldwin & Newtson

[57] **ABSTRACT**

Electronic generation of the display is accomplished by a system which includes a host computer, a plurality of object generators, and related circuitry. Each object generator contains a memory which stores the image of an object which may be displayed on the video display. The host computer assigns locations in the scene to the objects of each object generator. Each object generator includes its own microprocessor which performs calculations based on its own object information and position and range information received from the host computer to provide appropriate video signals for the display. The related circuitry of the system includes a blanking and count generator which provides signals whereby the color video information from the object generator is displayed on the video display and it also establishes times for permitting updating of the information between the host computer and the object generators. Further features include a priority chain linking the object generators which, if an overlap situation occurs where more than one object generator is calling for its information to be displayed in the same location on the video display, the object which has been assigned a higher priority, indicating that it is at a closer range than others, has its overlap information displayed on the video display instead of those of lower priority. Another feature is the data compression scheme employed to store the object image in each object generator.

6 Claims, 12 Drawing Figures



United States Patent [19]
Burns
[11] **4,201,887**
[45] **May 6, 1980**

[54] **DATA TELECOMMUNICATIONS TERMINAL**

[75] Inventor: **Chester A. Burns**, Palo Alto, Calif.
[73] Assignee: **Cordura Marketing, Inc.**, Chicago, Ill.

[21] Appl. No.: **904,983**
[22] Filed: **May 11, 1978**
[51] **Int. Cl.**[2] **H04M 11/00**
[52] **U.S. Cl.** ..... **179/2 DP; 364/900**
[58] **Field of Search** ..... 179/2 C, 2 DP; 364/200 MS File, 900 MS File

[56] **References Cited**

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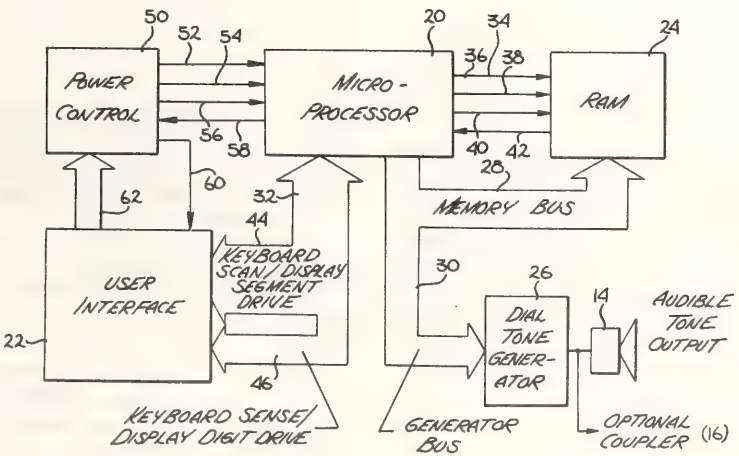
Primary Examiner—George G. Stellar

[57] **ABSTRACT**

A portable, hand-held data telecommunications terminal for use with a telephone system having a memory for storing data, a signal generator for generating signals corresponding to the data, a signal coupling device connected to the signal generator for coupling the signals to the telephone system, a keyboard, a microprocessor, and a self-contained power supply. The microprocessor is connected to the memory, the signal generator and the keyboard device so as to control, under the direction of the keyboard, the receipt of data from the keyboard, the storage of the data by the memory, and the generation of the signals by the signal generator. Data is entered into the memory from the keyboard device so that the data is available at a future time, to be coupled to the telephone system.

42 Claims, 13 Drawing Figures



United States Patent [19]
Schaeffer
[11] **4,218,754**
[45] **Aug. 19, 1980**

[54] **CONTROL OF HIGH SPEED PRINTER BY LOW SPEED MICROPROCESSOR**

[75] Inventor: **Timothy N. Schaeffer**, Arlington, Mass.
[73] Assignee: **Data Printer Corporation**, Cambridge, Mass.

[21] Appl. No.: **891,297**
[22] Filed: **Mar. 29, 1978**
[51] **Int. Cl.**[2] **G06F 3/12; B41J 5/30**
[52] **U.S. Cl.** **364/900; 400/279**
[58] **Field of Search** ..... 364/900 MS File; 400/279, 280, 281, 282

[56] **References Cited**

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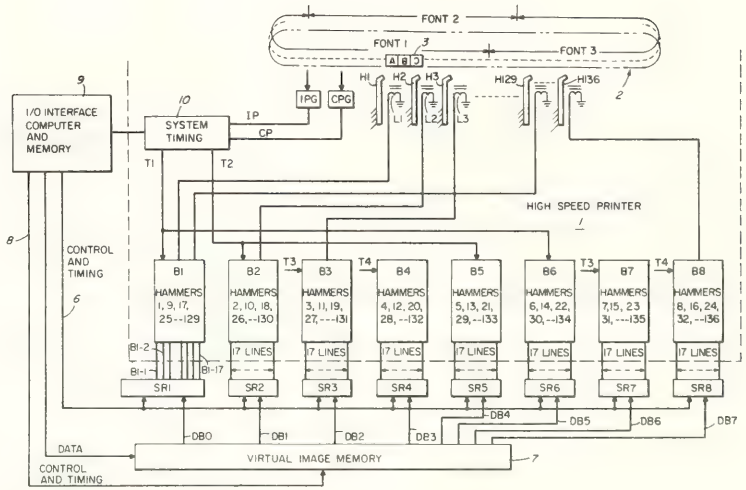
3,754,216	8/1973	Kekas et al.	364/900
4,009,654	3/1977	Harris, Jr. et al.	364/900

Primary Examiner—Leo H. Boudreau
Attorney, Agent, or Firm—John W. Ericson

[57] **ABSTRACT**

A control system for high speed printers including a low speed microprocessor that processes data input by a one-time serial operation on the data bytes to direct printing operations into a virtual image memory that is a map of the printing sequence for an entire line. A map of the character printing program for each print position is transferred for each character into a print control memory so that printing can proceed as though a large scale high speed computer was in charge of the printing process.

6 Claims, 11 Drawing Figures



United States Patent [19]

Ripley et al.

[11] **4,228,506**

[45] **Oct. 14, 1980**

[54] **CHARTER WITH AUTOMATIC EDITING**

[75] Inventors: **John A. Ripley**, Newport Beach; **Donald C. Woods**, Lompoc; **James Kaine**, Santa Ana, all of Calif.

[73] Assignee: **Del Mar Avionics**, Irvine, Calif.

[21] Appl. No.: **959,091**

[22] Filed: **Nov. 9, 1978**

[51] **Int. Cl.**[3] **G06F 3/05**

[52] **U.S. Cl.** **364/415**; 364/575; 364/900

[58] **Field of Search** 364/445, 447, 421, 422, 364/900, 200, 519-520, 572, 574, 575

[56] **References Cited**

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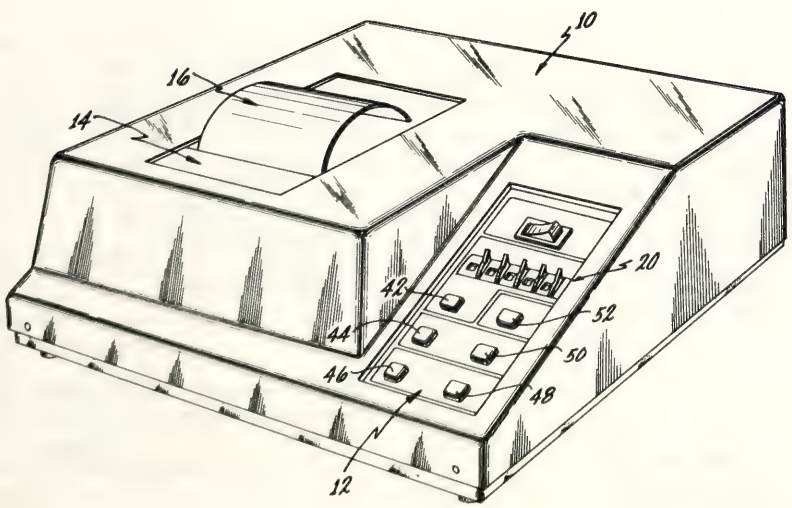
4,053,951	10/1977	Hudspeth, et al.	364/415
4,070,708	1/1978	Smallcombe et al.	364/575
4,110,730	8/1978	Varecka et al.	364/574 X

Primary Examiner—Edward J. Wise
Attorney, Agent, or Firm—Smyth, Pavitt, Siegemund, Jones & Martella

[57] **ABSTRACT**

An intelligent printer-plotter for use with a source of time-correlated digital systolic and diastolic blood pressure data and heart rate data receives, stores, analyzes, and edits the data, producing tables of data and graphs having a particular format. The charter smooths the data by a moving average technique and includes modes which permit the operator to edit the data manually or to command the charter to perform the editing automatically. In the automatic editing mode, the data are tested against pre-established criteria. Data not meeting the criteria is flagged so that it can be passed over in subsequent calculation and printing operations; however, the flagged data is not destroyed, but is retained in a memory to permit subsequent re-examination and to permit verification of the editing process.

9 Claims, 23 Drawing Figures



United States Patent [19]

Moshier

[11] **4,228,498**

[45] **Oct. 14, 1980**

[54] **MULTIBUS PROCESSOR FOR INCREASING EXECUTION SPEED USING A PIPELINE EFFECT**

[75] Inventor: **Stephen L. Moshier**, Cambridge, Mass.

[73] Assignee: **Dialog Systems, Inc.**, Belmont, Mass.

[21] Appl. No.: **841,390**

[22] Filed: **Oct. 12, 1977**

[51] **Int. Cl.**[2] **G06F 15/20**; G06F 15/34

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** ..... 364/200 MS File; 179/1 SA

[56] **References Cited**

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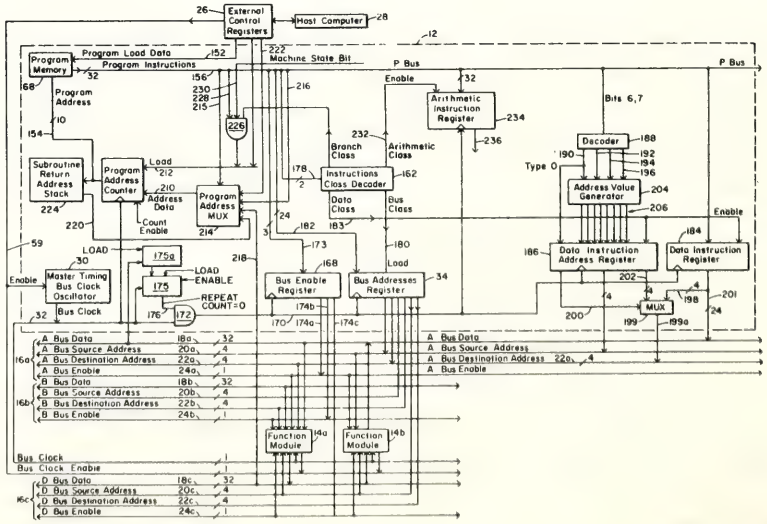
3,462,742	8/1969	Miller et al.	364/200
3,938,098	2/1976	Garlic	364/200
4,060,848	11/1977	Hyatt	364/200

Primary Examiner—Harvey E. Springborn
Attorney, Agent, or Firm—Kenway & Jenney

[57] **ABSTRACT**

A computing apparatus having at least three buses and a plurality of elementary function modules in circuit connection therewith, provides increased execution speed by implementing a pipeline effect. Each module is connected to at least one of the buses and at least one of the modules is connected to at least three of the buses. The buses each comprise a plurality of individual lines organized into groups: a group of source address lines, a group of destination address lines, and a group of data carrying lines. A control element is connected to each of the buses for directing the operation of the apparatus and the control element places source and destination addresses on the bus source address and destination address lines respectively for effectively connecting or configuring the function modules according to a selected program controlled configuration. The apparatus is useful in carrying out a plurality of machine operations during a single machine instruction cycle.

16 Claims, 6 Drawing Figures



United States Patent [19]

Boyd

[11] **4,203,153**

[45] **May 13, 1980**

[54] **CIRCUIT FOR REDUCING POWER CONSUMPTION IN BATTERY OPERATED MICROPROCESSOR BASED SYSTEMS**

[75] Inventor: **James C. Boyd**, Canton, Ohio

[73] Assignee: **Diebold, Incorporated**, Canton, Ohio

[21] Appl. No.: **895,771**

[22] Filed: **Apr. 12, 1978**

[51] **Int. Cl.**[2] **G06F 3/00**

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** ... 364/200 MS File, 900 MS File; 365/226, 227, 228, 229

[56] **References Cited**

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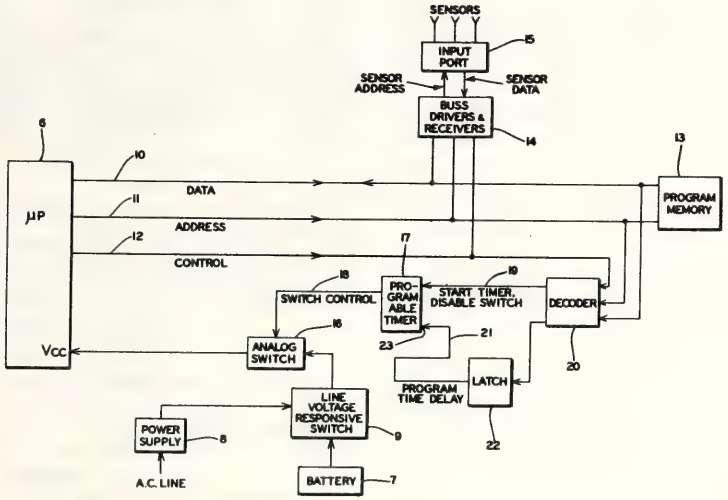
3,955,185	5/1976	Nishimura	340/324 R
3,969,703	7/1976	Kwiatkowski et al.	364/900
4,051,326	9/1977	Badagnani et al.	364/900
4,093,997	6/1978	Germer	364/900

Primary Examiner—Gareth D. Shaw
Assistant Examiner—E. Chan
Attorney, Agent, or Firm—Frease & Bishop

[57] **ABSTRACT**

In a microprocessor based system, wherein at least one microprocessor is battery powered, a power strobe circuit includes an analog switch for connecting the battery to the microprocessor only during programmed task performance. Upon completion of task performance, the microprocessor generates signals which trigger the analog switch to open, thereby deenergizing the microprocessor and to enable an external timer. After a predetermined period of time, which may be fixed in the timer or programmed, the timer causes the switch to reclose, thereby energizing the microprocessor for performance of another programmed task.

8 Claims, 3 Drawing Figures



United States Patent [19]

Lewine et al.

[11] **4,231,089**

[45] **Oct. 28, 1980**

[54] **DATA PROCESSING SYSTEM WITH APPARATUS FOR CORRECTING MICROINSTRUCTION ERRORS**

[75] Inventors: **Donald A. Lewine; Thomas M. Dundon**, both of Marlborough; **Ronald J. Setera**, Leominster, all of Mass.

[73] Assignee: **Digital Equipment Corporation**, Maynard, Mass.

[21] Appl. No.: **969,956**

[22] Filed: **Dec. 15, 1978**

[51] **Int. Cl.**[3] **G06F 11/16**

[52] **U.S. Cl.** **364/200**; 371/10

[58] **Field of Search** ... 364/200 MS File, 900 MS File, 364/200, 900; 235/303.1, 307; 371/10

[56] **References Cited**

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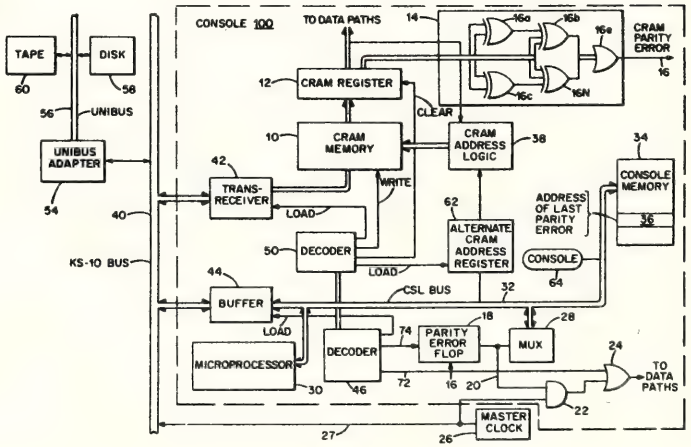
Primary Examiner—Raulfe B. Zache
Attorney, Agent, or Firm—Cesari & McKenna

[57] **ABSTRACT**

In a data processing system, a method and apparatus which enable an erroneous microinstruction word to be rewritten before it is executed. After the microinstruction word is written from memory into a control register, a parity network coupled to the control register determines whether a correct microinstruction is being executed. Upon a parity error being detected, the clock pulses to the data paths coupled to the control register are inhibited. The original microinstruction word is then fetched from secondary storage and rewritten into the microinstruction memory with the aid of a separate register providing the address to the microinstruction memory. Upon rewriting the microinstruction memory, the signal inhibiting the clock pulses is removed thereby allowing a new microinstruction to be executed. An additional feature includes apparatus for determining whether an error has previously occurred for the same microinstruction word, in which case a critical fault occurs and remedial maintenance is necessary.

10 Claims, 2 Drawing Figures



United States Patent [19]

Rapp et al.

[11] **4,199,814**

[45] **Apr. 22, 1980**

[54] **COMPUTER NUMERICAL CONTROL MACHINE TOOL**

[75] Inventors: **Edward J. Rapp**, Cleveland Heights; **Glen A. Johnson**, Cleveland, both of Ohio

[73] Assignee: **Digitcom, Inc.**, Mentor, Ohio

[21] Appl. No.: **841,597**

[22] Filed: **Oct. 12, 1977**

[51] **Int. Cl.**[2] **G06F 15/46; G05B 19/18**

[52] **U.S. Cl.** **364/474;** 318/568; 318/573; 318/574; 364/107; 364/120; 364/900

[58] **Field of Search** ..... 364/474, 475, 107, 114, 364/115, 120, 200 MS File, 900 MS File; 318/568, 569, 570, 572, 573, 571, 574, 685, 696

[56] **References Cited**

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4,060,851	11/1977	Nakatsukasa et al.	364/107 X
4,074,349	2/1978	Ueda	364/474 X
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"Numeripath CNC 800 Control Systems"—Giddings & Lewis Electronics Co., pp. 1-8, 1976.

Primary Examiner—Joseph F. Ruggiero

Attorney, Agent, or Firm—Fay & Sharpe

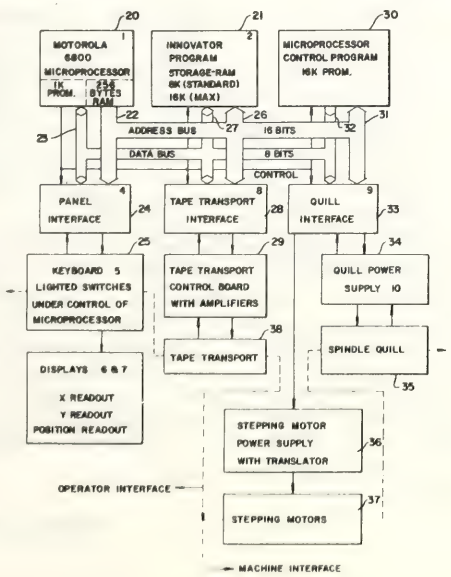
[57] **ABSTRACT**

This invention relates to a computer numerical control (CNC) machine tool system having a novel terminal controller and system therefor to control a machine tool generally with at least two axes and more probably three, with stepping motor controls for point-to-point positioning of the machine tool to an almost infinite variety of steps (generally not more than 200). The novelty resides in the ease of programming directly on the terminal controller of the CNC machine tool system. Generally at least some editing and offsets will be programmed from the machine tool.

The terminal controller consists of a microprocessor with some RAM and ROM, together with address and data bus plus I/O for magnetic tape handling and display for 6 to 8 digits in each of the X and Y positions, together with numeric keyboard for data input to the program steps and functional keys to control operation-automatic, manual and step-by-step, as well as controls for program input from tape to memory and memory to tape.

Particular features include the ease of inputting a program and preparing a tape and then editing the tape while in operation. Further features include circular and linear interpolation. For circular interpolation there are no quadrant limitations and a full or partial circle may be cut.

8 Claims, 14 Drawing Figures



United States Patent [19]

Verstegen

[11] **4,187,552**

[45] **Feb. 5, 1980**

[54] **READ ONLY MEMORY CHARACTER GENERATOR SYSTEM**

[75] Inventor: **Brian P. Verstegen**, Sunnyvale, Calif.

[73] Assignee: **Durango Systems, Inc.**, Cupertino, Calif.

[21] Appl. No.: **944,082**

[22] Filed: **Sep. 20, 1978**

[51] **Int. Cl.**[2] **B41J 3/50**

[52] **U.S. Cl.** **364/900;** 400/124

[58] **Field of Search** ... 364/200 MS File, 900 MS File; 400/124

[56] **References Cited**

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4,033,444	7/1977	Beery	400/124
4,109,777	8/1978	Ottenstein et al.	400/124

Primary Examiner—Mark E. Nusbaum

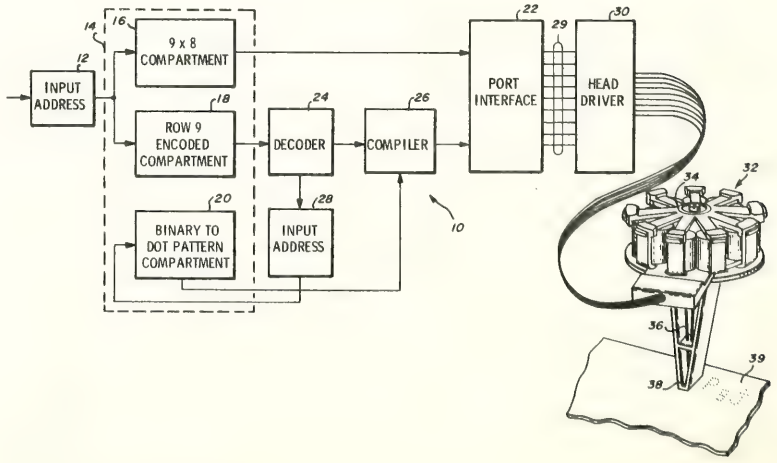
Assistant Examiner—C. T. Bartz

Attorney, Agent, or Firm—Thomas E. Schatzel

[57] **ABSTRACT**

A read only memory character generator system for generating dot print characters of a given font within a nine-column-by-nine-row dot matrix comprising a read only memory having a storage capacity of one byte per row of memory, the memory having a first memory means, a second memory means and a third memory means with the first memory means having nine memory row locations of memory storage devices for each character of the font to be printed, the memory storage devices at each successive row for each character being burned in pursuant to the dot matrix pattern for successive columns of dots of not more than eight rows for that given column of that given character, the second memory means having one memory row location of memory storage devices for each character of the font to be printed with the storage devices at each location being burned in pursuant to the dot matrix pattern for not more than six columns of dots for the ninth row of one of said characters and a binary code representation for the dot matrix pattern of the remaining columns of the ninth row dot matrix pattern for that particular character, and said third memory means having one memory row location of memory storage devices for each of said differing binary code representations with the storage devices at each location being burned in pursuant to the dot matrix pattern representation of one of said binary-coded representations.

7 Claims, 3 Drawing Figures



United States Patent [19]
Hansen et al.
[11] **4,231,096**
[45] **Oct. 28, 1980**

[54] **DIGITAL TYPESETTER**

[75] Inventors: **Walter I. Hansen**, Cold Spring Harbor; **Wiley E. Galbraith**, East Northport; **Louis C. Vella**, Selden; **Martin M. Cohen**, Scarsdale, all of N.Y.

[73] Assignee: **Eltra Corporation**, Toledo, Ohio

[21] Appl. No.: **950,242**

[22] Filed: **Oct. 10, 1978**

[51] **Int. Cl.**[3] **G06F 3/14**
[52] **U.S. Cl.** **364/523**; 340/730; 340/748; 354/7; 364/900
[58] **Field of Search** 364/200, 523, 900; 340/730, 748; 354/7

[56] **References Cited**

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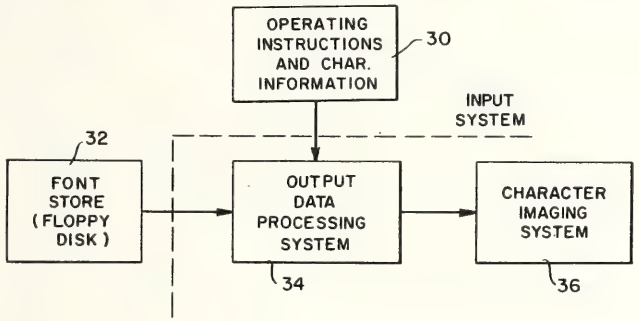
Primary Examiner—Jerry Smith
Attorney, Agent, or Firm—Joel I. Rosenblatt

[57] **ABSTRACT**

A digital typesetter for imaging graphics quality characters of a specified font. The typesetter includes an electronic data processing system which receives first digital data defining the identity, form, size and placement of characters to be typeset; receives second digital data defining the contour of each character to be typeset with respect to a normalized encoding set of first and second coordinates; and produces third digital data defining the character boundaries intersecting a raster (scan) line. This third digital data, for at least a portion of the raster line extending the width of several characters, is temporarily stored in a raster line storage buffer. A character imaging device, connected to the line storage buffer, is provided to image successive raster lines on a print medium. Drive means are also provided for moving the print medium in a direction transverse to the direction of the raster (scan) line.

44 Claims, 26 Drawing Figures



United States Patent [19]
Holsztynski et al.
[11] **4,215,401**
[45] **Jul. 29, 1980**

[54] **CELLULAR DIGITAL ARRAY PROCESSOR**

[75] Inventors: **Wlodzimierz Holsztynski; Stephen S. Wilson**, both of Ann Arbor, Mich.

[73] Assignee: **Environmental Research Institute of Michigan**, Ann Arbor, Mich.

[21] Appl. No.: **946,588**

[22] Filed: **Sep. 28, 1978**

[51] **Int. Cl.**[2] **G06F 7/00**
[52] **U.S. Cl.** ..... **364/200**; 340/146.3 MA; 364/515
[58] **Field of Search** ..... 340/146.3 H, 146.3 MA, 340/146.3 R; 364/200 MS File, 515, 900

[56] **References Cited**

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4,060,713	11/1977	Golay	340/146.3 MA
4,065,808	12/1977	Schomberg et al.	364/200

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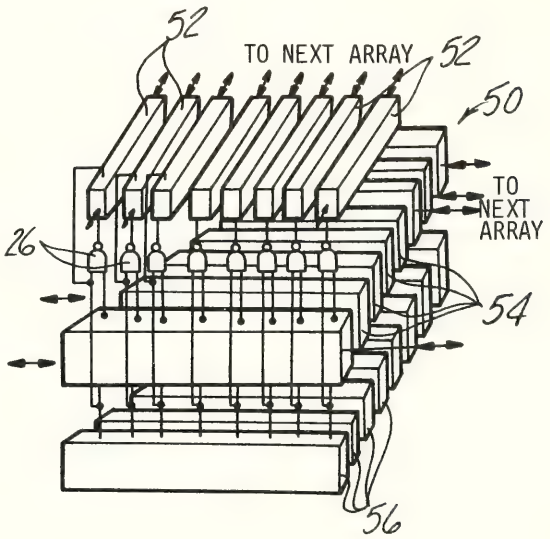
Duff et al., "A Cellular Logic Array for Image Processing", *Pattern Recognition*, vol. 5, pp. 229–247, Sep. 1973.

Primary Examiner—Leo H. Boudreau
Attorney, Agent, or Firm—Krass & Young

[57] **ABSTRACT**

A rectangular digital logic array for performing transformations on data matrices for solving wave equations, image processing problems and the like, includes a plurality of identical cells each having a processing element which receives one of its inputs from a single bit accumulator and provides its output to a similar single bit accumulator. The input accumulators of each row in the array are formed by a single parallel input, parallel output shift register and the output accumulators of each column in the array are similarly formed by a parallel input, parallel output shift register. The shift registers operate to connect each cell except those at the edge of the array with two neighboring cells along one axis and two neighboring cells along the orthogonal axis. Four edge shift registers bordering the array allow data to be transferred into and out of the cells and a central processor connected to each of the cells controls the sequence of cell operations and the transfer of data between cells for all cells simultaneously. The simple cell and interconnection structure allows the economical formation of large arrays so that very high processing speeds may be achieved despite the multiple processing steps which each elemental cell must undergo in order to perform a complex computation.

20 Claims, 7 Drawing Figures



United States Patent [19]

Nutter et al.

[11] **4,187,551**

[45] * **Feb. 5, 1980**

[54] **APPARATUS FOR WRITING DATA IN UNIQUE ORDER INTO AND RETRIEVING SAME FROM MEMORY**

[75] Inventors: **Geoffrey Nutter**, Cheadle; **William McGibbon**, Manchester, both of England

[73] Assignee: **Ferranti Limited**, England

[*] Notice: The portion of the term of this patent subsequent to Sep. 5, 1994, has been disclaimed.

[21] Appl. No.: **853,461**

[22] Filed: **Nov. 21, 1977**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 742,230, Nov. 16, 1976, Pat. No. 4,112,487.

[30] **Foreign Application Priority Data**

Nov. 21, 1975 [GB] United Kingdom 47988/75
Nov. 20, 1976 [GB] United Kingdom 48514/76

[51] **Int. Cl.**[2] **G06F 7/00**
[52] **U.S. Cl.** **364/900**
[58] **Field of Search** ... 364/200 MS File, 900 MS File

[56] **References Cited**

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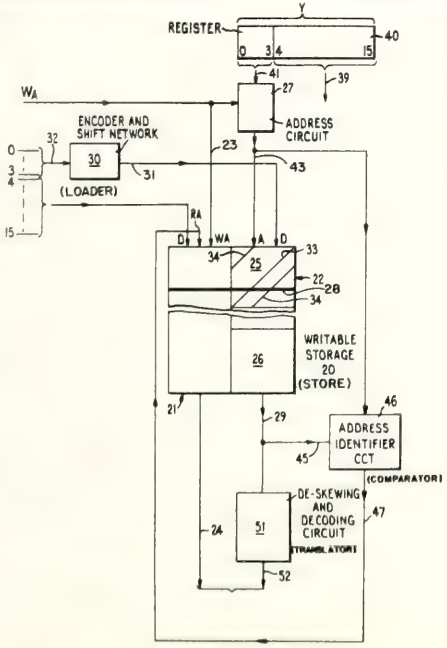
3,996,566	12/1976	Moran	364/200

Primary Examiner—Raulfe B. Zache
Attorney, Agent, or Firm—Cameron, Kerkam, Sutton, Stowell & Stowell

[57] **ABSTRACT**

Data processing apparatus includes a storage circuit or memory, and an addressing circuit for identifying word locations within the storage circuit or memory into and from which a plurality of information items are to be written and read, respectively. A translating circuit is provided for successively shifting, in a write mode of operation, at least a portion of each information item so that it is stored in the storage circuit in a manner that the stored information item in each word location has a bit order different from that order of any other information item as stored in the storage circuit. In a read mode of operation, the translating or de-skewing circuit shifts the information items as read out from the storage circuit in a direction opposite to that imparted during the writing mode.

18 Claims, 18 Drawing Figures



United States Patent [19]

Bowerman et al.

[11] **4,210,777**

[45] **Jul. 1, 1980**

[54] **PSEUDO-TRANSPARENT STOP BIT GENERATOR**

[75] Inventors: **John J. Bowerman**, Rock Ridge; **John F. Wilson**, Frederick, both of Md.

[73] Assignee: **Frederick Electronics Corp.**, Frederick, Md.

[21] Appl. No.: **915,725**

[22] Filed: **Jun. 15, 1978**

[51] **Int. Cl.**[2] **H04L 25/38**
[52] **U.S. Cl.** **375/117**; 364/200; 375/8
[58] **Field of Search** ..... 178/53.1 R, 53.1 A, 178/69.1, 15 BS

[56] **References Cited**

U.S. PATENT DOCUMENTS

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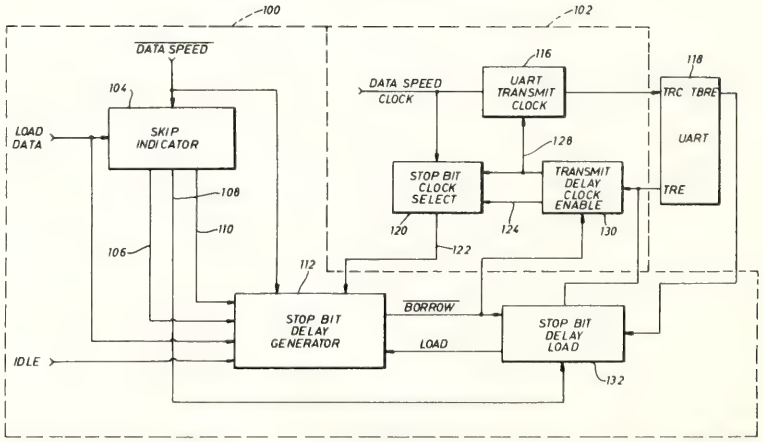
Primary Examiner—Benedict V. Safourek
Attorney, Agent, or Firm—Arnold, White & Durkee

[57] **ABSTRACT**

In a Telex switching system line terminator unit having means to transmit a character from the terminator to its terminal, in which the character is transmitted in a serial mode and terminated by a stop bit, an improvement in the manner of generating the stop bit is provided. A variable length stop bit is dynamically generated for each character transmitted such that the length of the stop bit is changed as the time required by the calling terminal to transmit the character to its terminator unit decreases over that required by the called terminator unit to transmit the character to the called terminal. Patterns in the rate of transfer of characters from the calling terminator unit to the called terminator unit are monitored to control the length of the stop bit.

23 Claims, 10 Drawing Figures



United States Patent [19]
Kobayashi et al.
[11] **4,229,804**
[45] **Oct. 21, 1980**

[54] **NUMERICAL CONTROL UNIT HAVING A CASSETTE TYPE MEMORY**

[75] Inventors: **Kengo Kobayashi**, Kawasaki; **Ryoji Imazeki**, Hachioji, both of Japan

[73] Assignee: **Fujitsu Fanuc Limited**, Hino, Japan

[21] Appl. No.: **808,398**

[22] Filed: **Jun. 20, 1977**

[30] **Foreign Application Priority Data**

Jun. 28, 1976 [JP] Japan 51-76140
Jun. 28, 1976 [JP] Japan 51-76141

[51] **Int. Cl.**[2] **G06F 13/00**; G05B 19/18
[52] **U.S. Cl.** **364/900**; 364/474
[58] **Field of Search** ... 364/900 MS File, 200 MS File, 364/474, 107, 118; 318/568; 365/229

[56] **References Cited**

U.S. PATENT DOCUMENTS

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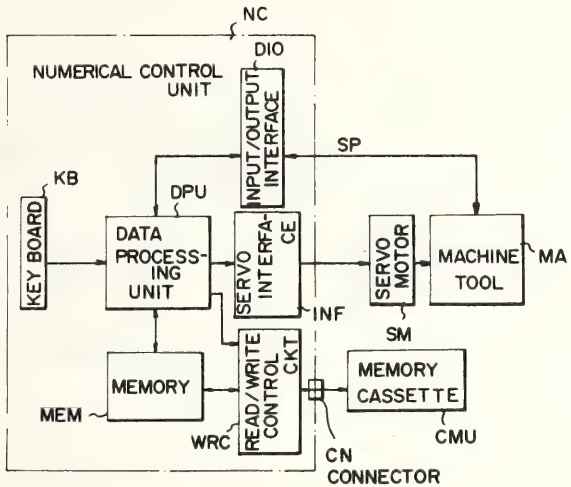
3,859,638 1/1975 Hume, Jr. 365/229
3,924,110 12/1975 Cochran et al. 364/900

Primary Examiner—Raulfe B. Zache
Attorney, Agent, or Firm—Staas & Halsey

[57] **ABSTRACT**

A numerical control unit in which command data is inputted from a keyboard and stored in an internal memory and which controls a machine tool based on the stored command data. A cassette type memory is constructed to be detachably mounted on the numerical control unit. When the cassette type memory is mounted on the numerical control unit, the command data can be transmitted between the cassette type memory and the internal memory and stored therein and even when the cassette type memory is removed from the numerical control unit, the stored content can be retained. By repeatedly reading out the command data stored in the cassette type memory, the machine tool can be controlled.

4 Claims, 18 Drawing Figures



United States Patent [19]
Motz
[11] **4,231,091**
[45] **Oct. 28, 1980**

[54] **ENGINE CONTROL SYSTEM**

[75] Inventor: **Phillip R. Motz**, Kokomo, Ind.

[73] Assignee: **General Motors Corporation**, Detroit, Mich.

[21] Appl. No.: **963,693**

[22] Filed: **Nov. 27, 1978**

[51] **Int. Cl.**[3] **G05B 15/00**; H03K 3/017; F02B 5/00
[52] **U.S. Cl.** **364/431**; 364/569; 364/900; 123/414; 123/417
[58] **Field of Search** ..... 364/424, 431, 442, 569; 123/32 EA, 32 EC, 117 R, 117 D

[56] **References Cited**

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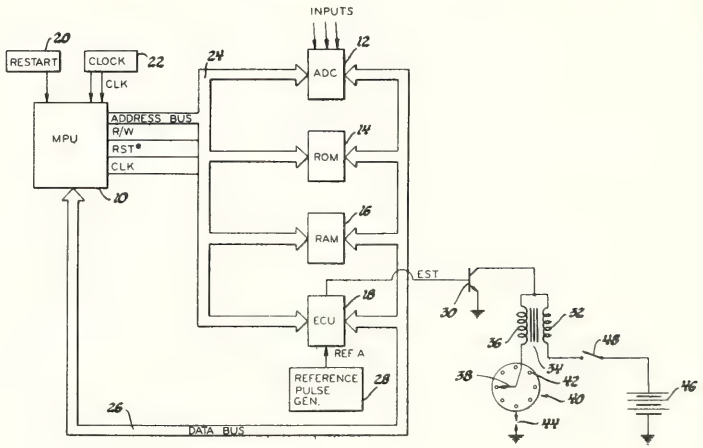
4,052,967 10/1977 Colling et al. ..... 123/117 D
4,143,622 3/1979 Klötzner et al. ..... 173/32 EC
4,157,699 6/1979 Mori ..... 123/117 D

Primary Examiner—Felix D. Gruber
Attorney, Agent, or Firm—Albert F. Duke

[57] **ABSTRACT**

An engine control system includes a microprocessor responsive to engine operating parameters for developing control words representing a desired dwell and firing time for use in controlling engine spark timing. An engine control unit is coupled to the microprocessor and utilizes the control words in calculating the desired rise and fall of the spark timing output relative to reference pulses, indicative to engine crankshaft position. The engine control unit includes a free-running counter which serves as a time reference for determining the period of the input reference pulses and for predicting the time of rise and fall of the output. Prediction of the next rise is made when the output falls and prediction of next fall is made when the output rises. Predictions are made on the assumption of constant frequency reference pulses. Errors resulting from this assumption are corrected when a reference pulse occurs.

5 Claims, 4 Drawing Figures



United States Patent [19]

Sibley

[11] **4,181,849**

[45] **Jan. 1, 1980**

[54] **VITAL RELAY DRIVER HAVING CONTROLLED RESPONSE TIME**

[75] Inventor: **Henry C. Sibley**, Adams Basin, N.Y.

[73] Assignee: **General Signal Corporation**, Stamford, Conn.

[21] Appl. No.: **873,574**

[22] Filed: **Jan. 30, 1978**

[51] **Int. Cl.**[2] **G07C 11/00**

[52] **U.S. Cl.** ..... **235/92 T**; 235/92 DP; 307/116; 364/900

[58] **Field of Search** ..... 361/197; 307/293, 116; 364/200 MS File, 900 MS File; 235/92 T, 92 ST, 92 PD, 92 DP, 92 CT

[56] **References Cited**

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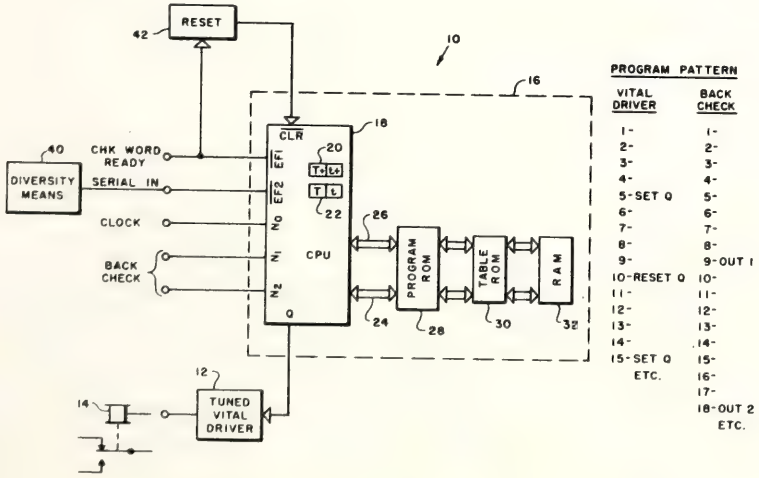
3,566,368	2/1971	De Blauw	364/200
3,723,975	3/1973	Kurtz et al.	364/900

Primary Examiner—Joseph M. Thesz
Attorney, Agent, or Firm—Milton E. Kleinman

[57] **ABSTRACT**

A vital relay driver whose response time can be readily controlled such that the release time of the relay may be varied, yet may be held to very close tolerances. The vital relay driver is controlled by a microprocessor dedicated to this function, such processor generating a dynamic signal of fixed frequency in dependence on a cycle number which is continually replenished; otherwise the microprocessor stops producing the dynamic signal and the relay is released in a closely known time.

6 Claims, 4 Drawing Figures



United States Patent [19]

Albani et al.

[11] **4,198,682**

[45] **Apr. 15, 1980**

[54] **SYMPTOM COMPRESSION DEVICE**

[75] Inventors: **Alfonso Albani**, Bollate; **Ermanno Maccario**, Pregnana Milanese, both of Italy

[73] Assignee: **Honeywell Information Systems Italia**, Milan, Italy

[21] Appl. No.: **863,463**

[22] Filed: **Dec. 22, 1977**

[30] **Foreign Application Priority Data**

Dec. 31, 1976 [IT] Italy 31040 A/76

[51] **Int. Cl.**[2] **G06F 5/00**

[52] **U.S. Cl.** ..... **364/900**; 340/347 DD

[58] **Field of Search** ..... 235/302.1; 328/37; 307/216; 364/200 MS File, 900 MS File, 200, 900; 340/347 DD

[56] **References Cited**

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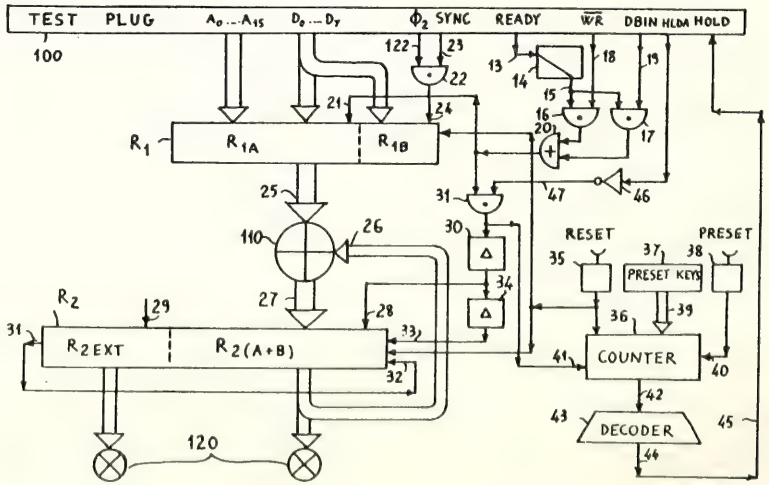
"A Deductive Method for Simulating Faults in Logic Circuits", Armstrong, Bell Telephone Laboratories, May 71.

Primary Examiner—Gareth D. Shaw
Assistant Examiner—E. Chan

[57] **ABSTRACT**

A symptom compression device receives binary coded information including bits signifying symptoms present in the course of each operating cycle at selected points in an integrated logical network, microprocessor or the like. The device includes a first register, a second shift register, an EXCLUSIVE OR logic network, and a display. The binary coded information is received on parallel inputs of the first register and applied from parallel outputs of the first register to a set of inputs of the EXCLUSIVE OR network, a second set of inputs which is connected to at least some parallel outputs from the second shift register. A set of outputs from the EXCLUSIVE OR network is connected to parallel inputs of the second shift register. In each cycle, the bits in the second shift register, which accumulate information representative of symptoms, are shifted in one direction and are recirculated. The display is connected to the parallel outputs from the second shift register. In a second embodiment, a third shift register receives the output from the EXCLUSIVE OR network. A multiplexor selectively applies signals from the outputs of the second or third shift register to the second set of inputs. The bits in the third shift register, which also accumulate information as to symptoms, are shifted in the opposite direction. A second display is connected to the outputs of the third shift register.

7 Claims, 4 Drawing Figures



United States Patent [19]
Muzzani et al.
[11] **4,204,254**
[45] **May 20, 1980**

[54] **ELECTRONIC COMPUTER INCLUDING AN INFORMATION REFRESHING ARRANGEMENT**

[75] Inventors: **Aldo Muzzani; Ilio Paccapelo**, both of Ivrea, Italy

[73] Assignee: **Ing. C. Olivetti & C., S.p.A.**

[21] Appl. No.: **907,490**

[22] Filed: **May 19, 1978**

[30] **Foreign Application Priority Data**

May 25, 1977 [IT] Italy 68191 A/77

[51] **Int. Cl.**[2] **G06F 13/02**; G06F 9/16
[52] **U.S. Cl.** **364/200**; 365/222
[58] **Field of Search** ... 364/200 MS File, 900 MS File; 365/222

[56] **References Cited**

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4,084,154	4/1978	Panigrahi	364/900

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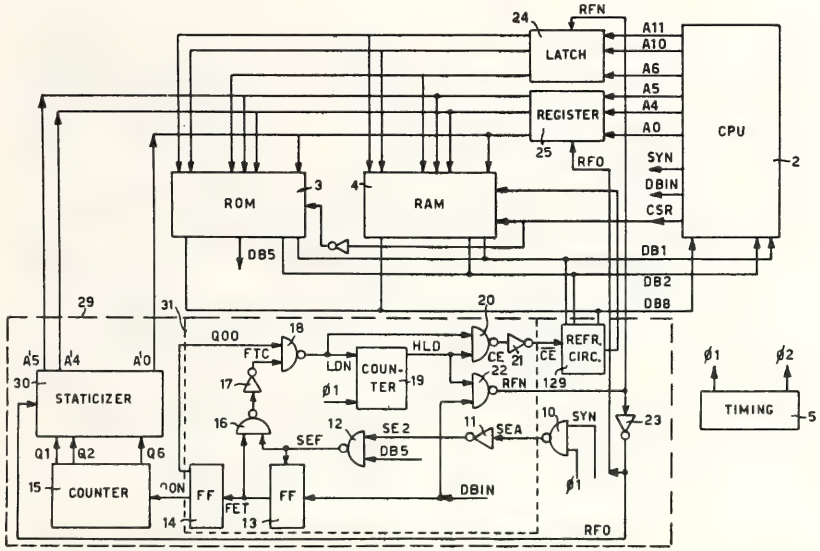
Primary Examiner—James D. Thomas
Attorney, Agent, or Firm—Schuyler, Birch, McKie & Beckett

[57] **ABSTRACT**

The operative memory of the computer is of the MOS type and is cyclically refreshed under the control of logic circuits, in turn controlled by the timing unit during the microinstructions decoding. Particularly, every machine cycle in which an odd microinstruction is fetched, a row of memory locations is addressed for being refreshed during the same cycle, before the next following machine cycle is started, thus preventing any overlapping of refreshing operation with the CPU operation on the memory.

4 Claims, 3 Drawing Figures



United States Patent [19]
Faulkner et al.
[11] **4,217,637**
[45] **Aug. 12, 1980**

[54] **DATA PROCESSING UNIT WITH TWO CLOCK SPEEDS**

[75] Inventors: **Trevor L. Faulkner**, Wilmslow; **Barry M. Hall**, Grantham, both of England

[73] Assignee: **International Computers Limited**, London, England

[21] Appl. No.: **894,852**

[22] Filed: **Apr. 10, 1978**

[30] **Foreign Application Priority Data**

Apr. 20, 1977 [GB] United Kingdom 16380/77

[51] **Int. Cl.**[2] **G06F 1/04**; G06F 9/02; G06F 5/06
[52] **U.S. Cl.** **364/200**
[58] **Field of Search** ... 364/200 MS File, 900 MS File; 340/691

[56] **References Cited**

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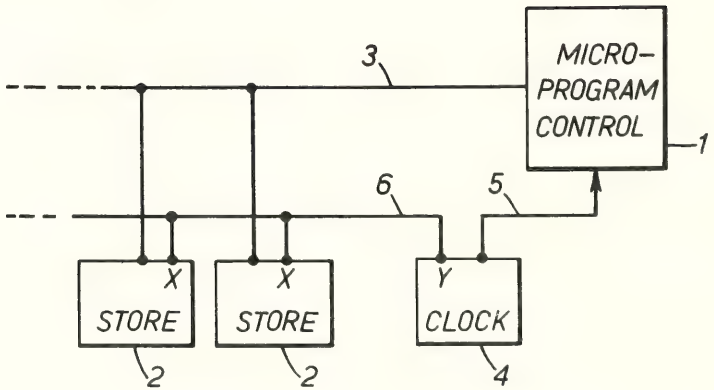
Primary Examiner—Gareth D. Shaw
Assistant Examiner—E. Chan
Attorney, Agent, or Firm—Hane, Roberts, Spiecens & Cohen

[57] **ABSTRACT**

A data processing unit in which the clock speed is selected to match the access times of the store units connected to it. This is achieved by means of a special terminal on each store unit, this terminal being internally grounded if the unit is of a slow access type, and open-circuited if the unit is of a fast access type.

2 Claims, 4 Drawing Figures



United States Patent [19]

Pfeifer

[11] **4,228,519**

[45] **Oct. 14, 1980**

[54] **MONITORING METHOD AND SYSTEM FOR A PARKING LOT**

[75] Inventor: **Heinrich Pfeifer,** Villingen-Schwenningen, Fed. Rep. of Germany

[73] Assignee: **Kienzle Apparate GmbH,** Villingen, Fed. Rep. of Germany

[21] Appl. No.: **948,407**

[22] Filed: **Oct. 4, 1978**

[30] **Foreign Application Priority Data**

Oct. 5, 1977 [DE] Fed. Rep. of Germany 2744768

[51] **Int. Cl.**[3] **G07C 1/30**

[52] **U.S. Cl.** ..... **364/900;** 58/141; 194/DIG. 22; 235/92 T; 340/51

[58] **Field of Search** ..... 340/51; 58/141, 142, 58/143; 194/DIG. 21, DIG. 22; 235/92 T, 92 TC; 364/900 MS File, 200 MS File

[56] **References Cited**

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3,998,307	12/1976	Kolben et al.	194/DIG. 22
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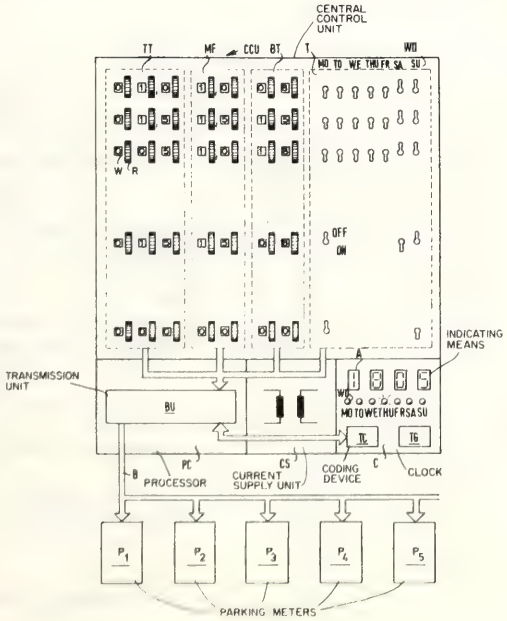
4,031,991	6/1977	Malott	340/51

Primary Examiner—Leo H. Boudreau
Attorney, Agent, or Firm—Toren, McGeady and Stanger

[57] **ABSTRACT**

A method for electronically monitoring parking lots and an electronic monitoring system for carrying out such method are disclosed. The method and system employs the use of a central control unit and a plurality of parking meters connected to the central control unit. The central control unit generates the time of day which is sent to and electronically stored in each parking meter. Depending on the number of coins inserted in a meter, an amount of time corresponding to the coins is calculated based on a given tariff. This time is added to the time of day to determine a time of departure. This time is indicated on indicating means provided at each meter. The actual time of day and the paid-for parking time are repeatedly compared until they are equal. At that time, the indicating means is cleared. A microprocessor, a variable storage element and a fixed storage element are provided at each meter to effect the necessary calculations and storage required. Additional features are also disclosed.

15 Claims, 2 Drawing Figures



United States Patent [19]

Levy

[11] **4,218,760**

[45] **Aug. 19, 1980**

[54] **ELECTRONIC DICTIONARY WITH PLUG-IN MODULE INTELLIGENCF**

[75] Inventor: **Michael Levy,** Plantation, Fla.

[73] Assignee: **Lexicon,** Miami, Fla.

[21] Appl. No.: **941,050**

[22] Filed: **Sep. 11, 1978**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 848,527, Nov. 3, 1977, Pat. No. 4,158,236, which is a continuation-in-part of Ser. No. 723,049, Sep. 13, 1976, abandoned.

[51] **Int. Cl.**[2] **G06F 15/02;** G06F 15/38

[52] **U.S. Cl.** ..... **364/900;** 364/419; 35/35 R

[58] **Field of Search** ... 364/200 MS File, 900 MS File, 364/419, 706; 35/6, 8 R, 35 R, 9 B; 340/711, 782, 798; 400/109

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4,075,679	2/1978	Christopher et al.	364/200
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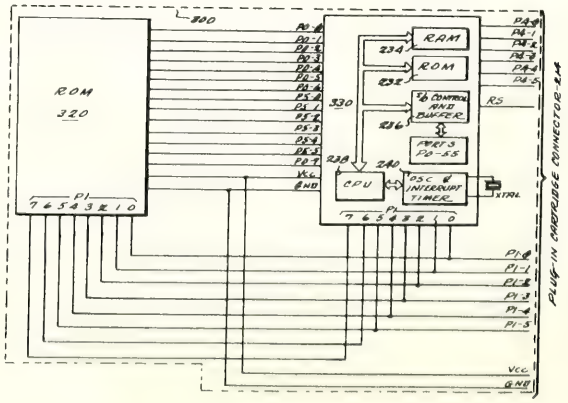
1448211	9/1976	United Kingdom 364/900
1492376	11/1977	United Kingdom .

Primary Examiner—Mark E. Nusbaum
Attorney, Agent, or Firm—Cushman, Darby & Cushman

[57] **ABSTRACT**

A portable electronic dictionary in a hand-held housing which mounts a plurality of alpha-numeric displays and a keyboard. A plug-in module contains a microcomputer and a ROM which stores a plurality of pairs of sequences of alpha-numeric characters and is searched by a central processing unit in the microcomputer under instructions stored as firmware in another ROM forming part of the microcomputer. One sequence of each stored pair is compared with a sequence which is entered into the keyboard and stored in a RAM also forming part of the microcomputer until a match is found. After one or more sequences have been entered into the keyboard and locations of matching pairs are stored in the microcomputer RAM, the pairs of stored sequences can be rolled across the display. Either sequence of each pair can be compared with a sequence entered into the keyboard.

12 Claims, 17 Drawing Figures



United States Patent [19]
Gunawardena
[11] **4,212,058**
[45] **Jul. 8, 1980**

[54] **COMPUTER STORE MECHANISM**

[75] Inventor: **Jaya A. Gunawardena**, Peradeniya, Sri Lanka

[73] Assignee: **National Research Development Corporation**, London, England

[21] Appl. No.: **834,872**

[22] Filed: **Sep. 20, 1977**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 726,162, Sep. 24, 1976, abandoned.

[30] **Foreign Application Priority Data**

Sep. 27, 1975 [GB] United Kingdom 39647/75

[51] **Int. Cl.**[2] **G11C 9/00; G06F 13/00**
[52] **U.S. Cl.** **364/200**
[58] **Field of Search** ... 364/200 MS File, 900 MS File

[56] **References Cited**

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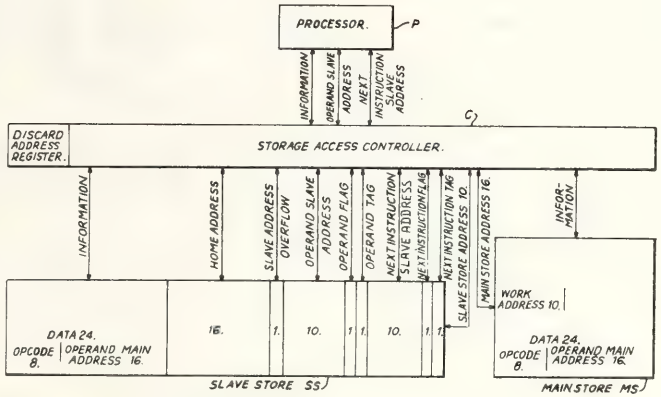
Primary Examiner—Gareth D. Shaw
Assistant Examiner—C. T. Bartz
Attorney, Agent, or Firm—Cushman, Darby & Cushman

[57] **ABSTRACT**

In a computer system having two levels of memory, a random access memory is used as a slave store for both code and directly addressed data. Each slave store word includes two slave address fields, one for the slave address of an operand and the other for the slave address of the next instruction. Validation means are provided to determine whether the word at such a slave address has been overwritten since the slave address was recorded.

13 Claims, 10 Drawing Figures



United States Patent [19]
Sukonick et al.
[11] **4,197,590**
[45] **Apr. 8, 1980**

[54] **METHOD FOR DYNAMICALLY VIEWING IMAGE ELEMENTS STORED IN A RANDOM ACCESS MEMORY ARRAY**

[75] Inventors: **Josef S. Sukonick**, Cupertino; **Greg J. Tilden**, San Jose, both of Calif.

[73] Assignee: **NuGraphics, Inc.**, Cupertino, Calif.

[21] Appl. No.: **870,822**

[22] Filed: **Jan. 19, 1978**

Related U.S. Application Data

[62] Division of Ser. No. 650,372, Jan. 19, 1976, Pat. No. 4,070,710.

[51] **Int. Cl.**[2] **G06F 3/14**
[52] **U.S. Cl.** **364/900**; 340/721; 340/726; 340/731; 340/747; 340/750; 340/792; 340/799
[58] **Field of Search** ... 364/200 MS File, 900 MS File, 364/514, 515; 340/324 AD, 721, 723, 724, 731, 726, 747, 750, 792, 799

[56] **References Cited**

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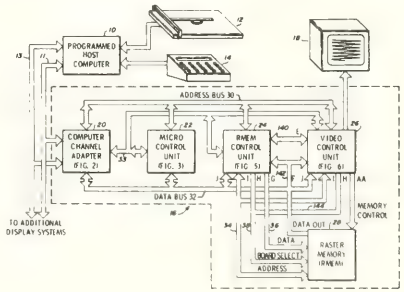
Aydin Controls Data Sheet for the Model 5214A Display Generator.

Primary Examiner—Mark E. Nusbaum
Assistant Examiner—Thomas M. Heckler
Attorney, Agent, or Firm—Spensley, Horn, Jubas & Lubitz

[57] **ABSTRACT**

A computer graphics display system including random access raster memory for storing data to be displayed, a raster memory control unit for writing data into the raster memory, a video control unit for causing such information to be displayed on a CRT display screen, a micro control unit for controlling the function and timing of the raster memory control unit and the video control unit, and a computer adapted for facilitating data exchange between the micro control unit and a host computer. The displayed image can have extremely high complexity with essentially no problem of display flicker. Zoom and pan features allow the use of a very complex stored image in a flexible manner, and a split-screen technique enables an operator to work on a very complex picture at a detail level while still having an overview of the total picture, or any portion thereof, simultaneously presented before him. The split-screen feature also allows the simultaneous display of alphanumeric messages such as prompts, menus, or X-Y readouts added to the graphics display and a small area of the raster memory is usually reserved for this purpose. An XOR feature allows a selective erase that restores lines crossing or concurrent with erased lines. The XOR feature permits part of the drawing to be moved or "dragged" into place without erasing other parts of the drawing.

16 Claims, 21 Drawing Figures



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United States Patent [19]
Sano et al.
[11] **4,225,779**
[45] **Sep. 30, 1980**

[54] **BANKING APPARATUS AND METHOD**

[75] Inventors: **Jyunji Sano**, Ohtsu; **Kuniaki Okazaki**, Moriyama, both of Japan

[73] Assignee: **Omron Tateisi Electronics Co.**, Kyoto, Japan

[21] Appl. No.: **912,739**

[22] Filed: **Jun. 5, 1978**

[30] **Foreign Application Priority Data**

Jun. 10, 1977 [JP] Japan 52/69234
Jun. 10, 1977 [JP] Japan 52/69235

[51] **Int. Cl.**[3] **G06K 17/00**; G06F 15/30
[52] U.S. Cl. **235/379**; 364/900
[58] **Field of Search** ... 364/900 MS File, 200 MS File, 364/408; 235/379; 340/149 A, 152 R

[56] **References Cited**

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FOREIGN PATENT DOCUMENTS

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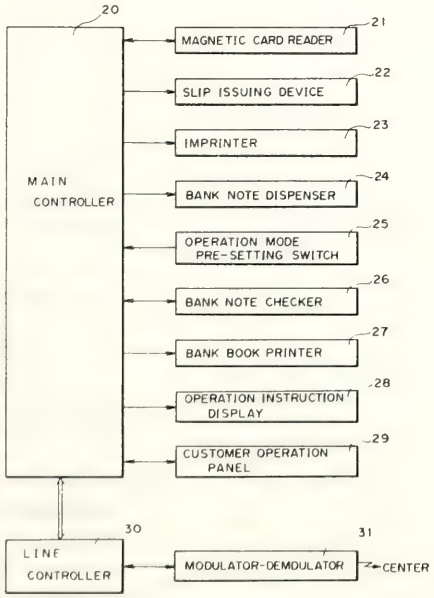
Primary Examiner—Raulfe B. Zache
Attorney, Agent, or Firm—Stevens, Davis, Miller & Mosher

[57] **ABSTRACT**

Banking apparatus comprising a plurality of transaction devices having at least one common operative device, means for presetting a pattern of transactions representing a combination of transactions processable according to a status of the transaction devices, means connected with the means for presetting the pattern of transactions for generating a first predetermined signal pattern, means for entering a customer selected transaction into the apparatus, means connected with the means for entering for generating a second predetermined signal, means for checking for the presence or absence of a predetermined relation between the first and second predetermined signal patterns and for judging whether a customer selected transaction is available and means for executing a customer selected transaction which has been judged to be available by the judging means.

13 Claims, 7 Drawing Figures



United States Patent [19]
Strunc
[11] **4,214,310**
[45] **Jul. 22, 1980**

[54] **MANAGEMENT DATA SYSTEM FOR PRINT SORTER**

[75] Inventor: **Gerald R. Strunc**, Maple Grove, Minn.

[73] Assignee: **Pako Corporation**, Minneapolis, Minn.

[21] Appl. No.: **949,694**

[22] Filed: **Oct. 10, 1978**

[51] **Int. Cl.**[2] **G06M 3/06**
[52] **U.S. Cl.** ..... **364/475**; 235/92 PD; 355/13; 364/478; 364/900
[58] **Field of Search** ..... 364/900, 475, 525, 401–403, 364/471, 478; 235/92 SB, 92 PD, 92 PE, 92 EA; 355/13, 14, 16, 28, 29; 83/926 J

[56] **References Cited**

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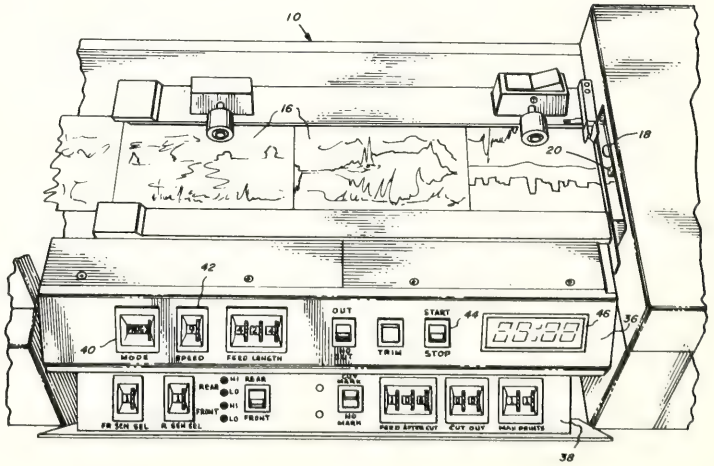
3,947,109 3/1976 Kinder et al. 355/29
4,123,649 10/1978 Strunc ..... 235/92 PD

Primary Examiner—Errol A. Krass
Attorney, Agent, or Firm—Kinney, Lange, Braddock, Westman and Fairbairn

[57] **ABSTRACT**

A management data system is used in conjunction with a photographic print cutting and sorting system. First and second storage means store two sets of data for each of a plurality of operators and printers. The two sets of data are independently resettable so that they reflect totals or percentages over two different time periods (for example, daily and monthly totals or percentages). A portable data retrieval device selects the particular operator or printer data from the two sets of data and displays operator totals, operator rates, printer totals or printer percentages based upon either the first or second set of data.

17 Claims, 4 Drawing Figures



United States Patent [19]

Sellner

[11] **4,224,600**

[45] **Sep. 23, 1980**

[54] **ARRAYS FOR PARALLEL PATTERN RECOGNITION**

[75] Inventor: **Harvey R. Sellner**, Newtown, Conn.

[73] Assignee: **The Perkin-Elmer Corporation**, Norwalk, Conn.

[21] Appl. No.: **23,984**

[22] Filed: **Mar. 26, 1979**

[51] **Int. Cl.**[2] **G06K 9/12**

[52] **U.S. Cl.** ..... **340/146.3 MA**; 364/200; 364/515

[58] **Field of Search** ..... 364/515, 416, 200 MS File, 364/900 MS File; 340/146.3 MA, 146.3 H, 146.3 F, 146.3 R

[56] **References Cited**

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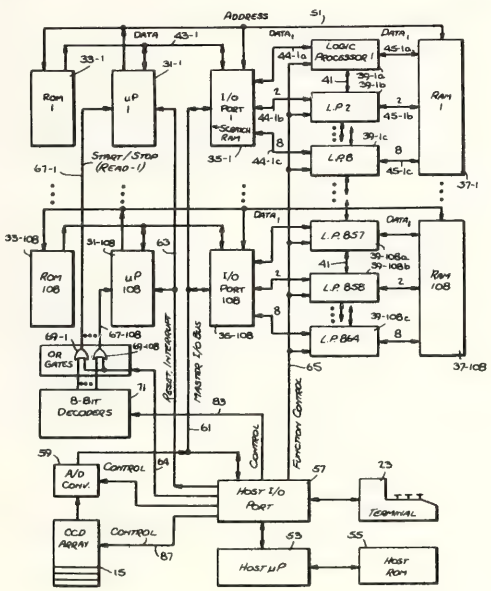
Primary Examiner—Leo H. Boudreau

Attorney, Agent, or Firm—Salvatore A. Giarratana; Francis L. Masselle; Edwin T. Grimes

[57] **ABSTRACT**

In order to perform pictorial pattern recognition at an extremely high data rate, a linear array of photodetectors reads information recorded on photograhic film and the data read is transferred sequentially to an array of microprocessors, converted into binary form and stored in the memories. The microprocessors operating in conjunction with transformation logic then perform successive transformations using an analysis technique, known in the art, which utilizes hexagonal surrounds.

13 Claims, 14 Drawing Figures



United States Patent [19]

Fedida et al.

[11] **4,193,121**

[45] **Mar. 11, 1980**

[54] **INFORMATION HANDLING APPARATUS HAVING MULTIPLE PORTS DISTRIBUTED AROUND SHIFTING REGISTER RINGS**

[75] Inventors: **Samuel Fedida; Desmond J. Sargent**, both of Felixstowe, England

[73] Assignee: **Post Office**, London, England

[21] Appl. No.: **814,921**

[22] Filed: **Jul. 12, 1977**

[30] **Foreign Application Priority Data**

Jul. 16, 1976 [GB] United Kingdom 29739/76

[51] **Int. Cl.**[2] **G06F 13/02**; G06F 3/00

[52] **U.S. Cl.** **364/900**; 365/78

[58] **Field of Search** ..... 365/78; 364/900 MS File, 200

[56] **References Cited**

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3,967,263	6/1976	Chang	364/900
4,027,288	5/1977	Barton	364/200
4,064,556	12/1977	Edelberg	364/900
4,065,756	12/1977	Danigrahi	365/78

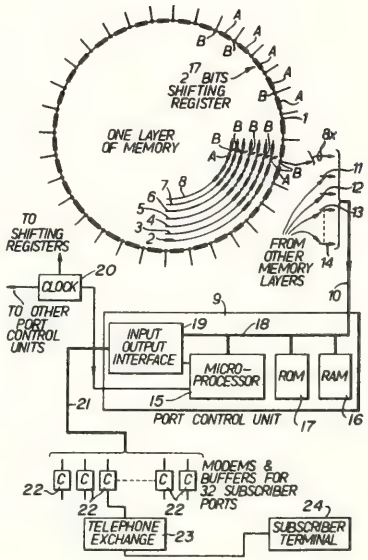
Primary Examiner—James D. Thomas

Attorney, Agent, or Firm—Hall & Houghton

[57] **ABSTRACT**

An information handling apparatus capable of having a large number of input/output ports includes a plurality of independent processors connected to respective positions around a plurality of closed rings of shifting registers arranged in parallel which form the main storage medium for the apparatus.

7 Claims, 1 Drawing Figure



United States Patent [19]

Gilbert et al.

[11] **4,193,112**

[45] **Mar. 11, 1980**

[54] **MICROCOMPUTER DATA DISPLAY COMMUNICATION SYSTEM WITH A HARDWIRE EDITING PROCESSOR**

[75] Inventors: **Judson T. Gilbert**, Hialeah; **George R. Harrison; Alan R. Holbrook**, both of Miami; **Michael Levy**, Pembroke Pines; **John B. Scott**, Miami Springs; **Harris K. Swan**, Miami, all of Fla.

[73] Assignee: **Racal-Milgo, Inc.**, Miami, Fla.

[21] Appl. No.: **651,249**

[22] Filed: **Jan. 22, 1976**

[51] **Int. Cl.**[2] **G06F 3/14**; G06F 9/00; G06F 13/00

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** ..... 340/172.5, 324 A, 324 AD, 340/711, 723, 724, 789, 798, 799, 800, 803; 445/1; 364/200 MS File, 900 MS File

[56] **References Cited**

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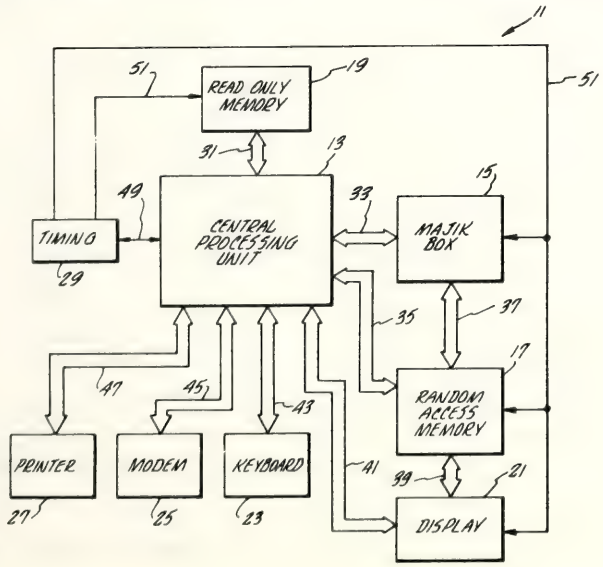
4,070,710	1/1978	Sukonick et al.	364/900
4,127,851	11/1978	Middel	340/324 AD

Primary Examiner—Melvin B. Chapnick
Attorney, Agent, or Firm—Jackson, Jones & Price

[57] **ABSTRACT**

A data display communication system wherein data generated locally by a keyboard or generated remotely and communicated by modems is displayed on a display device. Data displayed on the screen can be edited or reformatted prior to storage, print-out, or transmission to a remote location. Data communicated between storage and the central processing unit is handled in blocks that make up one full line of characters on the display device. All edit and format functions are performed on the basis of these blocks of data. Timing for the display device controls the operation of the system. The communication system utilizes a microprocessor operating in conjunction with specific hardware logic to handle display oriented operations.

22 Claims, 20 Drawing Figures



United States Patent [19]

Krauss et al.

[11] **4,181,947**

[45] **Jan. 1, 1980**

[54] **CONVEYOR SORTING SYSTEM**

[75] Inventors: **Dale A. Krauss; Robin L. Chang**, both of Grand Rapids, Mich.

[73] Assignee: **Rapistan, Incorporated**, Grand Rapids, Mich.

[21] Appl. No.: **908,999**

[22] Filed: **May 23, 1978**

[51] **Int. Cl.**[2] **G06F 15/20**; B65G 43/00

[52] **U.S. Cl.** **364/478**; 198/349; 209/942; 364/120; 364/900; 414/134

[58] **Field of Search** ..... 364/478, 479, 120, 552, 364/200 MS File, 900 MS File; 198/349, 356; 209/942, 546, 547, 552, 564, 604; 214/11 R, 11 C

[56] **References Cited**

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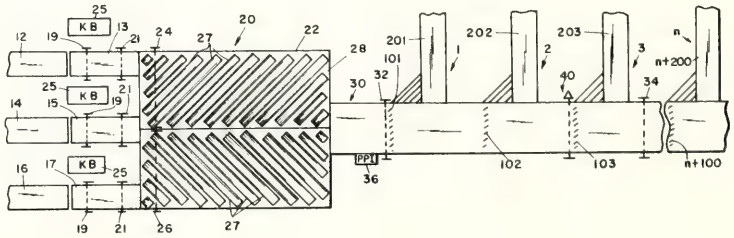
3,895,716	7/1975	Ugo	364/900 X

Primary Examiner—Joseph F. Ruggiero
Attorney, Agent, or Firm—Price, Heneveld, Huizenga & Cooper

[57] **ABSTRACT**

A high speed conveyor sorting system includes a plurality of infeed conveyors coupled to an induction station including a merging conveyor for singulating articles from the infeed conveyor and inducting them onto a sorting conveyor. An operator actuated control system is employed for controlling the release mechanism of the induction station and diverters spaced along the sorting conveyor for discharging articles from the sorting conveyor onto preselected diverting conveyors spaced longitudinally along the sorting conveyor. The control system includes a portable training detector which is movably positioned near each of the divert locations such that the travel of an article from a predetermined reference point detector near the induction station to each of the divert locations can be accurately ascertained by counting pulses from a pulse position indicator associated with the conveyor during the travel interval of the article. Such information is stored in memory means of the control system and subsequently employed for the actuation of a diverter at preselected divert locations to effect accurate discharge of articles from the sorting conveyor to divert conveyors at the selected divert locations.

28 Claims, 5 Drawing Figures



United States Patent [19]
Gunckel, II et al.
[11] **4,199,810**
[45] **Apr. 22, 1980**

[54] **RADIATION HARDENED REGISTER FILE**

[75] Inventors: **Thomas L. Gunckel, II**, Santa Ana; **John S. Irvine**, Fountain Valley, both of Calif.

[73] Assignee: **Rockwell International Corporation**, El Segundo, Calif.

[21] Appl. No.: **757,807**

[22] Filed: **Jan. 7, 1977**

[51] **Int. Cl.**[2] **G06F 13/00**
[52] **U.S. Cl.** **364/200**; 371/68
[58] **Field of Search** ..... 235/153 AE; 364/200 MS File, 900 MS File

[56] **References Cited**

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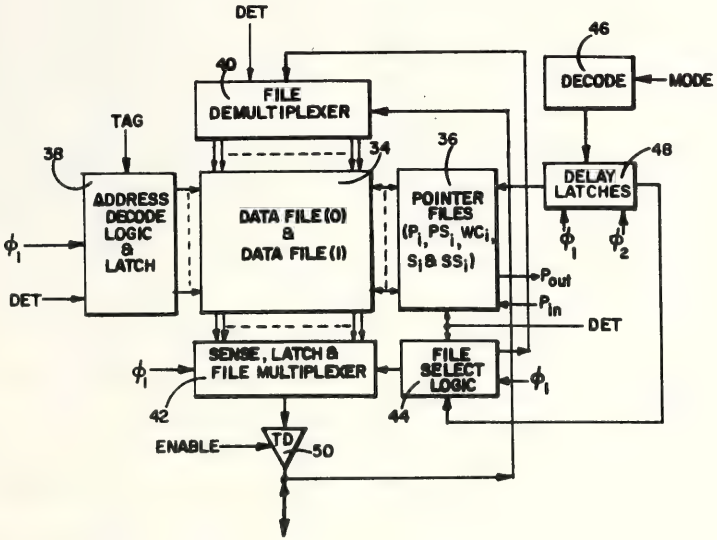
3,950,729	4/1976	Fletcher et al.	364/200
4,031,374	6/1977	Groudan et al.	235/153 AE

Primary Examiner—Howard A. Birmiel
Attorney, Agent, or Firm—H. Fredrick Hamann; Leonard Tachner

[57] **ABSTRACT**

A radiation hardened register file renders a central processing unit intrinsically hard to the disruptive effects of nuclear radiation by providing means for establishing a valid rollback point for each computer instruction operation performed in the central processing unit. Dual data register images provide alternate locations for storing data operands in the register file. A pointer register stores a signal the truth state of which indicates which of the two images currently provides the proper place to store information presently being written and also provides an indication of the current location of assured valid signals for a recovery operation and resumption of normal computer functions subsequent to a disruptive event. Pointer save registers are used to store the latest value of the signal stored in the pointer registers, thereby also preserving valid pointer information for recovery subsequent to a circumvented disrupting event. A master pointer register stores a signal indicating which of two alternate pointer save registers currently stores the appropriate signal for selecting the proper truth state for the signal in the pointer register.

21 Claims, 20 Drawing Figures



United States Patent [19]
Sloan et al.
[11] **4,222,111**
[45] **Sep. 9, 1980**

[54] **METHOD AND APPARATUS FOR MONITORING STATUS OF TABLES IN A RESTAURANT**

[75] Inventors: **John W. Sloan; Frank E. Bumb, Jr.**, both of Phoenix, Ariz.

[73] Assignee: **Sherwood Johnston**, Phoenix, Ariz.

[21] Appl. No.: **861,648**

[22] Filed: **Dec. 19, 1977**

[51] **Int. Cl.**[2] **G06F 3/02**
[52] **U.S. Cl.** ..... **364/900**; 340/286 R
[58] **Field of Search** ..... 364/200, 900; 235/92 B, 235/92 AC, 92 CP, 92 CT, 92 DP, 92 R

[56] **References Cited**

U.S. PATENT DOCUMENTS

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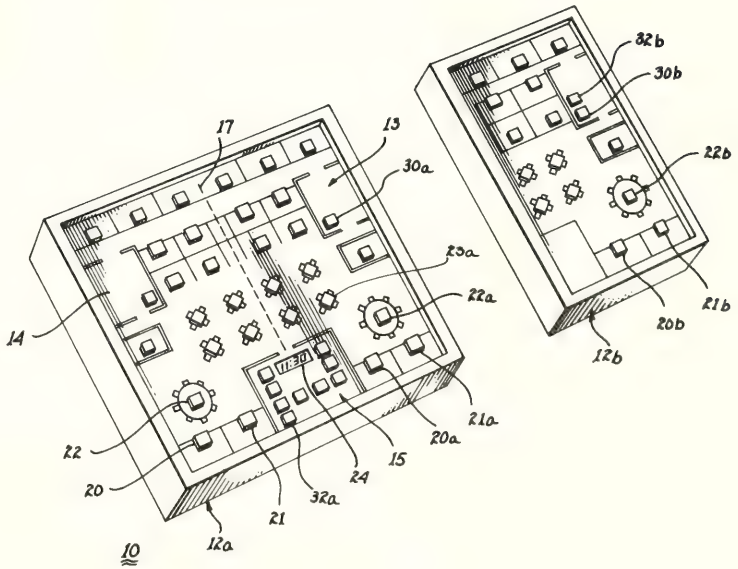
3,310,797	3/1967	Auger	340/286

Primary Examiner—Gareth D. Shaw
Assistant Examiner—David Y. Eng
Attorney, Agent, or Firm—Cahill, Sutton & Thomas

[57] **ABSTRACT**

System and method for monitoring occupancy and status of restaurant tables to minimize the time each table is unoccupied. The system includes a processor unit coupled by means of serial data buses to a host unit and a plurality of service units. The host unit includes separate push buttons, or "table buttons", which correspond, respectively, to tables within a particular service area of the restaurant. The processor unit computes and stores the status of each table in the restaurant. The processor periodically computes and transmits display information representative of the updated status of the tables to the host unit and the service units. Such display information for a particular table is utilized at both the host station and the appropriate service station to illuminate or flash the table buttons in such a manner as to indicate the present status of the corresponding tables to restaurant personnel. The table status for a particular table is updated by depressing the corresponding table button of either the host station or a service station. The table button thereby closes a switch, which causes switch closure information to be transmitted to the processor unit. The processor unit computes updated status information in response to the switch closure information received from the host unit or service unit and stores the updated table status in a memory of the processor unit. The updated status information is subsequently transmitted to the appropriate service unit and the host unit to illuminate or flash the appropriate table buttons in such a manner as to indicate the updated table status to restaurant personnel.

18 Claims, 12 Drawing Figures



United States Patent [19]

Caltagirone et al.

[11] **4,217,646**

[45] **Aug. 12, 1980**

[54] **AUTOMATIC CONTROL SYSTEM FOR A BUILDING**

[75] Inventors: **Anthony V. Caltagirone; George J. Bradford,** both of York, Pa.; **James J. Parro,** Skaneateles, N.Y.

[73] Assignee: **The Singer Company,** Stamford, Conn.

[21] Appl. No.: **971,980**

[22] Filed: **Dec. 21, 1978**

[51] **Int. Cl.**[2] **G05D 23/32;** H04Q 7/00

[52] **U.S. Cl.** ..... **364/493;** 165/22; 236/91 D; 237/2 A; 455/152; 340/310 R; 364/107; 364/900

[58] **Field of Search** ..... 364/400, 492, 493, 483, 364/200, 900, 418, 104, 107; 340/310 R, 310 A; 236/91 D, 91 E, 91 F, 46 R, 46 C; 237/2 R, 2 A; 325/301, 302, 310, 314; 219/490, 494, 509, 510; 307/39, 38, 52, 116, 117; 165/13, 14, 22, 32

[56] **References Cited**

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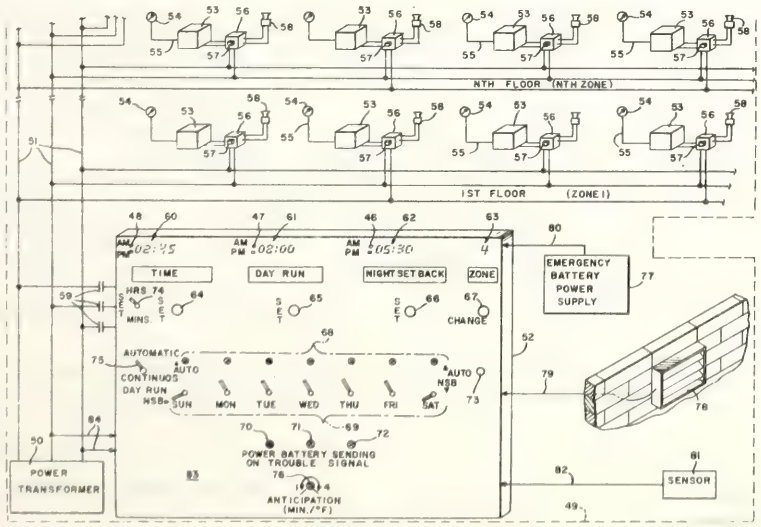
4,114,141	9/1978	Travis	340/310 A
4,167,786	9/1979	Miller et al.	364/493

Primary Examiner—Errol A. Krass
Attorney, Agent, or Firm—Charles R. Lewis

[57] **ABSTRACT**

An automatic system for controlling the environmental conditions in a building divided into a plurality of zones includes a control station that sends control signals over the power lines of the building to control power consuming appliances in the various zones. The control station includes a programmable computer that is operably coupled to various displays and control switches on a control panel. In one mode of operation the switches and displays are utilized to program a schedule into the computer for controlling the various power consuming appliances such as heating and airconditioning units, lights, machinery and the like in order to provide a desired environment within the various zones of the building. In another mode of operation the displays on the control panel provide operator information as to the programmed schedule for the zones whereas the switches on the control panel enable the schedule stored within the programmed computer to be selectively overridden to accommodate changing conditions, such as holidays and the like, where newly desired environmental conditions in the various zones of the building differ from the schedule stored within the programmed computer. The system has the capability of automatically advancing the scheduled start up time of heating units dependent upon the difference between the temperature outside the building and a reference temperature in order to insure that environmental conditions in the various zones of the building are at a desired level at the time of occupancy.

52 Claims, 34 Drawing Figures



United States Patent [19]

Hellman et al.

[11] **4,218,582**

[45] **Aug. 19, 1980**

[54] **PUBLIC KEY CRYPTOGRAPHIC APPARATUS AND METHOD**

[75] Inventors: **Martin E. Hellman,** Stanford; **Ralph C. Merkle,** Palo Alto, both of Calif.

[73] Assignee: **The Board of Trustees of the Leland Stanford Junior University,** Stanford, Calif.

[21] Appl. No.: **839,939**

[22] Filed: **Oct. 6, 1977**

[51] **Int. Cl.**[2] **H04L 9/04**

[52] **U.S. Cl.** **178/22;** 364/900

[58] **Field of Search** 178/22

[56] **References Cited**

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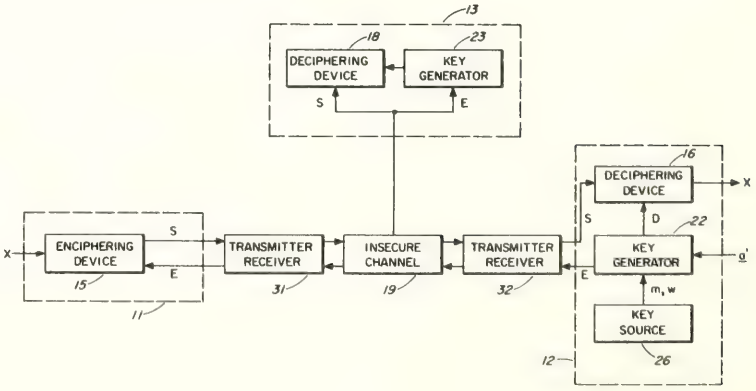
Primary Examiner—Howard A. Birmiel

[57] **ABSTRACT**

A cryptographic system transmits a computationally secure cryptogram that is generated from a publicly known transformation of the message sent by the transmitter; the cryptogram is again transformed by the authorized receiver using a secret reciprocal transformation to reproduce the message sent. The authorized receiver's transformation is known only by the authorized receiver and is used to generate the transmitter's transformation that is made publicly known. The publicly known transformation uses operations that are easily performed but extremely difficult to invert. It is infeasible for an unauthorized receiver to invert the publicly known transformation or duplicate the authorized receiver's secret transformation to obtain the message sent.

17 Claims, 13 Drawing Figures



United States Patent [19]
Henry et al.
[11] **4,217,658**
[45] **Aug. 12, 1980**

[54] **PROCESS CONTROL SYSTEM THAT CONTROLS ITS OUTPUTS ACCORDING TO THE RESULTS OF SUCCESSIVE ANALYSIS OF THE VERTICAL INPUT COLUMNS OF A HYPOTHETICAL LADDER DIAGRAM**

[75] Inventors: **Donald E. Henry**, Bettendorf, Iowa; **Thomas A. Murrell**, Urbana, Ill.; **Marvin H. Schilt**, Bettendorf, Iowa; **Alfred C. Weaver**, Champaign, Ill.

[73] Assignee: **Struthers-Dunn, Inc.**, Pitman, N.J.

[21] Appl. No.: **819,038**

[22] Filed: **Jul. 25, 1977**

[51] **Int. Cl.**[2] **G06F 15/46**
[52] **U.S. Cl.** **364/900**; 364/104
[58] **Field of Search** ..... 364/200 MS File, 104, 364/107, 117, 900 MS File

[56] **References Cited**

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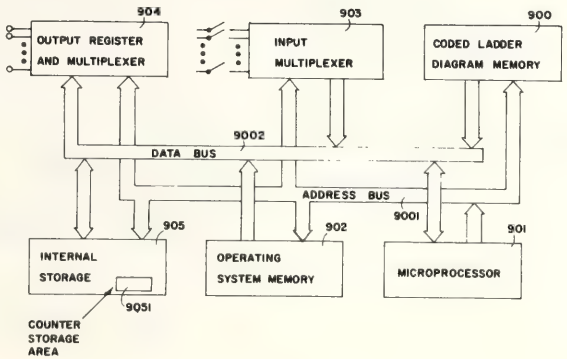
Primary Examiner—Mark E. Nusbaum
Attorney, Agent, or Firm—William D. Hall

[57] **ABSTRACT**

A process control system for controlling a set of outputs according to a multiplicity of inputs. The process control system analyzes the condition of the inputs as though they were arranged in a hypothetical ladder diagram which is a representation of the circuitry that would be required to control the loads if simple switches were interconnected, by wires, in the conventional way to control the loads. The hypothetical ladder diagram includes a plurality of hypothetical horizontal rows of circuit elements in which the circuit elements are also located in hypothetical vertical columns. All of the hypothetical vertical columns, except the last, are "input" vertical columns since they represent input circuit elements. The last vertical column contains the loads (or outputs) and is an "output" vertical column. The hypothetical input vertical column at the left end of the hypothetical ladder is first analyzed by the processing unit to determine whether there is a potential (binary 1), or no potential (binary 0), at the output of each circuit element of that hypothetical vertical column. These outputs of the circuit elements of said first vertical column are then fed back into the processor for an analysis of the second hypothetical input vertical column to likewise determine whether there is a potential (binary 1), or the lack of a potential (binary 0), at the output of each circuit element of said second vertical column. This procedure continues until all of the hypothetical input vertical columns have been analyzed. The oututs of the last input vertical column to be analyzed are then utilized by the processor to analyze the output vertical column to determine which output or outputs should be energized or de-energized to thus operate the controlled machinery.

11 Claims, 14 Drawing Figures



United States Patent [19]
Katzman et al.
[11] **4,228,496**
[45] **Oct. 14, 1980**

[54] **MULTIPROCESSOR SYSTEM**

[75] Inventors: **James A. Katzman**, San Jose; **Joel F. Bartlett**, Palo Alto; **Richard M. Bixler**, Sunnyvale; **William H. Davidow**, Atherton; **John A. Despotakis**, Pleasanton; **Peter J. Graziano**; **Michael D. Green**, both of Los Altos; **David A. Greig**; **Steven J. Hayashi**, both of Cupertino; **David R. Mackie**, Ben Lomond; **Dennis L. McEvoy**, Scotts Valley; **James G. Treybig**; **Steven W. Wierenga**, both of Sunnyvale, all of Calif.

[73] Assignee: **Tandem Computers Incorporated**, Cupertino, Calif.

[21] Appl. No.: **721,043**

[22] Filed: **Sep. 7, 1976**

[51] **Int. Cl.**[3] **G06F 15/16**; G06F 15/06
[52] **U.S. Cl.** **364/200**
[58] **Field of Search** ... 364/200 MS File, 900 MS File

[56] **References Cited**

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4,034,347	7/1977	Probert	364/200
4,034,794	10/1978	Matsumoto	364/200 X
4,035,777	7/1977	Moreton	364/200
4,040,028	8/1977	Pauker et al.	364/200
4,041,472	8/1977	Shah et al.	364/900
4,130,865	12/1978	Heart et al.	364/200

Primary Examiner—Mark E. Nusbaum
Attorney, Agent, or Firm—Donald C. Feix

[57] **ABSTRACT**

A multiprocessor system the kind in which two or more separate processor modules are interconnected for parallel processing includes two redundant interprocessor buses dedicated exclusively to interprocessor communication. Any processor module may send information to any other processor module by either bus. The buses are shared in use by the processor modules on a time-sharing basis. Use of each bus is controlled by a special bus controller.

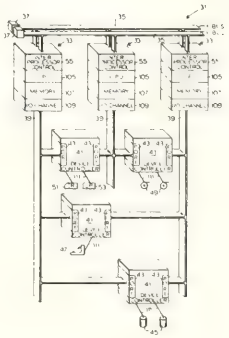
The multiprocessor system includes an input/output system having multi-port device controllers and input-/output buses connecting each device controller for access by the input/output channels of at least two different processor modules. Each device controller includes logic which insures that only one port is selected for access at a time.

The multiprocessor system includes a distributed power supply system which insures nonstop operation of the remainder of the multiprocessor system in the event of a failure of a power supply for a part of the system. The distributed power supply system includes a separate power supply for each processor module and two separate power supplies for each device controller. Either one of the two power supplies provides the entire power for the device controller in the event the other power supply fails. The distributed power supply system permits any processor module or device controller to be powered down so that on-line maintenance can be performed in a power-off condition while the rest of the multiprocessor system is on-line and functional.

The multiprocessor system includes a memory system in which the memory of each processor module is divided into four logical address areas—user data, system data, user code and system code. The memory system includes a map which translates logical addresses to physical addresses and which coacts with the multiprocessor system to bring pages from secondary memory into primary main memory as required to implement a virtual memory system. The map also provides a protection function. It provides inherent protection among users in a multiprogramming environment, isolates programs from data and protects system programs from the actions of user programs. The map also provides a reference history information for each logical page as an aid to efficient memory management by the operating system.

The multiprocessor system includes in the memory of each processor module an error detection and correction system which detects all single bit and double bit errors and which corrects all single bit errors in semiconductor memory storage.

80 Claims, 42 Drawing Figures



United States Patent [19]
Hamano et al.
[11] **4,213,179**
[45] **Jul. 15, 1980**

[54] **DATA PROCESSING APPARATUS FOR ELECTRONIC CASHIER REGISTERS**

[75] Inventors: **Koichi Hamano; Takao Morimoto; Junko Watanabe; Kaoru Ono; Norio Yagi**, all of Shizuoka, Japan

[73] Assignee: **Tokyo Electric Co., Ltd.**, Tokyo, Japan

[21] Appl. No.: **944,591**

[22] Filed: **Sep. 21, 1978**

[30] **Foreign Application Priority Data**

Oct. 8, 1977 [JP] Japan 52-121101
Oct. 8, 1977 [JP] Japan 52-121104

[51] **Int. Cl.**[2] **G06F 15/02**; G06F 15/20
[52] **U.S. Cl.** **364/405**; 364/900
[58] **Field of Search** 364/405, 404, 200, 900

[56] **References Cited**

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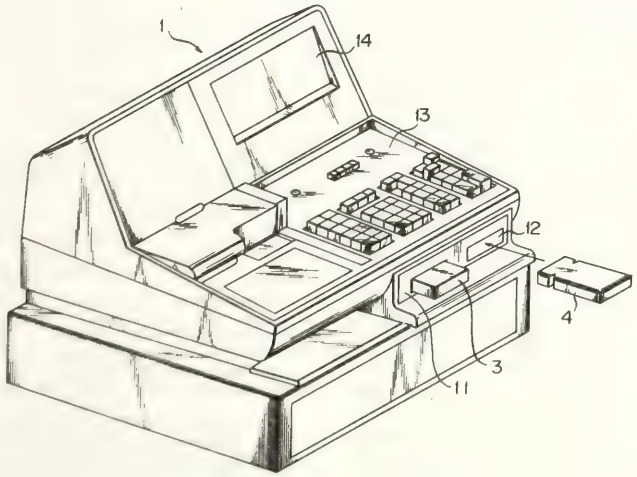
51-98924	8/1976	Japan	364/709

Primary Examiner—David H. Malzahn
Attorney, Agent, or Firm—Frishauf, Holtz, Goodman & Woodward

[57] **ABSTRACT**

A data processing apparatus for an electronic cash register comprises a keyboard having a plurality of entry keys, a printer, a memory unit, an interface circuit with which a memory pack storing sales data is mechanically, electrically and removably coupled and a data processing unit connected with the keyboard, the printer, the memory unit and the interface circuit. Responding to operations of one of the keys for sales data selection, the data processing unit energizes the memory pack connected to the interface circuit to read out the sales data corresponding to the operated sales information key from the energized memory pack and write the read-out sales data into the memory unit and then issue a print signal to the printer for printing the sales data.

6 Claims, 31 Drawing Figures



United States Patent [19]
Schuller et al.
[11] **4,231,105**
[45] **Oct. 28, 1980**

[54] **VENDOR CONTROL CIRCUIT**

[75] Inventors: **James T. Schuller**, St. Louis County; **Paul N. Albrecht**, Ballwin; **Hugo M. Canizares**, Bridgeton, all of Mo.

[73] Assignee: **UMC Industries, Inc.**, Stamford, Conn.

[21] Appl. No.: **921,960**

[22] Filed: **Jul. 5, 1978**

[51] **Int. Cl.**[3] **G07F 11/62**; G06F 15/21
[52] **U.S. Cl.** **364/900**; 194/10; 364/479
[58] **Field of Search** ..... 364/900 MS File, 404, 364/405, 479; 235/92 AC; 340/149 R; 194/1 N, 2, 10

[56] **References Cited**

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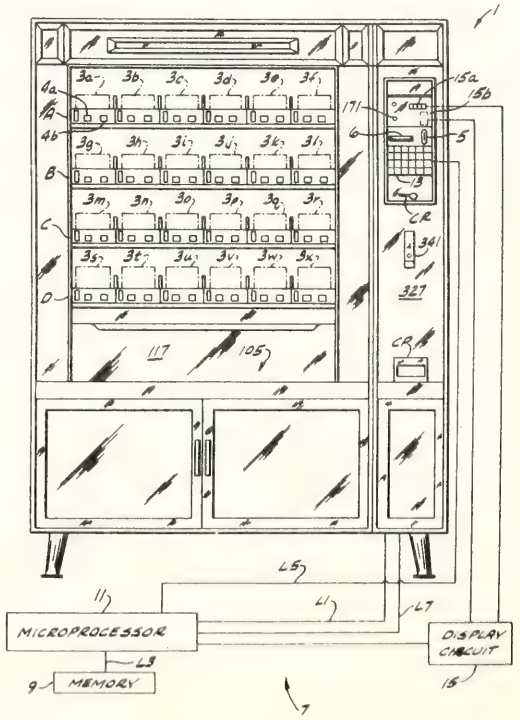
Primary Examiner—Jerry Smith
Attorney, Agent, or Firm—Senniger, Powers, Leavitt and Roedel

[57] **ABSTRACT**

A control circuit for a vendor for vending a plurality of items comprising a microprocessor, an electrically alterable memory, a display circuit and an interrogation circuit. Values of parameters, typically prices, associated with the items to be vended are stored in the memory. The interrogation circuit can be activated to retrieve from memory the value of the parameter (e.g., price) associated with any given item. The parameter value is thereupon displayed by the display circuit. The display circuit displays the parameter value retrieved from memory independently of whether the microprocessor has another input equal in value to the value of that parameter. The parameter value stored in the memory for any given item can be altered by the microprocessor.

38 Claims, 42 Drawing Figures



United States Patent [19]

Buscher et al.

[11] **4,218,737**

[45] **Aug. 19, 1980**

[54] **REVENUE METERING SYSTEM FOR POWER COMPANIES**

[75] Inventors: **David J. Buscher**, Silver Spring, Md.; **Robert G. Ellingwood**, Vancouver, Wash.; **Marc A. Ressler**, College Park, Md.

[73] Assignee: **The United States of America as represented by the Secretary of the Army**, Washington, D.C.

[21] Appl. No.: **829,037**

[22] Filed: **Aug. 30, 1977**

[51] **Int. Cl.**[3] **H02J 13/00**; G01R 11/57; G01R 19/30

[52] **U.S. Cl.** **364/493**; 364/483; 364/900; 340/151; 324/116

[58] **Field of Search** ... 364/200 MS File, 900 MS File, 364/483, 492, 493, 464; 340/150, 15; 324/103 R, 116

[56] **References Cited**

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3,972,470	8/1976	Takagi	364/483
4,008,458	2/1977	Wensley	340/151
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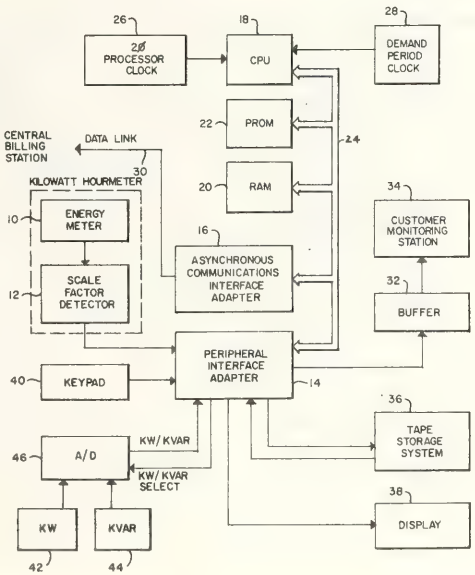
4,050,096	9/1977	Bennett	364/200
4,075,699	2/1978	Schneider	324/103 R
4,077,061	2/1978	Johnston	364/483

Primary Examiner—James D. Thomas
Attorney, Agent, or Firm—Nathan Edelberg; Robert P. Gibson; Saul Elbaum

[57] **ABSTRACT**

An energy meter at an electrical substation contains a detector which changes state each time a quantity of energy is consumed. This data is accumulated in a microprocessor system. Real time energy consumption data is fed back to a customer monitoring station and may be telemetered to a power company central billing station. Customer and power company have their demand periods synchronized by the microprocessor system.

5 Claims, 2 Drawing Figures



United States Patent [19]

Games et al.

[11] **4,212,078**

[45] **Jul. 8, 1980**

[54] **COMPUTER CONTROLLED FACILITY MANAGEMENT SYSTEM (FMS)**

[75] Inventors: **John E. Games**, Granby; **Richard E. Rosien**, Windsor; **William W. Bitterli**, Simsbury, all of Conn.

[73] Assignee: **United Technologies Corporation**, Hartford, Conn.

[21] Appl. No.: **864,557**

[22] Filed: **Dec. 27, 1977**

[51] **Int. Cl.**[2] **G06F 3/04**; G06F 15/46; H04Q 9/00

[52] **U.S. Cl.** **364/900**; 165/22

[58] **Field of Search** ... 364/200 MS File, 900 MS File, 364/114, 118; 236/1 B, 1 C; 165/13, 14, 22, 27, 28

[56] **References Cited**

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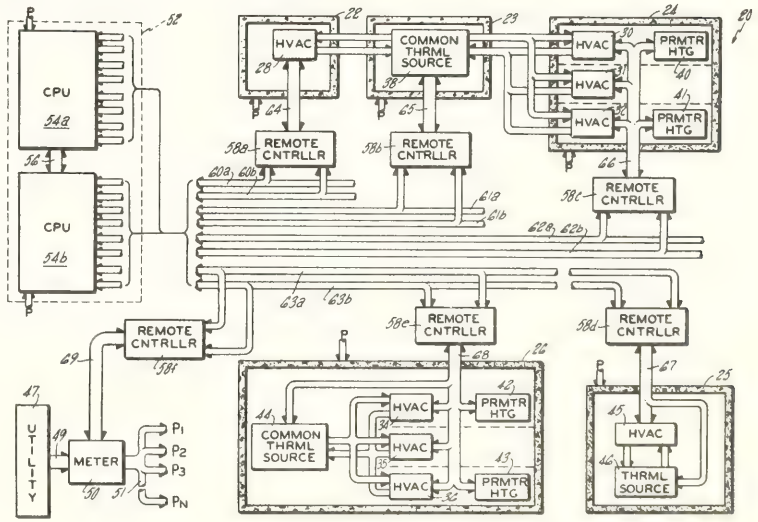
4,090,248	5/1978	Swanson et al.	364/900

Primary Examiner—Mark E. Nusbaum
Assistant Examiner—Thomas M. Heckler
Attorney, Agent, or Firm—Dominic J. Chiantera

[57] **ABSTRACT**

A central control system includes a central processing unit (CPU) installed in a central location of a facility, and interconnected with a plurality of remote controllers, each located in an associated one of several buildings in the facility and each including a remote microprocessor (RMP), the CPU automatically controlling, simultaneously from the central location, the closed loop operation of individual environmental conditioning systems in the several buildings comprising the facility in combination with the RMP associated therewith and in dependence on the sensed temperature conditions within the living spaces associated with each system. The CPU includes a keyboard responsive to operator control for receiving selected parameter reference values provided by the operator at the central location, the reference values establishing the closed loop gains and reference temperatures for the individual environmental systems, the reference values being instantaneously changeable by the operator in one, or all of the environmental systems to accommodate changes in operating conditions. The central control including two CPUs, each fully capable of providing automatic control of the facility environmental conditioning systems in combination with the RMPs, the system further including redundant interconnecting lines between each CPU and the plurality of RMPs, each line including a liner receiver for each RMP, to provide the simultaneous control of the closed loop operation of the individual environmental conditioning systems in each of the buildings in such a manner as to provide fail-safe control of each from the centralized location.

4 Claims, 7 Drawing Figures



United States Patent [19]

Frey et al.

[11] **4,181,971**

[45] **Jan. 1, 1980**

[54] **APPARATUS FOR PRESENTING A SEQUENCE OF FIXED PICTURES**

[75] Inventors: **Richard C. Frey; Malcolm R. Railey,** both of Akron, Ohio; **Thomas J. Wargo,** Waukegan, Ill.

[73] Assignee: **The University of Akron,** Akron, Ohio

[21] Appl. No.: **656,395**

[22] Filed: **Feb. 9, 1976**

[51] **Int. Cl.**[2] **G06F 3/14**

[52] **U.S. Cl.** **364/900;** 340/724; 340/798; 358/142; 364/521

[58] **Field of Search** ..... 340/172.5, 324 A, 324 AD, 340/724, 798, 723; 445/1; 444/1; 235/151; 364/200 MS File, 900 MS File, 521; 358/142

[56] **References Cited**

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4,016,362	4/1977	Bristow et al.	358/142

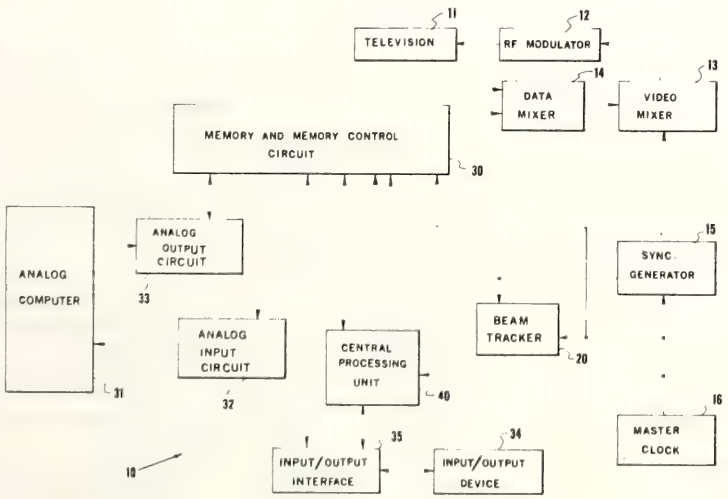
Primary Examiner—Mark E. Nusbaum

Attorney, Agent, or Firm—Hamilton, Renner & Kenner

[57] **ABSTRACT**

Disclosed is a device which can utilize, as an input signal, the solution to mathematical problems from an analog computer or which can be used directly with a process that is governed by a mathematical problem to pictorially depict the solution to the problem. The problem being solved can be dynamically displayed on a device such as a conventional television receiver for use by a student, technician or the like. The input signal indicative of the solution of the mathematical problem is fed to a memory and control device which can store the same for subsequent use. The memory also has stored therein data representative of the images necessary to create the pictorial representation of the problem. A programmable device, preferably in the form of a digital computer, interprets the input signals and directs the data in the memory so that it is properly displayed on the television receiver.

35 Claims, 11 Drawing Figures



United States Patent [19]

Corwin et al.

[11] **4,198,685**

[45] **Apr. 15, 1980**

[54] **TEXT EDITING SYSTEM HAVING FLEXIBLE REPETITIVE OPERATION CAPABILITY WITH KEYBOARD INTERACTIVE FEATURE**

[75] Inventors: **Daniel W. Corwin,** Dunstable; **Harold S. Koplow,** Lynnfield; **David Moros,** Winchester; **Paul Anagnostopoulos,** Burlington, all of Mass.

[73] Assignee: **Wang Laboratories, Inc.,** Lowell, Mass.

[21] Appl. No.: **959,649**

[22] Filed: **Nov. 13, 1978**

[51] **Int. Cl.**[2] **G06F 3/02;** G06F 3/14

[52] **U.S. Cl.** **364/900**

[58] **Field of Search** 364/200, 900

[56] **References Cited**

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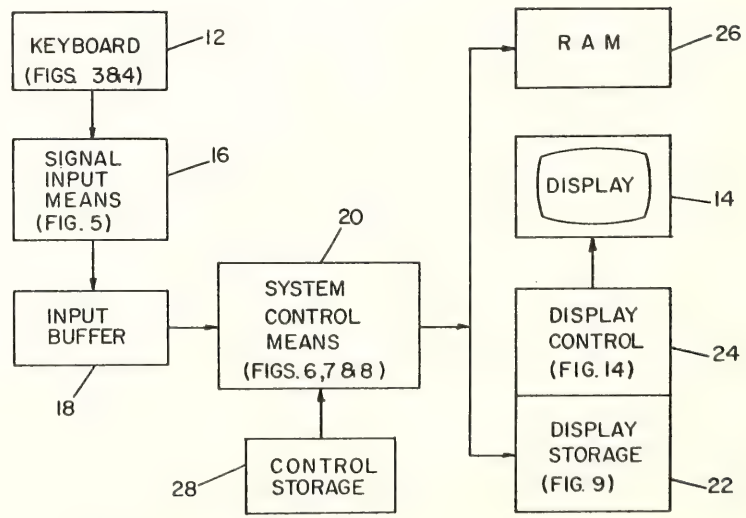
4,137,564	1/1979	Spencer	364/200
4,150,429	4/1979	Ying	364/200

Primary Examiner—Harvey E. Springborn

[57] **ABSTRACT**

An improvement in a text-editing system having a keyboard for inputting character and text-editing operation signals, a CRT display, display storage and text storage, and additional special condition storage; the system responds to a select/store signal to select a sequence of signals from text storage and store it into special condition storage, and thereafter responds to a recall signal to disable the keyboard, retrieve the stored sequence, and operate according to it. A keyboard interactive operation signal can be stored as part of such a sequence. The system responds to retrieval of this signal to permit input of a keystroke string through the keyboard to the display storage and text storage; the system further responds to a keystroke string end indicator, input through the keyboard, to resume recall and execution of the stored sequence.

3 Claims, 21 Drawing Figures



United States Patent [19]

Otis, Jr. et al.

[11] **4,197,579**

[45] **Apr. 8, 1980**

[54] **MULTI-PROCESSOR FOR SIMULTANEOUSLY EXECUTING A PLURALITY OF PROGRAMS IN A TIME-INTERLACED MANNER**

[75] Inventors: **Alton B. Otis, Jr.**, San Francisco; **Peter E. Forsman**, Palo Alto, both of Calif.

[73] Assignee: **Xebec Systems Incorporated**, Santa Clara, Calif.

[21] Appl. No.: **913,084**

[22] Filed: **Jun. 6, 1978**

[51] **Int. Cl.**[2] **G06F 9/20**

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** ..... 364/200 MS File

[56] **References Cited**

U.S. PATENT DOCUMENTS

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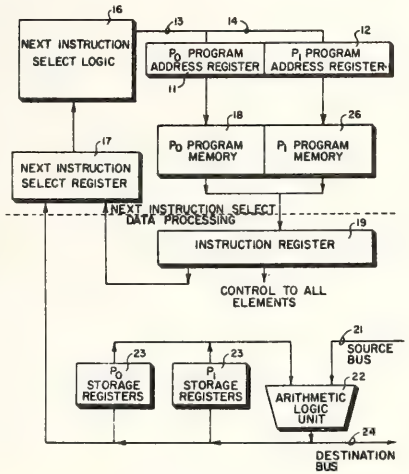
3,980,992	9/1976	Levy et al.	364/200

Primary Examiner—Harvey E. Springborn
Attorney, Agent, or Firm—C. Michael Zimmerman

[57] **ABSTRACT**

A computer processor is described capable of simultaneously executing a plurality of programs. It accomplishes this by utilizing the next instruction select elements of a processor to select the next instruction for one program, while the data processing elements of the processor are executing an instruction of another program. The processor includes in addition to the next instruction select and data processing elements normally found in a microprocessor, additional program dependent elements for each of the plurality of programs to be processed. That is, it includes for each of the programs to be processed, a program memory allocation, a program address register, and the non-shared data storage registers, such as accumulators.

8 Claims, 3 Drawing Figures



United States Patent [19]

Chesley

[11] **4,191,996**

[45] **Mar. 4, 1980**

[54] **SELF-CONFIGURABLE COMPUTER AND MEMORY SYSTEM**

[76] Inventor: **Gilman D. Chesley**, 22431 Starling Dr., Los Altos, Calif. 94022

[21] Appl. No.: **818,235**

[22] Filed: **Jul. 22, 1977**

[51] **Int. Cl.**[2] **G06F 11/04**

[52] **U.S. Cl.** ..... **364/200**; 235/303.41; 324/73 AT; 324/73 PC

[58] **Field of Search** ... 364/200 MS File, 900 MS File; 235/304, 304.1, 303.42, 302.3, 303.41; 324/73 R, 73 AT, 73 PC

[56] **References Cited**

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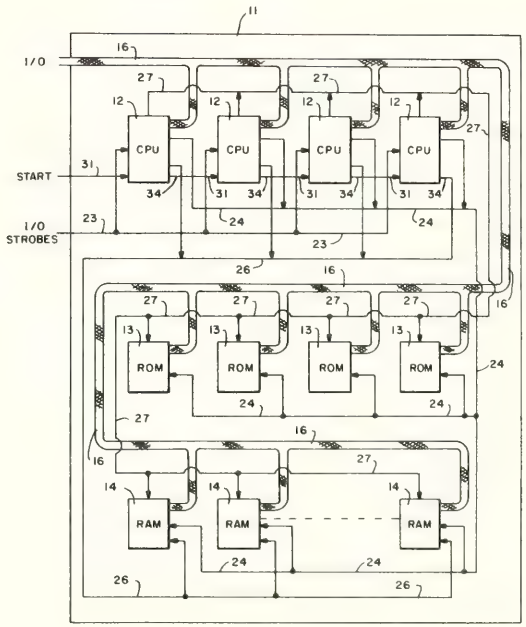
4,058,851	11/1977	Scheuneman	364/200
4,066,880	1/1978	Salley	235/302.3

Primary Examiner—Mark E. Nusbaum
Attorney, Agent, or Firm—Flehr, Hohbach, Test, Albritton & Herbert

[57] **ABSTRACT**

Computer and memory system on a wafer which contains redundant elements and which is capable of self-testing and self-configuration to form a complete system consisting of a central processing unit (CPU), a read only memory unit (ROM), and a plurality of read/write random access memory units (RAM). These units are interconnected by a common bus, which is also available for external connections to the wafer. The first CPU tests each ROM to find a good one and then uses the program contained in that ROM to test itself. If the first CPU does not test satisfactorily, the remaining CPU's are tested until a good one is found. The RAM's are then tested with the good ROM and CPU, and the results are tabulated to form a page oriented computer system.

14 Claims, 4 Drawing Figures



United States Patent [19]

Godsey

[11] **4,181,941**

[45] **Jan. 1, 1980**

[54] **INTERRUPT SYSTEM AND METHOD**

[76] Inventor: **Ernest E. Godsey**, 6641 Amahl Cir., Tucson, Ariz. 85704

[21] Appl. No.: **890,121**

[22] Filed: **Mar. 27, 1978**

[51] **Int. Cl.**[2] **G06F 9/18**

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** ... 364/200 MS File, 900 MS File; 340/147 LP

[56] **References Cited**

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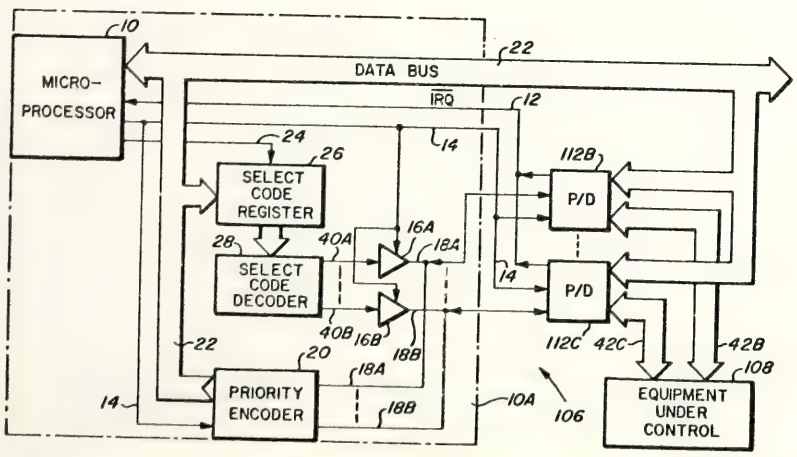
3,866,181	2/1975	Gayman	364/200
3,909,790	9/1975	Shapiro	364/200
4,028,664	6/1977	Monahan	364/200
4,034,349	7/1977	Monaco	364/200

Primary Examiner—James D. Thomas
Attorney, Agent, or Firm—Cahill, Sutton & Thomas

[57] **ABSTRACT**

Method and system for responding to an interrupt signal sent to a microprocessor from one of a plurality of peripheral devices. An acknowledge signal is transmitted from the microprocessor to the peripheral devices. The acknowledge signal operatively isolates select/request terminals of the respective peripheral devices from outputs of a select code decoder. The acknowledge signal also enables the select/request terminals to be inputted to a priority encoder. The acknowledge signal further enables a signal to be produced on the select/request terminal of the interrupting peripheral device, thereby causing the priority encoder to produce a select code representative of the interrupting peripheral device. The select code is subsequently inputted to the microprocessor to enable the microprocessor to access an interrupt service subroutine for the interrupting peripheral device. Subsequent to the end of the acknowledge signal, the select code is inputted by the microprocessor to a select code decoder and is decoded thereby to produce an enable signal which is transmitted to the select/request terminal of the interrupting peripheral device. The enable signal enables the interrupting peripheral device to communicate with the microprocessor via the data bus, thereby permitting the interrupting peripheral device to be serviced by the accessed interrupt service subroutine.

16 Claims, 9 Drawing Figures



United States Patent [19]

Root

[11] **4,218,755**

[45] **Aug. 19, 1980**

[54] **WEATHER FORECASTING APPARATUS**

[76] Inventor: **Steven A. Root**, 804 E. Hills Dr., Bountiful, Utah 84010

[21] Appl. No.: **916,152**

[22] Filed: **Jun. 19, 1978**

[51] **Int. Cl.**[2] **G06F 3/02**; G06F 3/14; G01W 1/10

[52] **U.S. Cl.** ..... **364/900**; 364/420; 364/715; 73/170 R

[58] **Field of Search** ... 364/200 MS File, 900 MS File, 364/420, 439, 443, 449, 458, 550, 557, 558, 715; 73/170 R; 324/72

[56] **References Cited**

U.S. PATENT DOCUMENTS

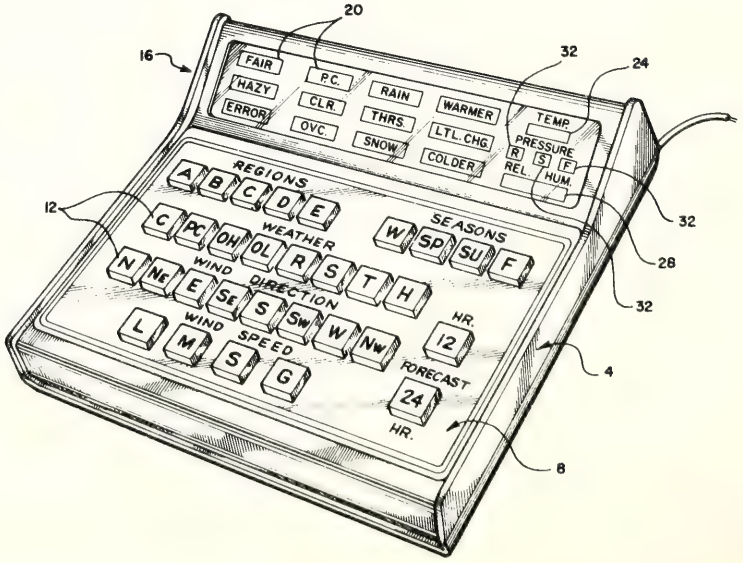
1,920,048	7/1933	Anareta	73/170 R
3,753,117	8/1973	Downing et al.	73/170 R
3,859,635	1/1975	Watson et al.	364/200
3,924,111	12/1975	Farris	364/443
3,979,057	9/1976	Katz et al.	364/443
3,979,728	9/1976	Reddaway	364/200
4,023,408	5/1977	Ryan et al.	73/170 R
4,087,857	5/1978	Joyce et al.	364/200
4,095,221	6/1978	Slocum	73/170 R
4,114,442	9/1978	Pratt	364/557
4,133,509	1/1979	Bliss	244/188

Primary Examiner—Mark E. Nusbaum
Attorney, Agent, or Firm—Thorpe, North & Gold

[57] **ABSTRACT**

Weather forecasting apparatus for producing a visual indication of a weather forecast in response to supplied information, with such supplied information including current weather conditions, current wind speed and wind direction, geographical region information, and season of the year information. The apparatus includes a keyboard upon which such information may be entered, encoders for encoding the information, a display section for lighting one of a plurality of lamps to indicate forecasted weather, and read only memory elements having a plurality of memory locations for storing weather forecast data and for supplying the weather forecast data to the display section from memory locations specified by the coded data. Temperature and relative humidity detecting circuitry may also be included in the apparatus for providing a visual indication of the current temperature and current relative humidity.

9 Claims, 6 Drawing Figures



REFERENCE CITATION INFORMATION

CPU'S AND OTHER SYSTEMS

During the examination of an application for a patent in the United States, references may be cited by the examiner and applicant to show the state of the art or to indicate the prior art most closely related to the invention which is claimed in the application. The information presented below is based on the references made record of during the examination of U.S. Patents granted in the subject technology from 1975-1979. A more detailed explanation of these data appears in Appendix A.

TOTAL PATENTS ISSUED (1975-1979)	457
TOTAL REFERENCES CITED	3094
U.S. Patent References Cited	2956
Foreign Patent References Cited	19
Other References Cited	119

COUNTRY OF ORIGIN OF U.S. PATENT REFERENCES CITED	NUMBER OF CITATIONS
United States	2546
Japan	118
United Kingdom	89
West Germany	62
France	36
Italy	34
Netherlands	17
Switzerland	15
Sweden	9
Israel	8
Canada	8
Belgium	7
Others	7

MOST FREQUENTLY CITED PATENTS	NUMBER OF CITATIONS
3,760,171	30
3,757,306	26
3,702,988	24
3,821,715	21

MOST FREQUENTLY CITED ASSIGNEES	NUMBER OF CITATIONS
International Business Machines Corporation	445
Honeywell Information Systems, Incorporated	189
Burroughs Corporation	143
Texas Instruments, Incorporated	123

United States Patent [19]

Wang et al.

[11] **3,760,171**

[45] **Sept. 18, 1973**

[54] **PROGRAMMABLE CALCULATORS HAVING DISPLAY MEANS AND MULTIPLE MEMORIES**

[75] Inventors: **An Wang**, Lincoln; **Harold Stanley Koplow**, Peabody; **Shu-Kuang Ho**, Chelmsford, all of Mass.

[73] Assignee: **Wang Laboratories, Inc.**, Tewksbury, Mass.

[22] Filed: **Jan. 12, 1971**

[21] Appl. No.: **105,875**

[52] **U.S. Cl.** **235/156**, 340/172.5

[51] **Int. Cl.** **G06f 15/00**, G06f 15/02

[58] **Field of Search** ..... 235/156, 159, 160, 235/164; 340/324 R, 172.5, 365 R

[56] **References Cited**

UNITED STATES PATENTS

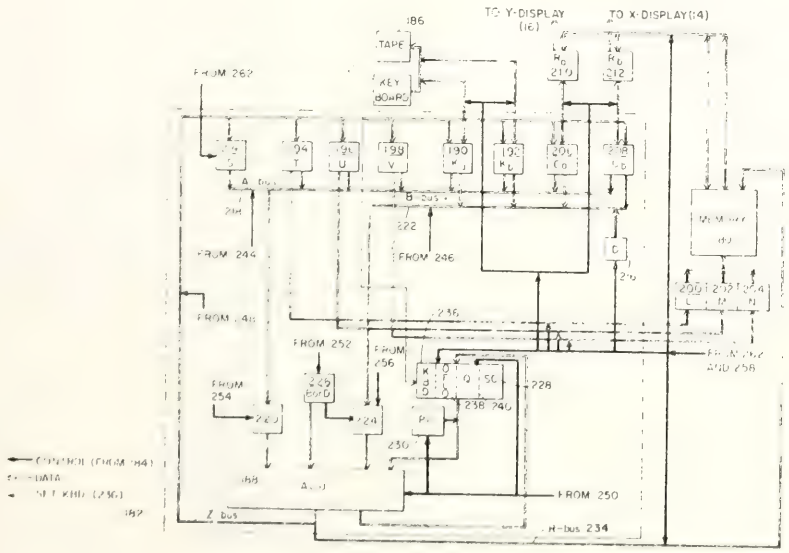
3,389,404	6/1968	Koster	340/172.5
3,346,853	10/1967	Koster et al.	340/172.5
3,389,379	6/1968	Erickson et al.	235/168 X
3,428,950	2/1969	Chang et al.	340/172.5
3,487,369	12/1969	King et al.	340/172.5
3,533,076	10/1970	Perkins et al.	340/172.5
3,588,841	6/1971	Ragen	340/172.5

Primary Examiner—Eugene G. Botz
Assistant Examiner—David H. Malzahn
Attorney—Martin Kirkpatrick

[57] **ABSTRACT**

A programmable desk type calculator has a display and a keyboard having a first group of keys for entering numerical values, a second group of keys for entering instructional values including subroutine designators, and a key for causing the calculator to display an extended precision result. The calculator also has a first memory for storing instructional and numerical values, a second memory for storing a plurality of fixed control words, each of which has a plurality of control fields and an arithmetic unit for operating on numerical values in accordance with a series of control words selected in response to an instructional value for producing a result which is displayed directly.

16 Claims, 13 Drawing Figures



United States Patent [19]

Boone

[11] **3,757,306**

[45] **Sept. 4, 1973**

[54] **COMPUTING SYSTEMS CPU**

[75] Inventor: **Gary W. Boone**, Houston, Tex.

[73] Assignee: **Texas Instruments Incorporated**, Dallas, Tex.

[22] Filed: **Aug. 31, 1971**

[21] Appl. No.: **176,668**

[52] **U.S. Cl.** **340/172.5**, 307/303

[51] **Int. Cl.** **G06f 7/00**, H03k 19/08

[58] **Field of Search** 340/172.5; 235/157; 307/238, 303

[56] **References Cited**

UNITED STATES PATENTS

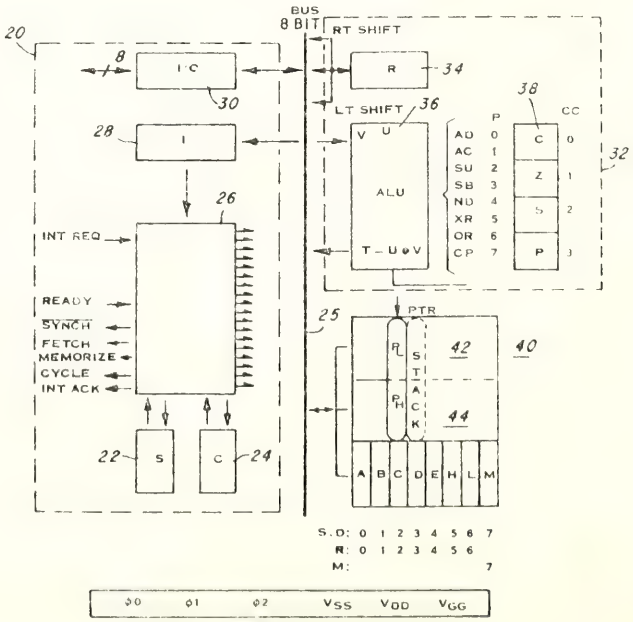
3,210,733	10/1965	Terzian et al.	340/172.5
3,597,641	8/1971	Ayres	307/303
3,641,511	2/1972	Cricchi et al.	307/238
3,611,437	10/1971	Varadi et al.	307/238
3,461,434	8/1969	Barton et al.	340/172.5
3,588,845	6/1971	Ling	340/172.5 X
3,560,940	2/1971	Gaensslen	340/172.5

Primary Examiner—Paul J. Henon
Assistant Examiner—Mark Edward Nusbaum
Attorney—Harold Levine, John G. Graham, et al.

[57] **ABSTRACT**

A central processing unit (CPU) is utilized in combination with external random access or serial memory units. The CPU includes a parallel arithmetic logic unit (ALU), accumulator and file register, program and memory address register, and a 7 level program address stack. The parallel processor includes programmable logic arrays, shift registers, and random access memories combined monolithically on a single chip. The CPU is capable of addressing up to 65 kilobytes of memory, and has an instruction cycle time on the order of 10 microseconds. Interface ligic synchronizes operation of the CPU with the external memory. An 8-bit parallel bus interconnects the functional elements of the CPU. An external 8-bit bus is used to interconnect the external memory units with the CPU. Multiplexing techniques enable both input and output data to be transmitted over the same bus, simplifying design and improving reliability.

8 Claims, 56 Drawing Figures



United States Patent

Haney et al.

[15] 3,702,988

[45] Nov. 14, 1972

[54] **DIGITAL PROCESSOR**

[72] Inventors: **Ralph D. Haney; James E. Zachar,** both of Dayton; **Charles J. Drozd,** Centerville, all of Ohio

[73] Assignee: **The National Cash Register Company,** Dayton, Ohio

[22] Filed: **Sept. 14, 1970**

[21] Appl. No.: **72,084**

[52] **U.S. Cl.** **340/172.5**

[51] **Int. Cl.** **G06f 7/48**

[58] **Field of Search** 340/172.5

[56] **References Cited**

UNITED STATES PATENTS

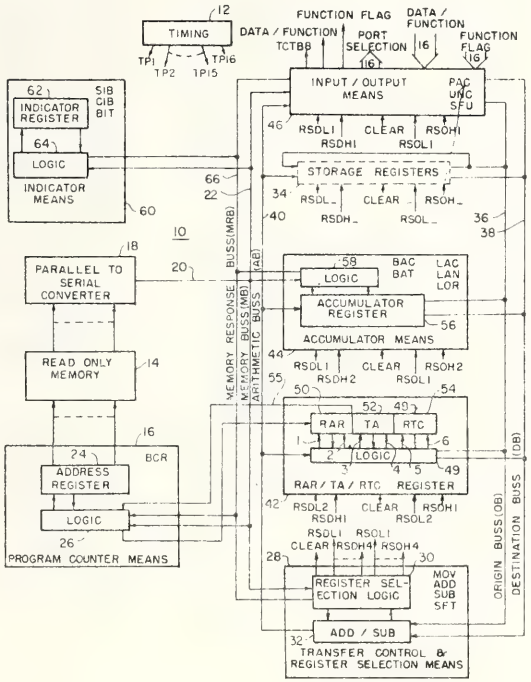
3,315,235	4/1967	Carnevale et al.	340/172.5
3,579,201	5/1971	Langley	340/172.5
3,391,394	7/1968	Ottaway	340/172.5
3,440,618	4/1969	Chinlund	340/172.5
3,480,914	11/1969	Schlaeppi	340/172.5

Primary Examiner—Paul J. Henon
Assistant Examiner—Ronald F. Chapuran
Attorney—Louis A. Kline, John J. Callahan and Harry W. Barron

[57] **ABSTRACT**

A digital processor built entirely of metal-oxide semiconductor devices constructed on integrated circuits by large-scale integration techniques is shown. The processor includes a read-only memory means which provides a series of coded instruction signals in a serial-by-bit manner to a memory buss line. A plurality of logic circuits is coupled to the memory buss line, and each responds to selected ones of the instruction signals to perform a certain operation. There is also provided a plurality of registers which can be used in processing information.

31 Claims, 23 Drawing Figures



United States Patent [19]

Hoff, Jr. et al.

[11] 3,821,715

[45] June 28, 1974

[54] **MEMORY SYSTEM FOR A MULTI-CHIP DIGITAL COMPUTER**

[75] Inventors: **Marcian Edward Hoff, Jr.,** Santa Clara; **Stanley Mazor,** Sunnyvale; **Federico Faggin,** Cupertino, all of Calif.

[73] Assignee: **Intel Corporation,** Santa Clara, Calif.

[22] Filed: **Jan. 22, 1973**

[21] Appl. No.: **325,511**

[52] **U.S. Cl.** .... **340/172.5,** 340/173 R, 340/173 SP, 307/238

[51] **Int. Cl.** **G06f 13/00,** G11c 11/44

[58] **Field of Search** ..... 340/172.5, 173 SP, 173 R; 307/238, 279

[56] **References Cited**

UNITED STATES PATENTS

3,460,094	8/1969	Pryor	340/172.5
3,641,511	2/1972	Cricchi et al.	307/238 X
3,680,061	7/1972	Arbab et al.	340/173 R
3,681,763	8/1972	Meade et al.	340/173 R
3,685,020	8/1972	Meade	340/172.5
3,702,988	11/1972	Haney et al.	340/172.5
3,719,932	3/1973	Cappon	340/173 R
3,731,285	5/1973	Bell	340/172.5
3,735,368	5/1973	Beausoleil	340/173 R
3,737,866	6/1953	Gruner	340/172.5
3,740,723	6/1973	Beausoleil et al.	340/172.5

OTHER PUBLICATIONS

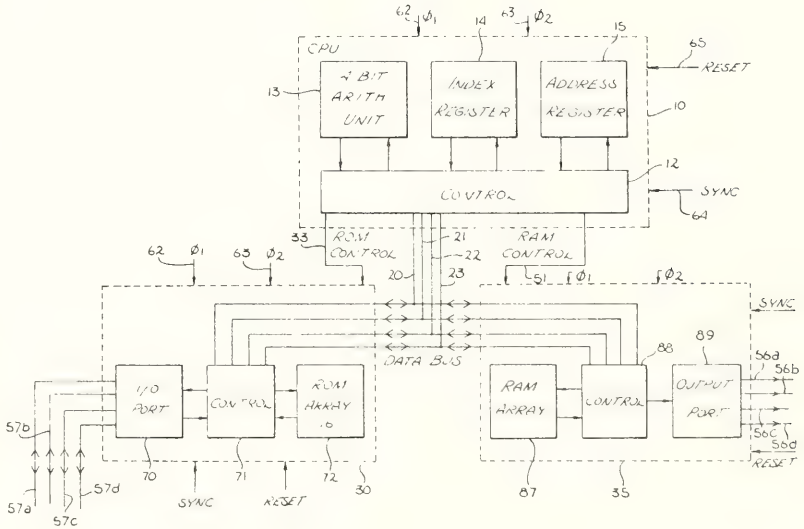
Schuenemann, "Computer Control" in IBM Technical Disclosure Bulletin, Vol. 14, No. 12, May 1972; pp. 3794–3795.

Primary Examiner—Paul J. Henon
Assistant Examiner—Melvin B. Chapnick
Attorney, Agent, or Firm—Spensley, Horn & Lubitz

[57] **ABSTRACT**

A general purpose digital computer which comprises a plurality of metal-oxide-semiconductor (MOS) chips. Random-access-memories (RAM) and read-only-memories (ROM) used as part of the computer are coupled to common bi-directional data buses to a central processing unit (CPU) with each memory including decoding circuitry to determine which of the plurality of memory chips is being addressed by the CPU. The computer is fabricated using chips mounted on standard 16 pin dual in-line packages allowing additional memory chips to be added to the computer.

17 Claims, 5 Drawing Figures



APPENDIX A - EXPLANATORY NOTES

Composite Total (Part 2B and Part 3): Part 2C of each profile contains an alphabetical listing of assignees. In some instances, assignees are listed in more than one place due to variations in the printing of the name. These variations occur for a number of reasons, such as typographical errors, changes in company names or differences in spacing or abbreviations. These variations also occur on the first pages of the patents which are shown in Part 3. In Parts 2B and 3 of each profile, which rank assignees according to number of patents held, the number of patents listed for certain assignees may be a composite resulting from the combination of different titles which in fact signify identical assignees. An asterisk appears next to these totals. This will alert the reader that the particular assignee is listed under more than one title in Part 2C or that different titles are grouped as one in Part 3. The assignees making up the composite groupings are listed below.

For: ALLEN-BRADLEY COMPANY
See Also: ALLAN-BRADLEY COMPANY

For: RAYTHEON COMPANY
See Also: RAYTHEON CORPORATION

For: TOKYO SHIBAURA ELECTRIC CO., LTD.
See Also: TOKYO SHIBAURA DENKI KABUSHITA KASHI

For: OLIVETTI, ING. C., + C. S.P.A.
See Also: ING. C. OLIVETTI & C., S.P.A.

For: MATSUSHITA ELECTRONICS CORPORATION
See Also: MITSUSHITA ELECTRONICS CORPORATION

For: SPERRY CORPORATION
See Also: SPERRY RAND CORPORATION

Application Filing Date: The application filing date information as set forth in Parts 1 and 2A of the profiles is determined by taking all patents which issued between 1967 and 1979 and distributing them according to the year the application was filed in the PTO. Patents which were granted prior to 1967 are not included since the application date information for these patents is not in the data base. Also, applications which were filed but never issued (roughly 30% of the total filings), as well as those applications which were still pending as of December 31, 1979 are not included. Thus, only those applications which were filed and subsequently became patents with patent grant dates between 1967 and 1979 are included.

While the length of time between the patent application date and the patent grant date varies from patent to patent, the current average pendency is approximately 22 months. Clearly many applications filed in 1979 were still pending at the end of 1979, as were a number of those filed in 1978. Thus application filing date data for these years is incomplete. While a small number of applications which were filed prior to 1978 were still pending, OTAF feels that the application date data prior to January 1978 is essentially complete. That is, the number shown for applications filed in the years prior to 1978 will not differ substantially with the passage of time, and this number is a true reflection of the number of applications

filed in that year which have and will become patents. However, for the subsequent years, 1978 and 1979, that number will increase as more applications filed in those years become patents.

For those years prior to 1967, it should be remembered that the numbers reflect only those applications which became patents between 1967 and 1979. Thus, the column "pre-66" does not include all applications filed before 1966 but only those which issued in 1967 and subsequently. The graph of this information in Part 1 of each profile is limited to the years 1968 to 1977 and thus is an accurate representation of activity based on the application dates of subsequently issued patents.

Assignee - This term refers to a company, organization or individual to which the inventor's rights to a patent are assigned. For the purpose of this publication, the assignee will in all cases refer to the assignee at the time the patent was granted. Approximately 80% of all U.S. patents are assigned when granted. By far, the largest portion of assignees are corporations.

Country Codes - The following country codes appear in Part 2D of the profiles.

DT - Federal Republic of Germany
EN - England
FR - France
JA - Japan
NO - Norway
SU - Union of Soviet Socialist Republics

Reference Citation Information (Part 4): During the examination of applications for U.S. patents, the examiner and the applicant may cite references which they believe to be representative of the prior art most closely related to the claimed invention. Such references are made of record in the application, indicating that they have been considered by the examiner. Part 4 of each profile sets forth data based on the references cited during the examination of patents which issued in the technology from 1975 through 1979. Citations may be U.S. patents, foreign patents or non-patent (literature) references, and the number of each is listed.

Under the heading, "Country of Origin of U.S. Patent References Cited," the residence countries of the inventors of the technology disclosed in the references are listed, together with the number of citations from each country. A particular U.S. patent may be cited as a reference in more than one application. Frequently-cited patents may be more important than those less frequently cited. Consequently, a list of the four "Most Frequently Cited U.S. Patents" is given along with the number of applications in which each was cited. The title pages of these patents are presented, which further identify the inventor and technology involved. The "Most Frequently Cited Assignees" is a list of the four assignees whose patents were used most often as references during the examination period of the patents which issued in the subject area. If a particular patent is used as a reference in more than one application, the "Number of Citations" will reflect each time it was cited.

APPENDIX B

OBTAINING PREVIOUS OTAF PUBLICATIONS**

Copies of the previous OTAF publications listed below are available from:

National Technical Information Service (NTIS)
5285 Port Royal Rd.
Springfield, Virginia 22161
(703) 487-4650

When ordering from NTIS, please give the publication title and its "COM" or "PB" number.

1. Initial Publication, May 1973
   COM 73-10767; Cost: Domestic - $11.00 Foreign - $22.00
   Describes OTAF program and gives sample reports on 24 wide ranging areas of technology in varying levels of detail.

2. Early Warning Report, December 1973
   COM 74-10150; Cost: Domestic - $16.00 Foreign - $32.00
   Spotlights those technological areas experiencing a high level of overall activity or of foreign activity. Reviews patent activity in a number of energy areas, including nuclear; solar; geothermal; and tide, wind and wave energy.

3. Third Report, June 1974
   COM 74-11383; Cost: Domestic - $12.00 Foreign - $24.00
   Presents an overview of the technological activity, across all technologies, of a group of selected foreign countries and a group of selected U.S. states. Extends energy area treatments to include oil shale and coal gasification technologies. Reviews additional high overall activity technological areas.

4. Fourth Report: A Review of Patent Ownership, January 1975
   COM 75-10050; Cost: Domestic - $10.00 Foreign - $20.00
   Identifies the 73 corporations and government agencies which received 500 or more patents during the five year period 1969-1973, and reviews and compares their patent activity across the spectrum of technology. Also reviews in terms of patent ownership, the patent activity during the same period, in nuclear energy technology and oil shale and coal gasification technology.

5. Fifth Report, August 1975
   COM 75-11142; Cost: Domestic - $11.00 Foreign - $22.00
   Reviews 60 technological areas, not previously reported on, experiencing a high level of overall activity or of foreign activity. Presents patent activity data in categories corresponding to 36 Product Fields of the Standard Industrial Classification System.

** SPECIAL NOTE: NTIS AND GPO PRICES ARE SUBJECT TO CHANGE WITHOUT NOTICE.

6. Sixth Report, June 1976
PB 254188; Cost: Domestic - $12.00 Foreign - $24.00
Reviews 15 technologies with unusually high activity by foreign resident inventors, and 22 high overall activity technologies; updates the 1973 reports on patent activity in solar and other natural energy sources, and adds reports on the use of waste material and wind for energy generation. Presents comparisons of patenting to R&D expenditures and R&D manpower allocations in six selected industries. The report concludes with a review of six most often cited patents in 1975, 5 U.S. and 1 foreign patent.

7. Seventh Report, March 1977*
PB 265792; Cost: Domestic - $13.00 Foreign - $26.00
Reviews historical patenting and trademark registration trends, and includes the most extensive collection of historical U.S. patent data ever presented in a single publication. Makes first use in the series of data relating to patents granted by foreign nations for a study of invention sources. Makes first use in the series of pending patent application data for forecasting. Presents brief reviews of 16 technologies experiencing high overall or foreign patent activity. Concludes with the series most comprehensive assessment of activity in a given technology, specifically in computer memories.

8. Eighth Report, December 1977*
PB 276375; Cost: Domestic - $10.00 Foreign - $20.00
Reviews U.S. patenting in the context of domestic vs. international patenting and analyzes the balance of patenting between the U.S. and other countries. Presents a study demonstrating the uniqueness of patents and the patent file as a technological resource. Concludes with an in-depth analysis of patent activity in geophysical exploration for hydrocarbons.

9. Ninth Report, March 1979*
PB 293380; Cost: Domestic - $12.00 Foreign - $24.00
Reviews "Top Fifty" most active technologies (U.S.P.C. subclasses) in three categories -- Most Active, Fastest Growing, and Most Foreign-Active -- for each of three broad groupings of technology -- Chemical, Electrical and Mechanical. Examines trends in domestic patenting and independent inventor patenting. Includes an extensive review of patenting in "Ferrous Metal" technologies. Concludes with a discussion of two experiments in the transfer of "appropriate technology" to small businesses and developing countries.

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PATENT PROFILE SERIES

1. PATENT PROFILES-Synthetic Fuels, December, 1979*
PB 80128572; Cost: Domestic - $14.00 Foreign - $28.00

Profiles the patent activity in ten specific areas of synthetic fuel technology dealing with the conversion of solid carbonaceous material to liquid or gaseous hydrocarbons. Starting materials include coal, oil shale, bituminous sands, wood and organic wastes.

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*Also available from the Government Printing Office - see page 248.

2. PATENT PROFILES-Solar Energy, January 1980*
PB 80190010; Cost: Domestic - $12.00 Foreign - $24.00

Profiles the patent activity in five specific areas directed to energy provided by the sun and in three areas directed to energy derived from other natural sources, such as wind, tide, wave, and geothermal. A cumulative profile of the five solar areas illustrates the dramatic growth in this field.

NTIS Microfilm of Previous Reports
Domestic - $3.50 per report; Foreign - $5.25 per report

*NOTE:

*The following publications may also be obtained from:

The Superintendent of Documents
U.S. Government Printing Office
Washington, D.C. 20402.

Their identification numbers and cost are:

. Seventh Report, 003-004-00542-4; Cost: Domestic - $4.25;

. Eighth Report, 003-004-00550-5; Cost: Domestic - $3.75;

. Ninth Report, 003-004-00559-9; Cost: Domestic - $4.00;

. PATENT PROFILES-Synthetic Fuels, 003-004-00566-1; Cost: Domestic - $5.50;

. PATENT PROFILES-Solar Energy, 003-004-00568-8; Cost: Domestic - $5.50.

APPENDIX C

OBTAINING ADDITIONAL INFORMATION OR SPECIAL REPORTS

Background

OTAF's computerized base of data relating to the patent file includes, at present:

- all subclasses of the U.S. Patent Classification System
- the relationship of all subclasses of the U.S. Patent Classification System to the Standard Industrial Classification System in 55 Product Fields and Product Field combinations
- for U.S. patents issued since 1963,
  - the ownership at time of issue in seven categories (U.S. government, foreign government, U.S. corporation, foreign corporation, U.S. individual, and unassigned)
  - the country or state of residence of the inventor
- for U.S. patents issued since 1967,
  - the date the application for patent was filed in the U.S. Patent and Trademark Office
- for U.S. patents issued since 1969,
  - the specific (i.e. named) ownership of all patents which, at time of issue, were organizationally owned (e.g., by a corporation, foundation, government agency).
  - the patent title
- for U.S. patents issued since 1975,
  - the address of the inventor, and the field of search and references cited in the patentability examination leading to the patent grant.

Special Reports

Data can be retrieved on the basis of any one or any combination of the factors listed above, manipulated on most any given basis and presented in a number of formats, e.g., lists, tables, graphs, charts, etc. This flexibility is illustrated by the various types of reports presented in this Appendix and in the previous OTAF general distribution publications.

OTAF has developed several standard special report programs which are designed to extract and present, for any given grouping of patents, a wide variety of data. Excerpts from samples of reports prepared using these programs are included in this Appendix.

STANDARD SPECIAL REPORTS

"Technology Profile" Report

This is a multi-part report utilizing many of the elements in OTAF's data base to provide a detailed patent profile for a specific technology or grouping of technologies. Information provided includes rate of patenting, origin of patenting, type of assignment and specific assignment, patent numbers and their titles, and names and addresses of "independent" inventors. There are four parts (parts A,B,C,&D) to a complete report. Part A includes patenting activity percentages, general assignment and distribution of origin of patents; Part B includes, by assignee, the numbers of patents granted by both grant date and year of application filing, ranked by assignee with highest number of patents; Part C includes, alphabetically, the assignees and their specific patent numbers and titles; Part D gives the name and address of the inventors of patents unassigned at time of issue. Any Part can be prepared depending on your needs. This PATENT PROFILES publication is itself an example of the kinds of data presented in a "Technology Profile" report.

"Organizational Profile" Report

Beginning on page 252 are excerpts from the second of OTAF's standard format special reports, the Organizational Profile. This report profiles patent activity across the classes and subclasses of the U.S. Patent Classification System. Alternatively, these reports may be limited to specific classifications. A report for Communications Satellite Corp. is given as an example. Two pages of the 40 page report are included. This type of report can be prepared, for example, on the patents of any organization or grouping of organizations, or on the patents granted to the residents of any state or country or grouping of states or countries.

Multi-Corporate Patent Activity Profile

Like the above described Organizational Profile, this report also profiles patent activity across the classes and subclasses of the U.S. Patent Classification System. Multi-corporate Profiles may be limited to specific classifications. In this report the activty of up to eight organizations can be profiled simultaneously, facilitating comparisons between organizations. Unlike the Organizational Profile, no patent numbers or patent titles are given.

SIC Product Field Reports

On pages 254 to 256 is a listing of Standard Industrial Classification (SIC) Product Fields for which a concordance exists with subclasses of the U.S. Patent Classification System. Special patent reports, such as the "Technology Profile" Report can be prepared for any of these Product Fields.

How to Obtain Special Reports

1. In making an initial determination of interest in a OTAF special report, you are urged to review the data items that are available and decide if any one or combination of them might be useful to your needs. Special attention should be given to the standard format reports to determine if these multi-purpose, relatively low cost reports would meet your needs.

2. In most instances, interest, once determined, will be limited to particular technological areas or to particular organizations owning patents. In the case of technological areas, their definition is of key importance and must ultimately be in terms of classes and sub-classes of the U.S. Patent Classification System. If you are unfamiliar with the U.S. Patent Classification System, develop as clear and precise an explanation of your area(s) of interest as possible. For assignment information, the parent organization and its subsidiaries of interest should be identified. Recent name changes (e.g. Esso-Exxon), if known, should be indicated.

3. At this point, you should contact OTAF, indicate the type of information you desire and, if you wish, what your needs are. (Perhaps alternatives can be suggested to better meet those needs). If you cannot provide class and subclass definition of your area of interest, OTAF will attempt to do that for you, using your description of the area.

4. Once there is a clear mutual understanding of the information you want, the format in which you want it and the area(s) to be included, an estimate of cost will be developed and provided to you along with a statement of the work to be done.

5. Once agreement on work to be done and cost is reached, and payment is received, the report will be prepared and provided.

Costs

All special reports are prepared on a cost reimbursable basis. These costs may vary widely - from as low as $100.00 for some forms of our standard format reports, to several thousand dollars for complex and large scale treatments of many technological categories. The preparation of non-standard, specially-tailored reports, requiring extensive professional time, programming and/or computer time is subject to the availability of OTAF resources. Cost estimates for specifically requested special reports will be provided prior to report preparation.

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SAMPLE ORGANIZATIONAL PROFILE REPORT - COMMUNICATIONS SATELLITE CORPORATION

EXPLANATION OF DATA

DESCRIPTION OF PATENT PROFILES

THE REPORT PROFILES ONLY THOSE PATENTS FALLING INTO A PARTICULAR "CATEGORY" (E.G., SPECIFIC OWNERSHIP, COUNTRY OR STATE OF INVENTOR RESIDENCE), BY THE U.S. PATENT CLASSIFICATIONS INTO WHICH THOSE PATENTS HAVE BEEN PLACED.

EACH MAJOR PATENT CLASSIFICATION (CLASS) IS IDENTIFIED BY ITS TITLE. THEN, FOR EACH OF THE SUBCLASSES WITHIN THAT CLASS WHEREIN PATENTS FROM THE "CATEGORY" HAVE BEEN PLACED, THE FOLLOWING ARE GIVEN:

--TOTAL PATENTS
--OR (ORIGINAL) PATENTS
--XR (CROSS-REFERENCE) PATENTS
--PCT (PERCENT) OF TOTAL OR WITHIN THE "CATEGORY"
--PCT (PERCENT) OF ALL (OR & XR) PATENTS WITHIN THE "CATEGORY"

ALSO GIVEN ARE THE PATENT NUMBERS OF THE "CATEGORY" PATENTS IN THAT CLASSIFICATION. THE TYPE OF CLASSIFICATION (OR orXR) ASSIGNED TO EACH PATENT IS SHOWN IN PARENTHESES FOLLOWING THE PATENT.

FOR PATENTS ISSUING IN 1969 AND SUBSEQUENTLY, THE PATENT TITLES ARE GIVEN. (NOTE: ANY SYMBOLS IN A PATENT TITLE WHICH ARE NOT AVAILABLE ON THE COMPUTER PRINTER ARE SPELLED OUT, EG., β IS SHOWN AS BETA. SUPERSCRIPTS AND SUBSCRIPTS ARE INDICATED BY ENCLOSURE BETWEEN UPWARDLY OR DOWNWARDLY FACING SLASHES, E.G. , H_2O IS SHOWN AS H/2 \ O AND Y^2X IS SHOWN AS Y \2/X.)

PATENTS INCLUDED IN PROFILE

THE PATENTS INCLUDED IN THE REPORT ARE THOSE WHICH, ACCORDING TO THE DATA OF RECORD IN THE OTAF COMPUTER DATA BASE, FALL WITHIN THE CATEGORY COVERED IN THE REPORT. THESE CATEGORY DATA ARE RECORDED AT THE TIME OF PATENT ISSUE AND ARE ESSENTIALLY ACCURATE. HOWEVER, ANY PATENT LISTING OR DATA PROVIDED IN THIS REPORT SHOULD NOT BE CONSIDERED TO BE INCLUSIVE OF ALL RELEVANT PATENTS, NOR EXCLUSIVE OF ALL NON-RELEVANT PATENTS.

OTAF SPECIAL REPORT
CLASSIFICATION PROFILE - (1969 - 1977) PATENTS ASSIGNED TO THE COMMUNICATIONS SATELLITE CORP.

LASS 179 - TELEPHONY

SUBCLASS 100.3 A (CONTINUED)

3795768 (XR) - HOLOGRAPHIC IMAGE SCANNER/RECORDER SYSTEM

SUBCLASS 100.3 G TOTAL 1 (OR) 0 (XR) 1 PCT OF TOTAL OR 0.0 PCT OF ALL (OR+XR) .2

3795768 (XR) - HOLOGRAPHIC IMAGE SCANNER/RECORDER SYSTEM

SUBCLASS 170.2 TOTAL 8 (OR) 6 (XR) 2 PCT OF TOTAL OR 4.3 PCT OF ALL (OR+XR) 1.6

3780233 (OR) - ADAPTIVE ECHO CANCELLERS WITH COMPANDORS
3789165 (OR) - ECHO CANCELLER WITH VARIABLE THRESHOLD
3836734 (OR) - ADAPTIVE ECHO CANCELLER WITH MULTI-INCREMENT GAIN COEFFICIENT CORRECTIONS
3894200 (OR) - ADAPTIVE ECHO CANCELLER WITH DIGITAL CENTER CLIPPING
4021623 (OR) - AUTOMATIC H-REGISTER CLEAR FOR PREVENTION OF ERRONEOUS CONVOLUTION IN DIGITAL ADAPTIVE ECHO CANCELLE
R
4064379 (OR) - LOGARITHMIC ECHO CANCELLER
3937907 (XR) - DIGITAL ECHO SUPPRESSOR
4031338 (XR) - ECHO SUPPRESSOR USING FREQUENCY-SELECTIVE CENTER CLIPPING

SUBCLASS 170.6 TOTAL 5 (OR) 4 (XR) 1 PCT OF TOTAL OR 2.9 PCT OF ALL (OR+XR) 1.0

3725612 (OR) - ECHO SUPPRESSOR BREAK-IN CIRCUIT
3896273 (OR) - DIGITAL ECHO SUPPRESSOR
3937907 (OR) - DIGITAL ECHO SUPPRESSOR
4024358 (OR) - ADAPTIVE ECHO CANCELLER USING DIFFERENTIAL PULSE CODE MODULATION ENCODING
3894200 (XR) - ADAPTIVE ECHO CANCELLER WITH DIGITAL CENTER CLIPPING

SUBCLASS 170.8 TOTAL 1 (OR) 1 (XR) 0 PCT OF TOTAL OR .7 PCT OF ALL (OR+XR) .2

4031338 (OR) - ECHO SUPPRESSOR USING FREQUENCY-SELECTIVE CENTER CLIPPING

OTAL CLASS 179 TOTAL 76 (OR) 43 (XR) 33 PCT OF TOTAL OR 30.7 PCT OF ALL (OR+XR) 15.5

LASS 200 - ELECTRICITY, CIRCUIT MAKERS AND BREAKERS

SUBCLASS 8 A TOTAL 1 (OR) 0 (XR) 1 PCT OF TOTAL OR 0.0 PCT OF ALL (OR+XR) .2

3740499 (XR) - OIL FILLED STEPPING SWITCH

SUBCLASS 8 B TOTAL 1 (OR) 1 (XR) 0 PCT OF TOTAL OR .7 PCT OF ALL (OR+XR) .2

3740499 (OR) - OIL FILLED STEPPING SWITCH

SUBCLASS 11 TC TOTAL 1 (OR) 0 (XR) 1 PCT OF TOTAL OR 0.0 PCT OF ALL (OR+XR) .2

3740499 (XR) - OIL FILLED STEPPING SWITCH

OTAL CLASS 200 TOTAL 3 (OR) 1 (XR) 2 PCT OF TOTAL OR .7 PCT OF ALL (OR+XR) .6

SIC PRODUCT FIELDS

PRODUCT FIELDS	SIC CATEGORY
Food and Kindred Products	20
Textile Mill Products	22
Chemicals and Allied Products	28
Chemicals, Except Drugs & Medicines	281, 282, 284-289
Basic Industrial Inorganic & Organic Chemistry	281, 286
Industrial Inorganic Chemistry	281
Industrial Organic Chemistry	286
Plastics Materials & Synthetic Resins	282
Agricultural Chemicals	287
All Other Chemicals	284, 285, 289
Soap, Detergents, and Cleaning Preparations, Perfumes, Cosmetics & Other Toilet Preparations	284
Paints, Varnishes, Lacquers, Enamels, and Allied Products	285
Miscellaneous Chemical Products	289
Drugs and Medicines	283
Petroleum & Natural Gas Extraction & Petroleum Refining	13, 29
Rubber & Miscellaneous Plastics Products	30
Stone, Clay, Glass and Concrete Products	32
Primary Metals	33, 3462, 3463
Primary Ferrous Products	331, 332, 3399, 3462
Primary & Secondary Non-Ferrous Metals	333-336, 339 (except 3399), 3463
Fabricated Metal Products	34 (except 3462, 3463, 348)

PRODUCT FIELDS	SIC CATEGORY
Machinery, Except Electrical	35
Engines & Turbines	351
Farm & Garden Machinery & Equipment	352
Construction, Mining & Material Handling Machinery & Equipment	353
Metal Working Machinery & Equipment	354
Office Computing & Accounting Machines	357
Other Machinery, Except Electrical	355, 356, 358, 359
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General Industrial Machinery & Equipment	356
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PRODUCT FIELDS	SIC CATEGORY
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Motor Vehicles & Other Transportation	348, 371, 373-376, 379
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Ship & Boat Building & Repairing	373
Railroad Equipment	374
Motorcycles, Bicycles & Parts	375
Miscellaneous Transportation Equipment	379 (except 3795)
Ordnance Except Missiles	348, 3795
Aircraft & Parts	372
Professional & Scientific Instruments	38 (except 3825)

APPENDIX D

ACKNOWLEDGEMENTS

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